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Advancements and hurdles in contact engineering for miniaturized sub-micrometer oxide semiconductor devices

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With conventional silicon-based devices approaching their physical scaling limits, alternative channel materials, such as transition metal dichalcogenides and oxide semiconductors (OSs), have emerged as promising candidates for extending Moore's law and advancing performance, power efficiency, area scaling, and cost-effectiveness. Among these, OSs stand out as particularly promising, having already been established as the industry standard for high-end active-matrix organic light-emitting diodes due to their moderate mobility, extremely low off-current, steep subthreshold swing, excellent uniformity, and compatibility with low-temperature fabrication processes. However, to enable the deployment of OSs in more demanding applications, such as 3D dynamic random-access memory and other advanced electronic systems, further improvements are necessary, particularly in terms of enhancing on-current and hydrogen stability and reducing contact resistance (R_C). In this work, we review strategies to optimize electrical contact properties to improve the device performance of OSs and examine the underlying mechanism of R_C from a device physics perspective.

1. Introduction

Since the Hosono group's discovery of amorphous indium gallium zinc oxide (a-IGZO) in 2004, amorphous oxide semiconductors (AOSs) have garnered significant attention as channel materials in thin-film transistors (TFTs).[1] In 2013, LG Display pioneered the mass production of active-matrix organic light-emitting diode (AMOLED) televisions by using an IGZO-based backplane on 8th-generation glass substrates, setting a new industry standard for large-sized displays.[2,3] The success of IGZO electronics is largely attributed to its reasonable electron mobility, extremely low off-current, excellent large-area uniformity, compatibility with low-temperature processing, and reliable electrical stability.[4–6] As the semiconductor industry grapples with the physical limitations of further miniaturization, which is critical for improving performance, power efficiency, area scaling, and cost-effectiveness (often referred to as PPAC), AOSs have emerged as potential alternative channel materials. In particular, oxide semiconductors (OSs) have attracted considerable attention as channel materials for next-generation vertical channel transistors (VCTs), 2T0C and 3D dynamic random-access memory (DRAM) due to their aforementioned unique properties.[7–10] Their wide bandgap (E_G) enables promising solutions to the scaling and leakage challenges encountered in DRAM devices.[11,12] From a processing perspective, the atomic layer deposition (ALD) of the OS channel layer offers excellent conformality on complex nanoscale structures, presenting a compelling alternative to the conventional sputtering deposition method commonly used in display devices. This growing interest in AOSs is evidenced by the rising number of research papers on oxide semiconductor (OS) devices that are presented at major semiconductor conferences, such as the IEEE International Electron Device Meeting (IEDM) and the Symposium on VLSI Technology and Circuits, increasing from just 2 papers in 2016 to 40 in 2023.[8,13,14]

Scaling AOS-based devices poses several challenges, including short channel effects (SCEs) such as drain-induced barrier lowering, hot carrier effects, high-temperature process compatibility, threshold voltage (V_{TH}) control, hydrogen-related reliability, and contract resistance (R_C). Notably, as the channel length decreases, the influence of R_C and channel shortening at the metal–semiconductor (M–S) interface becomes increasingly pronounced, emerging as a critical barrier to device performance. R_C has long been a critical issue in the semiconductor industry because it limits further miniaturization and degrades the performance of nanoscale devices.[15–18] While substantial efforts have successfully reduced R_C in Si-based devices,

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AOSs, which have predominantly been utilized in the display industry, have faced less pressure to optimize electrical contact properties due to their comparatively less stringent scaling requirement, attributed to the larger contact hole sizes ($\geq 10^{-8}$ cm^2) relative to those (approximately 10^{-12} cm^2) in the semiconductor industry.[19] Consequently, the R_C in AOS TFTs remains approximately four orders of magnitude higher than in Si-based metal oxide semiconductor field-effect transistors. However, as advancements in high-resolution technology and DRAM drive the need for further scaling and enhancing of device performance, reducing R_C in AOSs is becoming an increasingly critical factor.[20,21] While this review primarily focuses on reducing R_C by optimizing ohmic contacts, the development of Schottky barrier (SB) TFTs, which operate in the deep subthreshold regime, has also been studied for enabling low-power operation in wearable devices and sensor circuitries.[22,23]

Although numerous comprehensive review articles on AOSs exist, the majority have predominantly focused on optimizing high performance and stability.[2,5,11,24–27] In this work, we shift the emphasis towards understanding the origin of R_C at the M–S interface and provide a classification of the latest methods for reducing R_C in AOS TFTs. Additionally, we compare the material properties and the enhancement strategies of AOSs with those of Si-based devices. In Section 2, we discuss the charge carrier injection mechanisms at the M–S junction and the methodologies employed to extract electrical contact properties. Section 3 covers recent advancements in reducing R_C in OS TFTs, broadly categorizing the approaches into band alignment and carrier density strategies, with a detailed view of leading studies on carrier density optimization. Finally, we propose potential strategies to further decrease R_C in future AOS-based devices.

2. Metal–semiconductor junction

2.1 Junction classification: formation of a Schottky barrier

M–S junctions typically exhibit an energy mismatch at the interface, leading to the formation of a Schottky barrier as a result of the difference in Fermi energy (E_F) between the metal and the semiconductor. In an ideal case in which surface interactions are negligible, the SB height (Φ_B) is determined solely by the metal work function (Φ_M) and the electron affinity of the semiconductor (χ), with Φ_B expressed as $\Phi_B = \Phi_M - \chi$.[28,29] Based on the relationship between the metal and semiconductor work functions, M–S junctions can be classified as either ohmic contacts (when $\Phi_M < \Phi_S$) or Schottky contacts (when $\Phi_M > \Phi_S$).

In practice, however, modifying Φ_B by using different metals is challenging. Experimental studies indicate that for most common semiconductors, the Φ_B at the M–S interface is relatively independent of the metal's work function, a phenomenon known as Fermi-level pinning (FLP). FLP at the charge neutral level (CNL) arises from several factors, including native point defects, interface trap states (D_{it}), and metal-induced gap states (MIGS).[30–33] Among these, MIGS are the most significant contributor to FLP, originating from the penetration of the metal's electron wave function into the semiconductor and forming tailing states within the semiconductor's E_G.[34,35] Furthermore, the extent of FLP is influenced by the E_G, with semiconductors that have a narrower E_G exhibiting stronger FLP due to the slower decay of the penetrated wave function.[36]

This behavior is quantitatively described by the pinning factor (S), defined as $S = d\Phi_B/d\Phi_M$. When $S = 1$, known as the Schottky–Mott limit, the Φ_B is free of FLP and depends solely on the Φ_M, reflecting an ideal M–S junction. In contrast, when $S = 0$, Φ_B becomes independent of Φ_M, with the E_F fully pinned at a fixed energy level, which is referred to as the CNL and is defined as the Bardeen limit (Fig. 1(c)). In reality, most semiconductors exhibit behavior between these two extremes, with smaller S values indicating stronger pinning. Studies have shown a correlation between S and electronegativity difference (ΔX), where ionic materials tend to exhibit S values near 1, while covalent materials are positioned closer to $S = 0$ (Fig. 1(d)).[37] This discrepancy arises because ionic materials have minimal surface energy changes, while covalent materials experience significant surface energy perturbation due to dangling bonds, resulting in stronger FLP and lower S values. It is noted that Schottky contacts can be employed selectively based on the specific device applications. Promising Schottky contact between oxide channel (*e.g.*, ZnO, IGZO) and metals (*e.g.*, Ag, Pt, Pd) can be achieved through low-temperature processing, making them suitable for use as a gate stack in MESFET.[21,22,38–40] However, their application in DRAM access transistors, which require a high thermal budget, remains challenging due to significant leakage currents and adverse interface deterioration.

2.2 Charge injection mechanism

The effective Φ_B at the M–S interface is a key determinant of current flow, with charge injection influenced by factors such as doping density (N_e), temperature, and applied voltage. The N_e directly affects the barrier width (x_d), which is described by the equation $x_d = (2k_s\varepsilon_0\Phi_M/qN_e)^{-1/2}$. N_e plays a crucial role in determining the current transport mechanism, which can be classified into thermionic emission (TE), thermionic-field emission (TFE), and field emission (FE) (Fig. 2(a)).[41] In lightly doped semiconductors, current predominantly flows *via* TE, where carriers are thermally excited and overcome the SB due to the wide x_d. As x_d increases, the barrier width narrows, and tunneling begins to play a role in the conduction mechanism. In a semiconductor with an intermediate N_e, thermally excited carriers partially tunnel through the SB, a process known as TFE. When x_d becomes sufficiently narrow due to high doping levels, carrier injection occurs through direct tunneling, forming an ohmic contact, a process referred to as FE, though this is rarely observed. The distinction between these charge injection mechanisms is governed by the comparison of thermal energy of k_BT to the characteristic energy E_{00}, defined by the equation $E_{00} = (N_e/\varepsilon_S m^*)^{1/2} qh/4\pi$. According to conventional demarcation points, current transport is dominated by TE when $E_{00} \leq 0.5kT$, by TFE when $0.5kT < E_{00} < 5kT$, and by FE when $5kT \leq E_{00}$ (Fig. 2(b)).

2.3 Extraction method: the gated transmission line method

The R_C in AOS TFTs is closely associated with the voltage required for charge transport across M–S interfaces at both

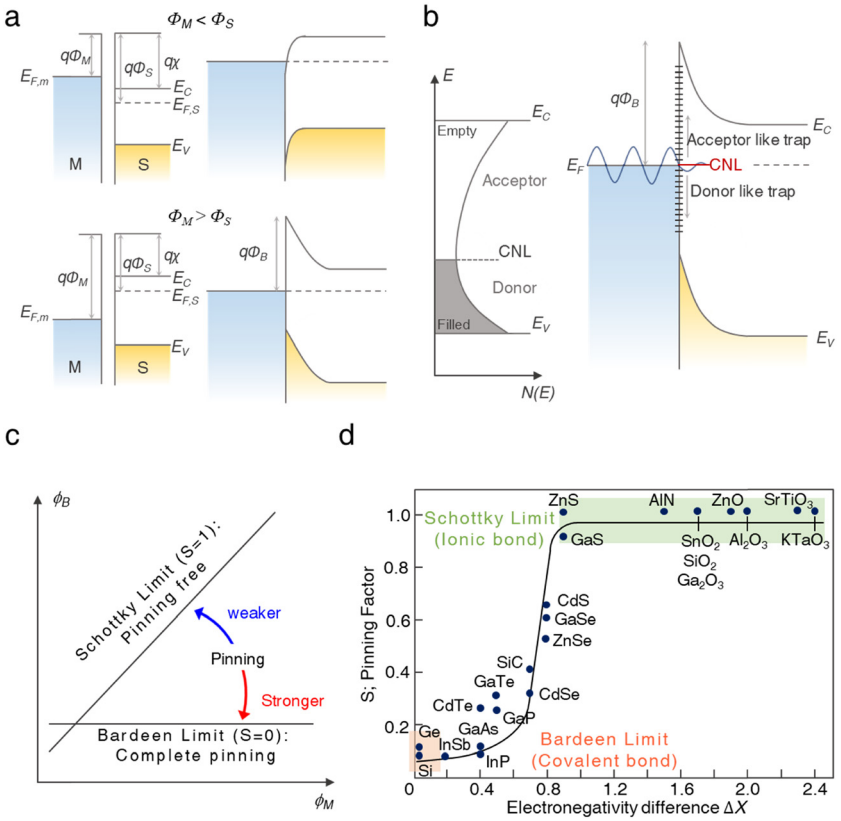

Fig. 1 (a) Energy band diagram illustrating Schottky and Ohmic contact in an ideal case. (b) Energy band diagram showing the effect of Fermi-level pinning (FLP) due to metal-induced gap states (MIGS, right), with a schematic of the charge neutral level as the branch point of the MIGS (left). (c) Schematic Φ_B–Φ_M plot indicating the degree of FLP at the metal–semiconductor interface. (d) Collected data showing the dependence of the pinning factor (S) on the electronegativity difference.

the source-channel and channel-drain junctions. The applied voltage (V_{app}) is distributed between the contact and channel regions, as expressed by the equation $V_{app} = 2\Delta V_{SD} + \Delta V_{Ch} = I_D(2R_C + R_{ch})$ (Fig. 3(a)). Here, ΔV_{SD} represents the voltage drop at the source and drain (S/D) and the channel interface, which primarily comes from the R_C that results from the energy barrier impeding carrier injection at the M–S junction. Given the significant impact R_C has on the electrical properties of AOS-based devices, accurate measurement of R_C is essential for evaluating contact enhancement strategies (Section 3).

Both R_{ch} and R_C exhibit gate bias (V_G) dependency due to the shift in the Fermi level within the semiconductor and the gate-field-induced reduction of the barrier height and width at the M–S interface (Fig. 3(b)). To accurately characterize R_C, the gated

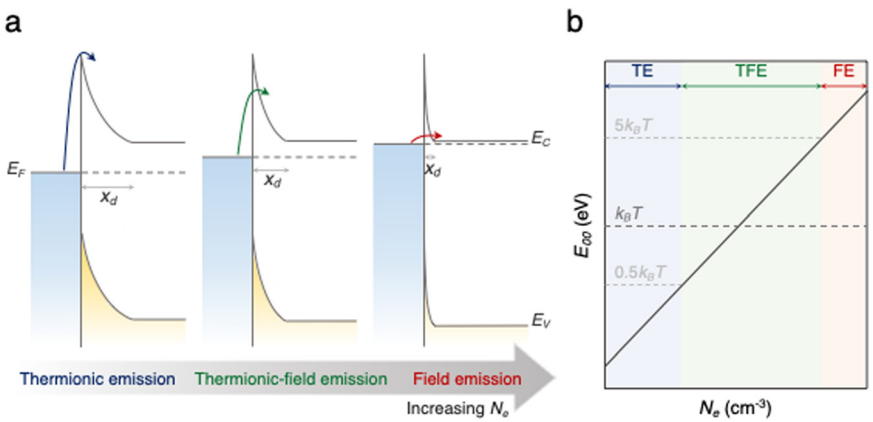

Fig. 2 (a) Schematic representation of the carrier transport at the metal–semiconductor interface as doping concentration increases. (b) E_{00} as a function of doping density, illustrating the three charge injection modes: thermionic emission (TE) when $E_{00} \leq 0.5kT$, thermionic-field emission (TFE) when $0.5kT < E_{00} < 5kT$, and field emission (FE) when $5kT \leq E_{00}$.

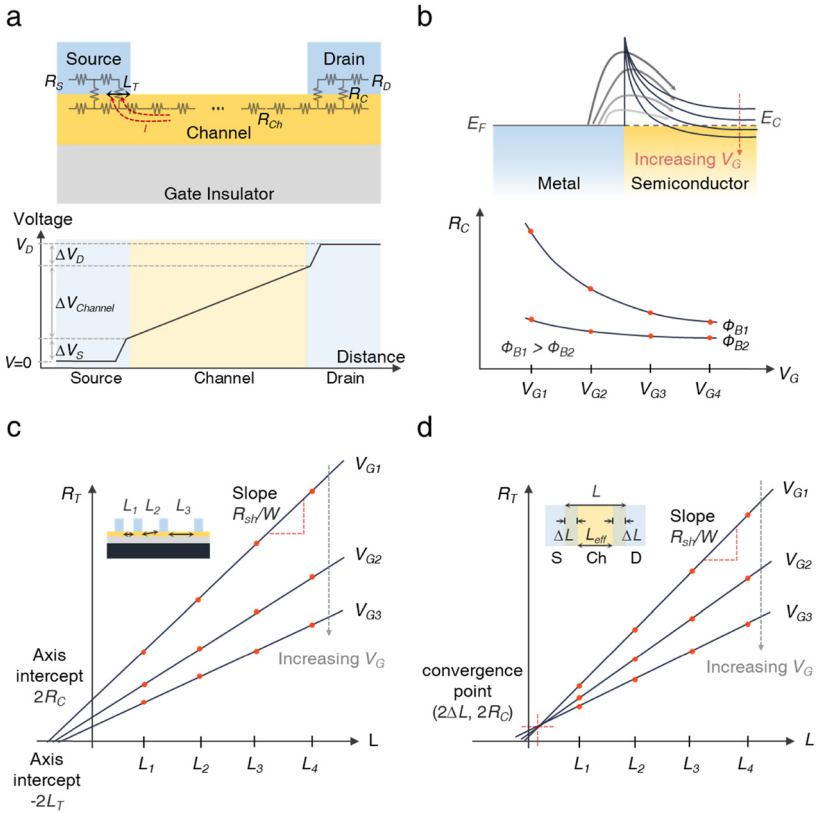

Fig. 3 (a) Schematic representation of a device illustrating the resistor network $R_T = R_{ch} + 2R_C$, along with a voltage profile indicating the voltage drop across the drain–channel–source region. (b) Energy band diagram showing the barrier decreasing as V_G increases, with a plot demonstrating the V_G dependence of R_C for high V_G and low Φ_B. (c), (d) Schematic graphs for a transmission line method (TLM) of R_T as a function of L.

transmission line method (g-TLM), also known as the gated transfer length model, is commonly employed. This method analyzes current–voltage (I–V) characteristics at different gate voltages ($V_G \gg V_T$) in the linear region ($V_D \rightarrow 0$) using a set of devices with varying channel lengths (L), resulting in a family of TLM curves. The I–V characteristics in the linear region are described by the equation:[28]

$$I_D = \mu_{FE} C_{OX} \frac{W}{L_{eff}} \left(V_G - V_T - \frac{1}{2} V_D \right) V_D \quad (1)$$

where L_{eff} is the effective channel length, defined as $L_{eff} = L - 2\Delta L$, with L being the mask channel length and ΔL accounting for process bias and lateral dopant diffusion. Thus, R_{ch} can be expressed as:[42]

$$R_{ch} = \frac{V_D}{I_D} = \frac{L - 2\Delta L}{W \mu_{FE} C_{OX} \left(V_G - V_T - \frac{1}{2} V_D \right)} \quad (2)$$

Taking R_C into account, the total device resistance (R_T) is given by:

$$R_T = R_{ch} + 2R_c = \frac{L - 2\Delta L}{W \mu_{FE} C_{OX} \left(V_G - V_T - \frac{1}{2} V_D \right)} + 2R_c \quad (3)$$

Because R_c remains constant while R_{ch} varies linearly with L, plotting R_T against L at a fixed V_G yields a straight line. If no intersection occurs (Fig. 3(c)), $\Delta L = 0$ and R_C become dependent on V_{GS} due to its correlation with carrier density. Here R_C and R_{sh}, where $R_{ch} = R_{sh} L/W$, can be extracted as a function of V_G. Alternatively, if an intersection occurs, $\Delta L \neq 0$, the convergence point indicates $2\Delta L$ and $2R_C$, in accordance with eqn (3). The value of ΔL generally arises from the diffusion of oxygen vacancies (V_O), which is more pronounced in the OSs with a higher concentration of V_O.[43] This diffusion leads to a reduction in SB width, thereby facilitating carrier injection and rendering electron injection independent of V_G.

3. Improvement method

When silicon is directly interfaced with metals, a Schottky junction forms due to Fermi level pinning, which arises from MIGS and the thermal instability caused by metal–silicon interdiffusion.[44] To overcome this issue, a silicide coupling layer is often introduced at the interface, creating an ohmic contact that reduces R_C while enhancing both the thermal and structural stability of the junction (Fig. 4(a)). Extensive research on improving the electrical contact properties of Si-based devices has focused on the use of different silicides, such as $TiSi_2$, NiSi, and $CoSi_2$, to optimize these properties.[45–49]

In indium-based OSs, such as a-IGZO, IZTO, and IGO, recent research efforts have focused on reducing the effective Φ_B at the metal–OS interfaces. The indium-based channels generally have relatively high work functions, typically exceeding 4 eV.[50–52]

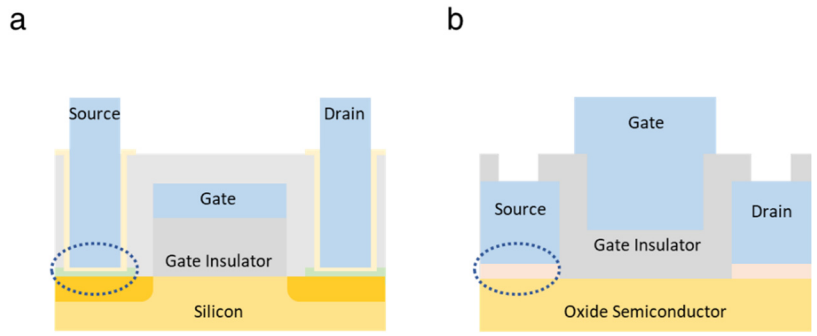

Fig. 4 Schematic illustrations of (a) silicon and (b) OS transistors. A number of different silicides are used to decrease the contact resistance in silicon transistors. In OS transistors, several methods are used, such as formation of a conduction region or insertion of an interlayer between the OS and the source or drain.

Despite efforts to pair these semiconductors with metals with similarly high Φ_M, achieving a low Φ_B remains a significant challenge. To overcome this, two primary approaches have been explored: (1) the formation of an n^+-doped conduction region at the M–S interface, and (2) the insertion of interlayers (ILs) to modify the interface (Fig. 4(b)). The anticipated advantages and limitations of these methods are outlined in Table 1, with their corresponding electrical properties detailed in Table 2. A comprehensive discussion of both strategies is provided in the following section.

3.1. Conductive region formation

3.1.1. Metal-induced methods. The use of metals with a high reducing power as S/D electrodes has been extensively studied as a means to create an n^+-doped region at the M–S interface. When such a metal (*e.g.*, Al, Ti, W) is inserted between the indium-based channel and the S/D electrodes, their strong reductive nature allows them to extract oxygen from the channel, owing to the relatively weak In–O bonds in the OS. This process generates V_O and free carriers, forming an n^+ conduction layer that reduces both the Φ_B and R_C.

Al-induced method. In a study by Yang *et al.*, self-aligned top-gate a-IGZO TFTs were fabricated, focusing on the Al-induced doping effect to create conductive S/D regions.[65] Post-deposition annealing (PDA) at 200 °C after Al deposition significantly increased V_O at the Al/a-IGZO interface. X-ray photoelectron spectroscopy (XPS) of the O1s spectra revealed an increase in V_O from 27% to 58% after the 200 °C PDA. Additionally, a shift in the In 3d XPS peaks indicated the

Table 1 Anticipated advantages and limitations of the discussed methods

	Approach	Pros.	Cons.
Conductive region formation	Metal-induced	No additional processing required	Formation of unwanted MO_x interfacial layers
	Doping	Broadly investigated	Deterioration of the OS surface
			Temporal instability
			Limited process margin
Interlayer insertion	OS engineering	No additional processing required	Alteration of overall electrical properties
	n^+ layer	Without deterioration of the OS surface	Requires additional processing steps
	DB layer	Prevents intermixing at the interface	Limitation in further improvement

Table 2 Summary of advancements in improving electrical contact properties in OS TFTs reported to date

Approach	OS	Deposition method	W/L (μm)	R_cW (Ω cm)	ρ_C (Ω cm^2)	μ_{FE} (cm^2 V^{-1} s^{-1})	Ref.
Metal-induced	IGZO	SPT	16/8	—	5.2×10^{-4}	16.1	53
	IGZO	SPT	2.4/0.8	2.7	—	8.5	54
Doping	IGZO	SPT	3/5	10.2	—	17.2	55
	IGZO	SPT	—	—	1.3×10^{-6}	—	56
	ZnO	ALD	15/2	0.3	—	39.2	57
	IGZTO	SPT	10/10	11.3	—	27.2	58
OS engineering	In_2O_3	ALD	—/0.04	0.002	1.3×10^{-9}	—	59
	IGZO	ALD	24/24	1.8	—	36.9	60
n^+ layer	IGZO	SPT	300/500	510.0	—	12.0	61
	IGZO	ALD	60/30	0.1	4.2×10^{-7}	45.3	62
DB layer	IGZO	SPT	625/95	18.0	—	11.5	63
	IGZO	SPT	1000/150	104.5	—	14.8	64

W/L: width and length of the channel; ρ_C: specific contact resistivity.

reduction of In according to the reaction: $2Al + In_2O_3 \rightarrow Al_2O_3 + 2In$ (Gibbs free energy (ΔG) = −752.6 kJ mol^{-1}). The resulting *I–V* characteristics of the Al-treated TFTs showed enhanced drain current in the on-state region, without current crowding at low V_D, indicating good ohmic contact with a low $R_C W$ of 10 Ω cm, while the untreated TFTs exhibited significantly suppressed drain current (Fig. 5(a)).

However, the strong reducing power of Al can lead to excessive conductivity in the channel region, potentially degrading the transfer characteristics.[66] Park *et al.* suggested that Ni electrodes would be more suitable S/D electrodes for high-density applications, where precise contact properties are crucial.[53] Thermally deposited Ni and Al electrodes were compared in terms of contact performance (Fig. 5(b) images shown top). Technology computer-aid design simulations showed that the Ni electrodes exhibited superior electrical properties compared to the Al electrodes, which was attributed to two factors: (1) a reduced generation and diffusion of V_O^+, which acts as a shallow donor, and (2) a lower metal intermixing at the M–S junctions in Ni-based devices (Fig. 5(b) images shown below).

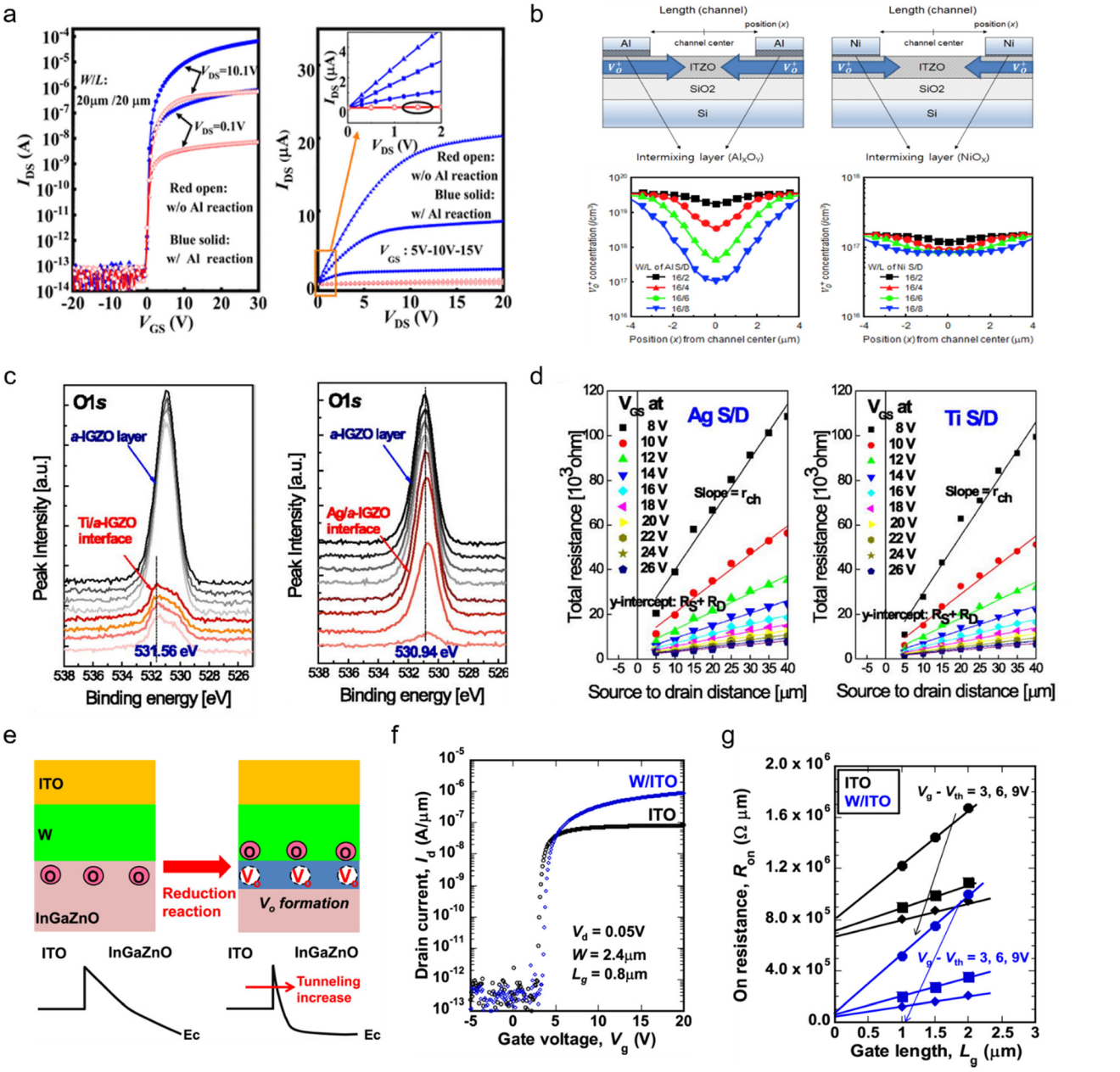

Fig. 5 (a) The *I–V* characteristics with and without an Al reaction. (b) Schematic illustration comparing the diffusion extent of V_O^+ when using Al and Ni electrodes (top images), along with a simulation of V_O^+ concentration in the ITZO layer (bottom images). (c) O1s XPS analysis from Ti/a-IGZO and Ag/a-IGZO interfaces from the TFT devices. (d) R_T plotted with respect to a-IGZO TFT channel length for different V_G with Ag and Ti electrodes. (e) Schematic illustration of the interfacial reaction between W and IGZO. (f) I_D–V_G characteristics of IGZO TFTs using ITO and W/ITO. (g) On resistance of IGZO TFTs using ITO and W/ITO.

Ti-induced method. Ti, known for its strong reducing power, can generate V_O and form TiO_2 at the interface with indium-based channels.[67] In a study by Choi *et al.*, using Ti as S/D electrodes in a-IGZO TFTs significantly lowered the resistance compared to Ag S/D electrodes.[68] Analysis with XPS revealed the formation of a TiO_x layer and V_O at the Ti/a-IGZO interface, facilitated by the lower formation enthalpy of TiO_x compared to that of In_2O_3, Ga_2O_3, and ZnO (Fig. 5(c)). In contrast, no V_O generation was observed at the Ag/a-IGZO interface, resulting in higher R_C. Consequently, the specific contact resistivity (ρ_C) of the Ti electrode was approximately one-third that of the Ag electrodes (Fig. 5(d)). However, the use of Ti electrodes can lead to V_O^+ formation and metal diffusion after thermal treatment, potentially reducing the effective channel length. This limits Ti's suitability for applications requiring aggressive scaling. Thus, Ti is often used in its metal–nitride form or combined with other materials.[69]

W-induced method. To mitigate the effective channel length shortening caused by V_O and metal diffusion during high temperature annealing, Kataoka *et al.* explored the use of indium tin oxide (ITO), which exhibits lower reactivity with IGZO.[54] However, the use of ITO alone resulted in a lower on-current compared to Ti electrodes due to a higher R_C. To address this, a 2 nm thick W layer was introduced to form a W/ITO electrode. XPS depth profile analysis revealed W–O bonds at the W/IGZO interface, indicating the formation of WO_3, which was absent in the W/ITO interface. Additionally, Ga 2p spectra indicated a reduction reaction between W and IGZO, leading to V_O formation and thinning of the depletion layer, thereby increasing the tunneling current (Fig. 5(e) and (f)). The R_CW values of the ITO and W/ITO were measured to be 1.8×10^5 and 2.7×10^4 Ω μm, respectively, with the W/ITO electrode exhibiting the lowest R_C (Fig. 5(g)). Other studies have also investigated the use of metals with strong reducing power to form an n^+ region at the OS interface while minimizing channel shortening.[70,71]

3.1.2. Doping. Another effective strategy for enhancing the contact properties of OS TFTs involves inducing an n^+ region through doping techniques applied between the channel and S/D. This can be achieved with ion implantation or plasma treatment.

Ion implantation. Several studies have explored the formation of n^+ regions using B ion implantation.[72,73] Kang *et al.* investigated the effect of varying implantation energy during B^+ ion implantation on the R_C of self-aligned coplanar a-IGZO TFTs (Fig. 6(a)).[55] B acts as an n-type dopant in metal oxide TFTs and is also well known for its stability at high temperature, due to the strong B–O bond. Ion implantation was performed at 30, 35, and 40 keV to compare the effects of implantation energy on device characteristics (Fig. 6(b)). With increasing implantation energy, device mobility improved and the R_cW decreased. However, the lateral spread (ΔL) of the

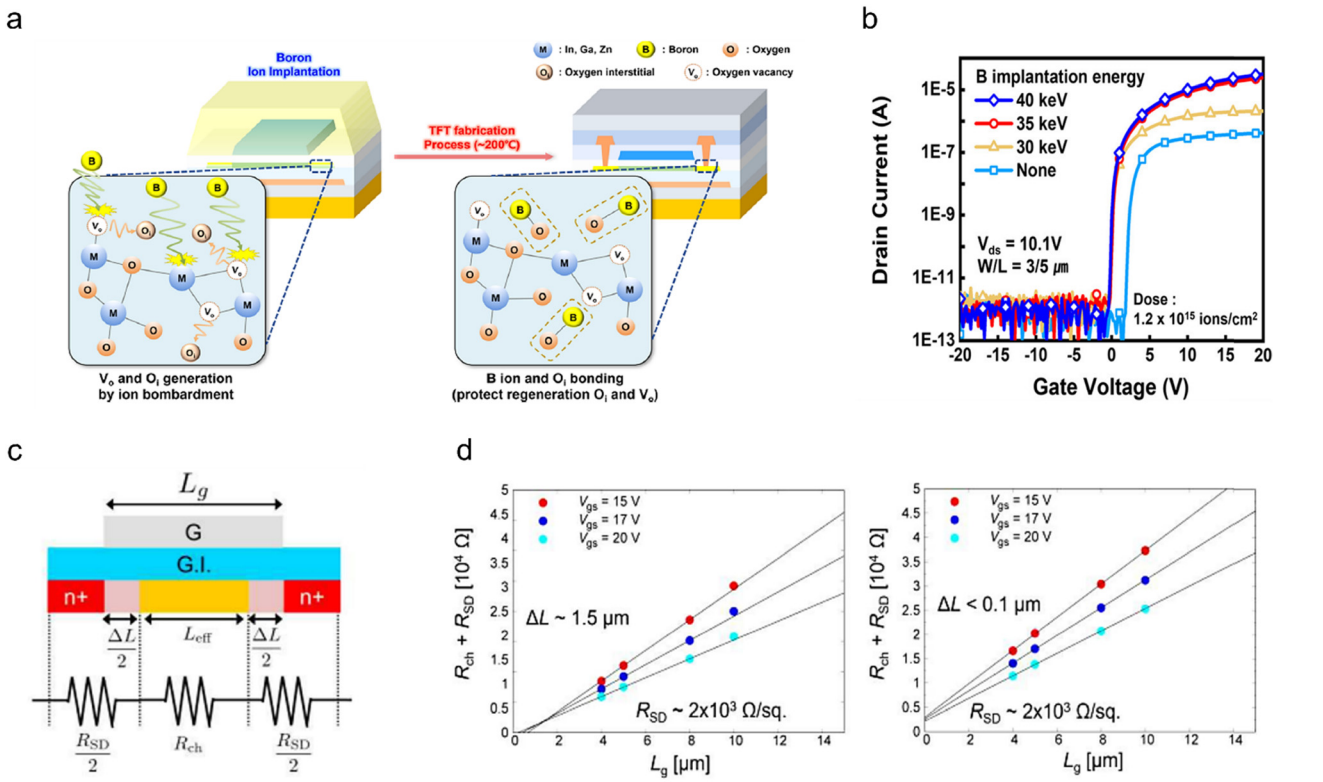

Fig. 6 (a) Schematic illustration of the reaction of B ions implanted in the IGZO surface. (b) The *I*–*V* characteristics at different B implantation energies. (c) Illustration of S/D series resistance R_{ch} + R_{SD} at the gate edges in TFTs. (d) Measurements of the S/D series resistances in Ne^+ (left) or B^+ (right) implanted TFTs as a function of gate length (L_g) for V_G of 15, 17, and 20 V.

implanted ions increased, likely due to enhanced B ion diffusion at higher energies. The ΔG of B_2O_3 ($-1{,}192.9$ kJ mol^{-1}) was significantly lower than that of In_2O_3 (-830.7 kJ mol^{-1}), Ga_2O_3 (-998.3 kJ mol^{-1}), and ZnO (-348.1 kJ mol^{-1}), which facilitated the formation of stable B–O bonds. This stability, in conjunction with oxygen interstitials, led to the creation of V_O sites during ion bombardment, ultimately increasing the carrier concentration (n_e).

Moreover, Ui *et al.* compared the effects of Ne^+ and B^+ ion implantation in a-IGZO TFTs.[74] Although Ne^+ ions are larger, they exhibited greater diffusion within a-IGZO during annealing, resulting in a smaller ΔL for B^+ implantation (Fig. 6(c) and (d)). This behavior was attributed to the stronger B–O bonding, which restricted diffusion. These findings underscore the importance of considering ion size, bonding energy, and implantation energy when optimizing ion implantation for contact region doping. Other ions, such as F and N, have also been investigated for similar doping applications.[75–77]

Plasma treatment. Plasma treatment, particularly using H and Ar plasma, has been extensively studied as an effective method for lowering the R_C in OS TFTs.[78–84] In an investigation by Park *et al.*, H plasma treatment with a variety of conditions was analyzed using TLM extraction to assess its impact on R_C (Fig. 7(a)).[56] The findings indicated that H treatment reduces the potential barrier width by increasing n_e, although weak M–OH bonds are partially diffused during the process. It was observed that R_C varied with plasma power and temperature, as shown in Fig. 8(b). The study emphasized that optimizing plasma power and process temperature is critical. Higher RF power introduces excessive H into a-IGZO, forming unstable bonds that lead to device instability. Proper thermal processing can mitigate this instability. Ahmad *et al.* investigated the relationship between ρ_C, hydrogen doping, and diffusion at the channel-S/D interface, noting changes in work function with increasing hydrogen plasma treatment time (Fig. 7(b)).[85] However, the high diffusivity and reactivity of H imposed limitations on process temperature and conditions.[86] Consequently, alternative approaches focused on inert gases, such as Ar and Ne, for plasma treatments.

In the work by Lu *et al.*, Ar plasma treatment was shown to affect contact properties, with prolonged treatment time promoting V_O formation, thereby reducing the barrier width, enhancing tunneling, and subsequently decreasing R_C (Fig. 7(c)).[57] This impact was significant in short-channel devices. For example, Zhang *et al.* demonstrated effective R_C reduction in a 302 nm self-aligned bottom-gate a-IGZO TFT, and attributed the improvement to increased V_O and carrier density (Fig. 7(d)).[87] The improved *I–V* transfer characteristics showed enhanced on-current and notable reliability, indicating that Ar plasma treatment is a promising technique for nanoscale AOS technologies, including micro-displays, flexible integrated circuits, and advanced optoelectronic applications.

Due to the relatively large mass of Ar ions, which can etch OS films, treatment with a nitrogen (N) plasma has also been investigated as a lower impact alternative.[58] The N plasma treatment has resulted in reduced R_CW and ΔL compared to an Ar plasma, which could be attributed to N's smaller ion mass and reduced collateral effects (Fig. 7(e) and (f)). Additionally, F plasma treatment has been explored as a technique to reduce R_C.[88,89] F ions, due to their similar ion radius to O, effectively passivate V_O sites (Fig. 7(g)). The robust metal–F bonds exhibit higher bond energy than metal–O bonds, maintaining enhanced stability even after annealing at 600 °C. Furthermore, the influence of a mixture of gases, such as $CF_4 + O_2$ or $Ar + O_2$, on R_C has also been investigated, providing additional feasibility for the use of plasma treatments to optimize device performance.[90–92]

3.1.3. Oxide semiconductor engineering. The electrical characteristics of AOS, including carrier density and E_G, which directly influences electrical contact properties, are notably dependent on the relative composition ratio of metal cations and oxygen. Several studies have examined the impact of varying cation composition ratios in OS TFTs to optimize performance and reduce R_C.[93,94] Lee *et al.* have demonstrated a strong correlation between In content and contact resistant, showing that increased In ratios result in a reduced E_G, higher electron affinity, and elevated work function. These factors contribute to a >40% reduction in the barrier height between the channel and S/D electrodes.[95] Consequently, R_CW significantly decreases from 13.5 to 1.8 Ω cm (Fig. 8(a) and (b)).

In a complementary study, Saito *et al.* found that IZO exhibited superior mobility and lower R_C than IGZO TFTs.[59] A measurement of Φ_B based on a TE model indicated an Φ_B of 0.46 eV for IGZO and 0.37 eV for IZO, highlighting a lower barrier in IZO. Moreover, Fowler–Nordheim tunneling current models revealed a 0.13 eV larger band offset at the IZO/SiO_2 interface compared to IGZO, consistent with the Φ_B difference (Fig. 8(c)). These findings underscored the critical role of metal composition in modulating Φ_B and R_C, with IZO TFTs showing approximately 75% lower S/D resistance compared to IGZO TFTs (Fig. 8(d)).

Channel thickness also influences carrier density, which in turn affects R_C. Niu *et al.* have observed that increasing carrier density in In_2O_3 results in ρ_C (Fig. 8(e)), and have proposed an optimal channel thickness for achieving target carrier density essential for next-generation, high-performance ultra-scaled back end of the line electronics.[60] However, while higher carrier density can decrease R_C, it may shift the material's behavior toward metallicity, necessitating careful optimization to balance a low R_C with semiconducting properties (Fig. 8(f)).[96]

As channel dimensions scale downward, thermal electron injection over the SB can lead to a significant increase in R_C. Recent research has therefore focused on optimizing channel thickness to modulate carrier density and exploring structural modifications to improve contact properties, with the ultimate goal of developing TFTs that combine high on-current and stable V_T.[97,98]

3.2. Interlayer insertion

3.2.1. n^+ layer. Doping techniques have been widely studied to improve contact properties (refer to Section 3.1). However, the OS interface near the S/D electrodes remains

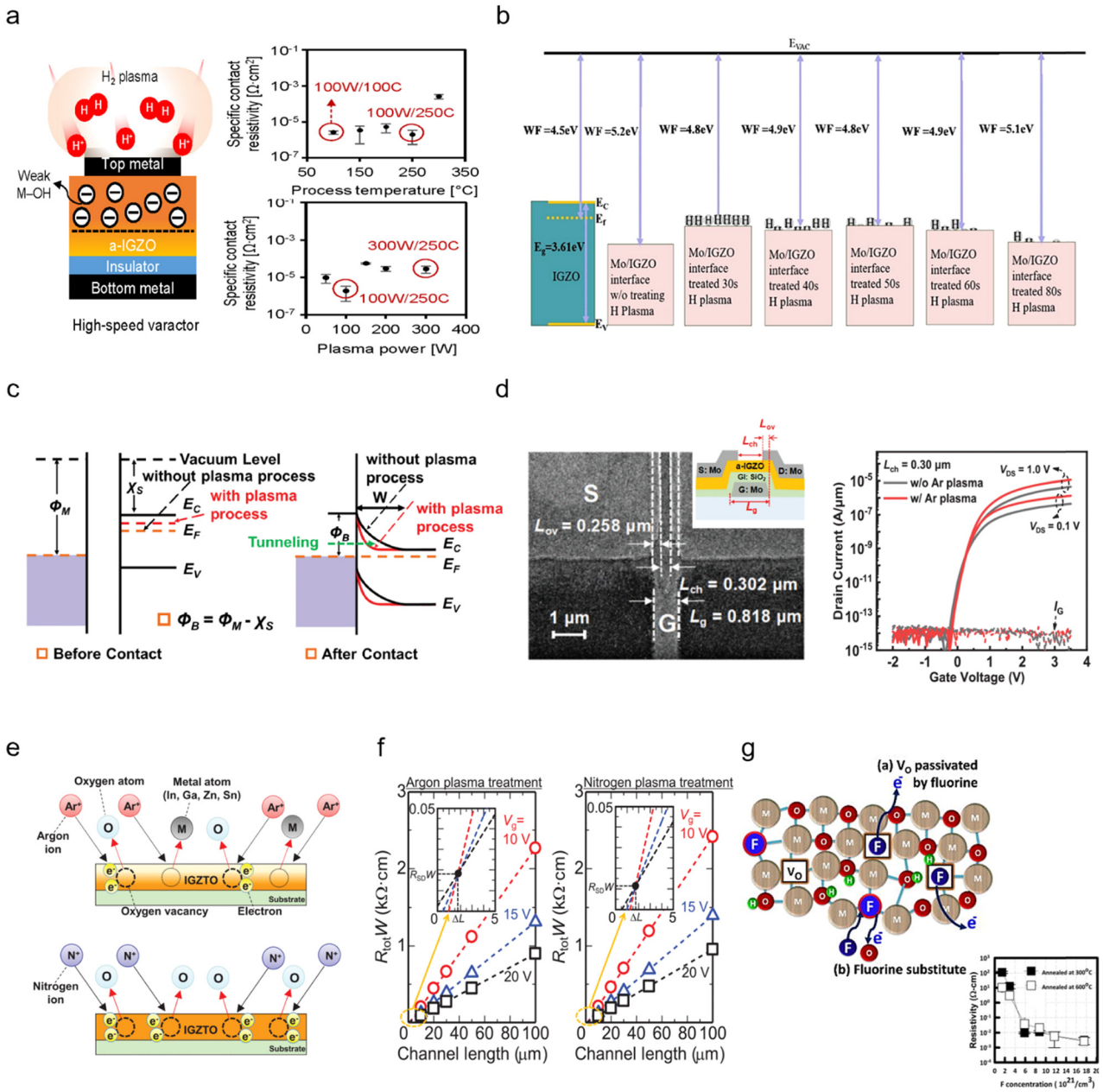

Fig. 7 (a) Schematic illustration of hydrogen plasma treatment on TFTs (left) and ρ_C as a function of process temperature and plasma power. (b) The schematic energy diagram of the work function at the Mo/IGZO interface. (c) The energy band diagrams of a Ti electrode and an OS layer, before (left) and after (right) contact. The effective potential barrier width is reduced with an Ar plasma process. (d) Top-down and cross-section SEM images of TFT (left) and the transfer characteristics of TFTs with and without Ar plasma treatment. (e) The illustration of the different mechanisms of Ar^+ and N^+ plasma treatments. (f) Width-normalized R_T as a function L for TFTs fabricated with Ar (left) and N (right) plasma treatment. (g) Model of F doping showing V_O passivated by F or F substitution for O. When F concentration increases, resistivity decreases.

vulnerable to degradation, leading to an increase in interface defects that can offset the advantages of higher carrier concentration (n_e). To address this challenge, the insertion of an n^+ layer, with a higher n_e than the OS channel, has been explored as an effective approach to reduce the barrier width while minimizing interface damage.[61,62,99–103]

Homogeneous layer. The n_e in sputter-derived OS layers can be modulated by controlling the oxygen partial pressure (P_{O_2}), power, and cation composition during the deposition process. Kim *et al.* investigated the modulation of the contact barrier in a-IGZO TFTs by varying the P_{O_2} in a homogenous IL, as shown in Fig. 9(a).[61] The deposition ratio of $O_2/(O_2 + Ar)$ was adjusted to 1% (type 1), 0% (type 2), and 20% (type 3) for the sputtered a-IGZO IL, using the same target as the channel layer. The type 2 device exhibited an improved μ_{FE} of 12.03 $cm^2\ V^{-1}\ s^{-1}$, a negative V_T shift of −4.1 V, and a 2.3-fold reduction in $R_C W$ compared to the type 1 device, which had a μ_{FE} of 9.95 $cm^2\ V^{-1}\ s^{-1}$, a V_T of

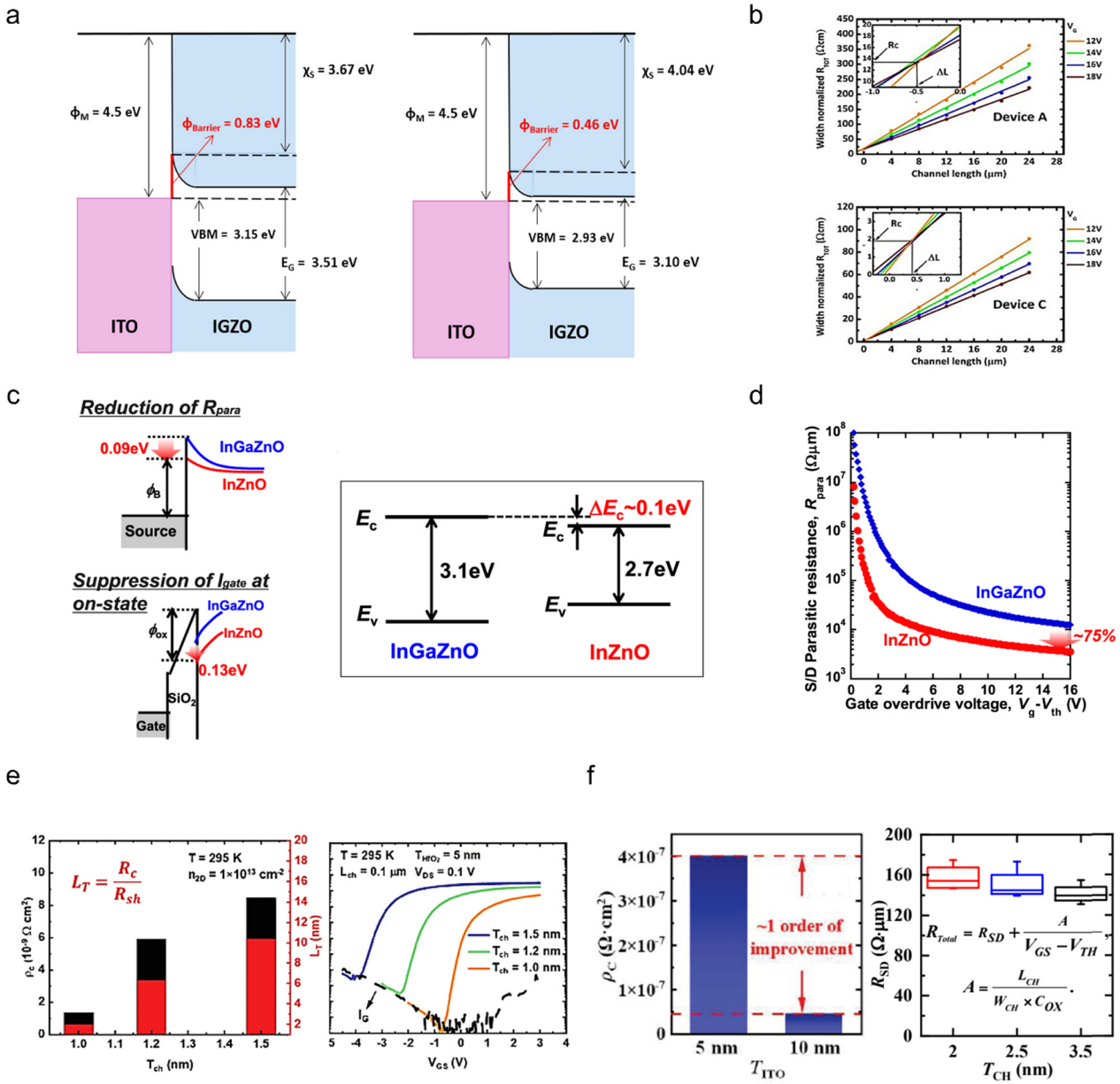

Fig. 8 (a) Schematic of the energy band diagram for contact structures of ITO and IGZO with low In concentration (left) and high In concentration (right). (b) Linear fit obtained from the TLM analysis for low In concentration (device A) and high In concentration (device B). (c) Schematic of the band diagram of IGZO and IZO. (d) Comparison of S/D R_C between IZO FETs and IGZO FETs. (e) Channel thickness dependence of ρ_C and current transfer length (left), and transfer characteristics for different channel thicknesses (right). (f) ρ_C with channel thicknesses (T_{ITO}) of 5 and 10 nm (left) and R_{SD} for different T_{ITO} (right).

5.8 V, and an R_CW of 575 Ω cm (Fig. 9(c) and (d)). The increase in P_{O2} from 0% to 1% and 20% resulted in a significant reduction in V_O from 39.1% to 21.9% and 12.6%, respectively, driven by the reaction $1/2O_2 + V_O^{2+} + 2e^- \rightarrow O_O$ (Fig. 9(b)). Consequently, the higher n_e observed in the type 2 IGZO IL can be attributed to the presence of intrinsic V_O defects, which act as donors and effectively form a highly doped layer, thereby enhancing ohmic contact properties.

Heterogeneous layer. Many studies have focused on identifying the optimal conditions for IL to achieve superior electrical contact properties. Recently, Jeong *et al.* proposed a multi-stack IL structure composed of an oxygen-scavenging TiN layer and an n^+ IGTO layer, highlighting the thickness dependence of the IGTO layer (t_{IGTO}) on the R_C of a-IGZO devices.[103] IGZO TFTs with a TiN/IGTO (3/8 nm) IL had the lowest R_CW of 0.7 Ω cm, which was significantly lower than the control device, which had an R_CW of 6.9 Ω cm. The observed performance degradation when $t_{IGTO} > 8$ nm, as shown in Fig. 6(e), was attributed to changes in crystallinity. Despite the high n_e in 12 nm thick IGTO (Fig. 9(f)), crystallization-induced deterioration at the M–S interface caused an increase in R_CW to 1.3 Ω cm.

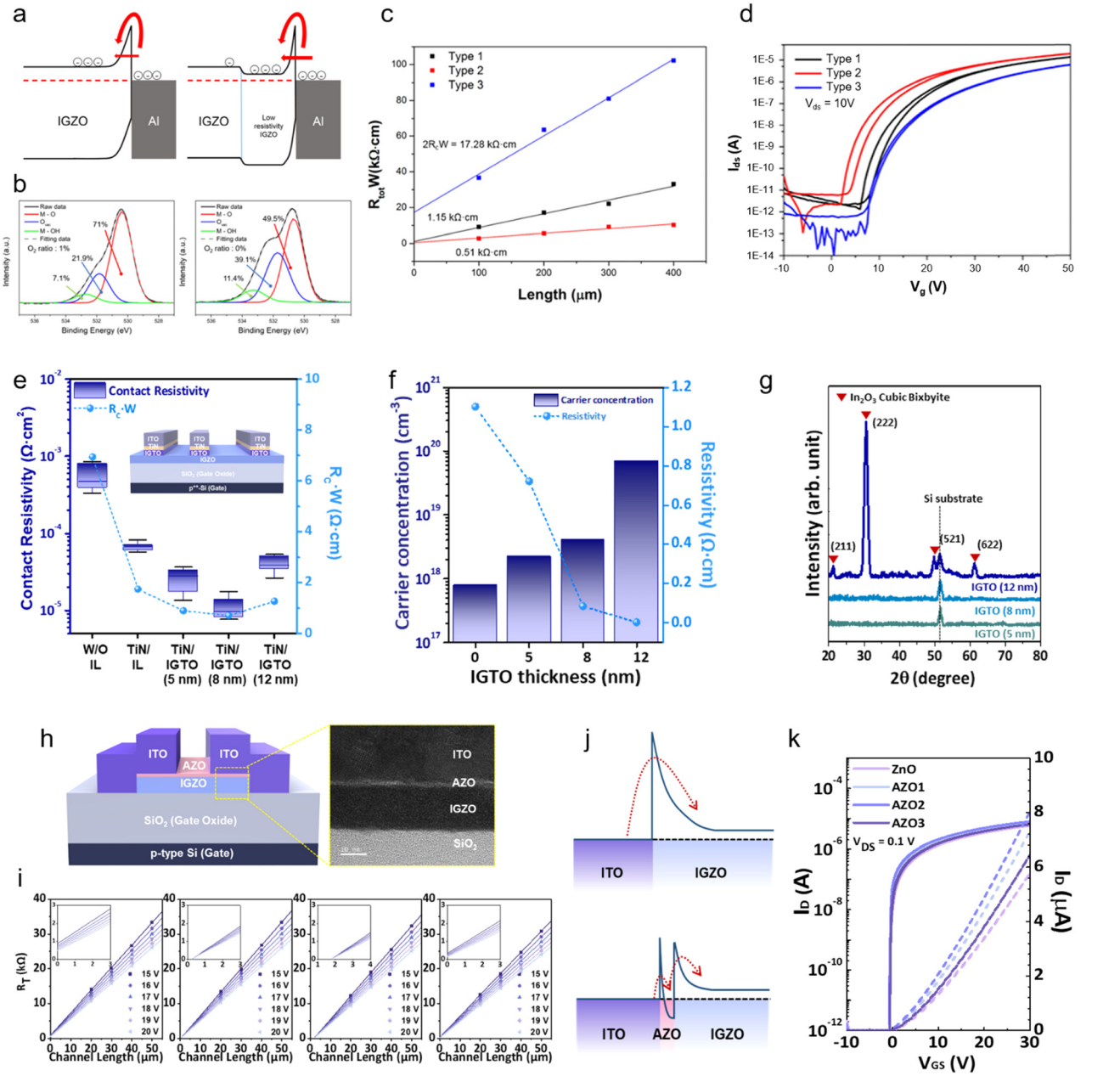

Fig. 9 (a) Energy band alignment of the contact region for a-IGZO TFTs without an interlayer (IL) and with a low resistivity IL. (b) O 1s XPS spectra of IGZO thin films with oxygen ratios of 0% and 1% during deposition. (c) R_TW as a function of L for three device types: type 1 without an IL; type 2 with an n^+-IGZO IL; type 3 with an n^--IGZO IL. (d) Transfer characteristics of the three a-IGZO TFT types. (e) Contact scheme-dependent ρ_C and R_CW in a-IGZO TFTs with different ILs. (f) Hall effect measurements of the IGTO/IGZO thin-film stacks with IGTO thickness (t_{IGTO}) values of 0, 5, 8, and 12 nm. (g) GIXRD pattern of the IGTO thin films with varying t_{IGTO}. (h) Device schematic of the proposed a-IGZO TFT structure with a cross-sectional HRTEM image. (i) R_T–L plots as a function of V_G in a-IGZO TLM devices with different ILs. (j) Schematic energy band diagrams at the contact region. (k) Transfer characteristics at V_D of 0.1 V with different ILs.

Additionally, Jeong *et al.* reported on an ALD-based ultrathin IL method (Fig. 9(h)).[62] The optimized doping ratio of an Al-doped ZnO IL was achieved by adjusting the number of Al_2O_3 injection cycles during the ALD process, resulting in the lowest R_CW of 0.13 Ω cm at an Al_2O_3 : ZnO ratio of 2 : 8 (Fig. 9(i)). This substantial improvement was corroborated by a schematic energy band diagram, based on UPS and ellipsometry analysis, which indicated a reduction in Φ_B due to the IL's high n_e. This enhanced electrical contact contributed to an increase in μ_{FE} from 38.8 to 45.3 $cm^2\ V^{-1}\ s^{-1}$, as shown in Fig. 9(k).

3.2.2. Diffusion barrier layer. Inserting a diffusion barrier (DB) layer is another effective method to enhance the contact properties of OS devices, because it prevents adverse metal atom interdiffusion into the OS channel during the thermal annealing, which can otherwise lead to instability and device performance degradation.[63,64,104] The choice of DB material

depends on factors such as reactivity, adhesion, anti-diffusion properties, and low R_C. For example, Jeong *et al.* used a 5 nm thick Ca-doped CuO ($CuCaO_x$) DB IL positioned between a Ca-doped Cu (CuCa) electrode and an a-IGZO channel.[104] This configuration exhibited significant improvements in electrical properties, with a μ_{FE} of 20.7 $cm^2\ V^{-1}\ s^{-1}$, an SS of 0.4 V $decade^{-1}$, and a R_CW of 25.8 Ω cm, in contrast to the control device with Cu S/D electrodes, which had corresponding values of 3.5 $cm^2\ V^{-1}\ s^{-1}$, 1.51 V $decade^{-1}$, and 175 Ω cm (Fig. 10(a)). This enhancement was attributed to the effective suppression of Cu diffusion toward the channel layer by the $CuCaO_x$ IL and the formation of an extremely smooth interface (Fig. 10(b) and (c)). An in-depth study on MoTi DB was also conducted to determine why the Cu/MoTi stack exhibited superior performance compared to individual materials such as Mo or Ti alone.[64] The MoTi alloy leveraged the advantageous properties of both elements: Mo provided an excellent DB against Cu migration, while Ti acted as an oxygen scavenger, facilitating the formation of low-ohmic contacts (Fig. 10(d)–(f)). The device incorporating a 5 nm thick MoTi IL exhibited superior electrical characteristics, including a significantly lower R_C, compared to devices without an IL or those using individual Mo and Ti ILs. The synergistic effect of Mo and Ti was crucial in achieving this improvement.

4. Suggestion

As the semiconductor industry progresses toward higher integration for PPAC, reducing device dimensions has become essential. This has spurred interest in short-channel and 3D structures such as VCTs, gate-all-around (GAA), and channel-all around (CAA) designs. However, research aimed at minimizing ΔL to mitigate SCEs while suppressing performance degradation caused by R_C remains relatively limited. To enable the application of OS in 3D architectures, further investigations into R_C reduction strategies and geometrical effects on R_C are imperative. Contact geometry plays a pivotal role in influencing local current density through variations in the electric field. While electric field concentration near edge contact can enhance charge transport and reduce R_C, it can also cause localized temperature rises along the current paths, resulting in increased R_C.[105,106] Therefore, optimizing contact geometry to manage field concentration is essential for improving device performance. In this context, studies have explored strategies to mitigate current crowding effects on R_C by modulating contract area and channel edge design. For instance, in transition-metal dichalcogenides (TMDs), minimized contact areas are often employed, whereas OSs have been investigated with an emphasis on increasing contact areas.[107–111] Specifically, integrating OS into DRAM architectures

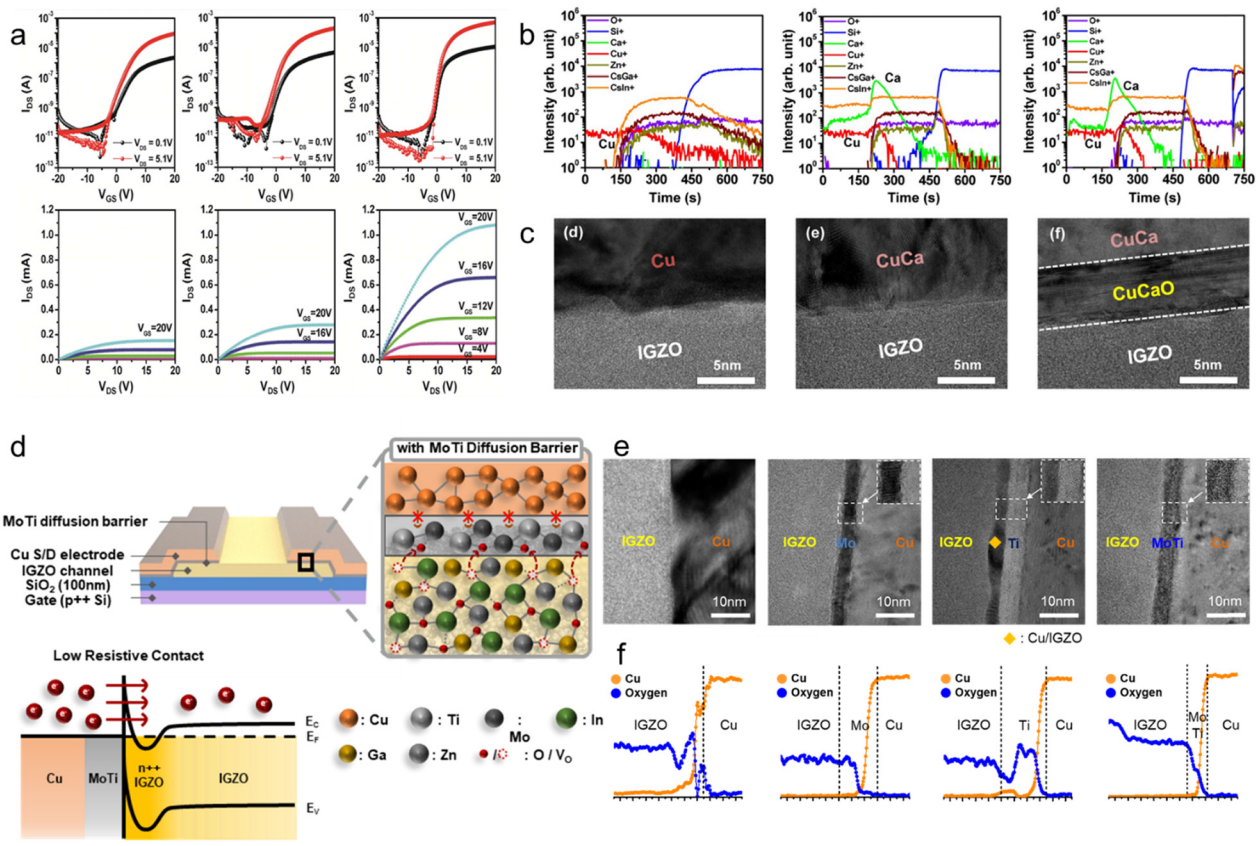

Fig. 10 (a) Transfer and output characteristics of a-IGZO TFTs with different S/D electrodes: Cu, CuCa, and CuCa/$CuCaO_x$. (b) Elemental depth profiling results for the a-IGZO devices with different S/D electrodes. (c) Cross-sectional TEM images of the channel and electrode stacks. (d) Concept of the synergistic effect in Cu/MoTi/IGZO stacks, combining diffusion blocking against Cu migration and forming a good n^+ layer. (e) Cross-sectional TEM images of Cu/IGZO, Cu/Mo/IGZO, Cu/Ti/IGZO, and Cu/MoTi/IGZO stacks. (f) Elemental depth profiles from EDS analysis of Cu and O for different stacks.

with nanometer-scale contact holes ($\sim 1 \times 10^{-12}$ cm^2) requires achieving a specific contact resistivity ($\rho_C = R_C \cdot A_C$) below 10^{-6} Ω cm^2 to avoid performance degradation and ensure reliable device operation. Meeting this target necessitates further research into scaling-friendly contact engineering approaches tailored to ultra-scaled and 3D device architectures.

5. Conclusion

OSs are emerging as promising candidates for next-generation channel materials, with the potential to address the scaling limitations inherent in conventional silicon-based devices. This review focuses on key strategies for reducing R_C in OS-based TFTs, which remains a critical challenge for further miniaturization and performance enhancement. While various methods – such as conductive region formation and interlayer insertion – have been explored to reduce R_C in OS TFTs, the majority of studies have focused on devices with relatively long channel length (>1 μm). The effectiveness of these strategies for sub-micrometer or even sub-100-nanometer channel lengths is highly dependent on the fabrication process, structure, and thermal budget. This remains an open question and warrants further investigation. In particular, the formation of an n^+ conduction region and interlayer insertion have demonstrated effectiveness in lowering the effective potential barrier between metal and semiconductor and enhancing carrier injection. As OS technologies advance into more sophisticated applications, such as DRAM, reducing R_C will be vital to meet the performance demands of future semiconductor devices. Continued innovation in contact engineering will be vital for unlocking the full potential of OSs in high-performance, scalable electronics, paving the way for their integration into future device architectures.

Data availability

The datasets used and/or analyzed during the current study are available from the corresponding author on reasonable request.

Conflicts of interest

There are no conflicts to declare.

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