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2D semiconductor SnP_2S_6 as a new dielectric material for 2D electronics†

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Due to the intriguing optical and electronic properties, 2D materials are promising for next generation optoelectronic and electric device applications. Exploring new 2D materials with novel physical properties is rewarding for this area. In this work, we systematically investigated the optoelectronic properties of 2D metal thiophosphate SnP_2S_6 with a unique nanoporous structure. The intermediate band-gap makes SnP_2S_6 a good candidate for both the channel and gate dielectric materials in the transistor device. SnP_2S_6 showed good photoresponse properties. In addition, the MoS_2 transistor with SnP_2S_6 as a dielectric layer showed a high dielectric constant (≈23) and a low subthreshold slope down to 69.4 mV dec^{-1}, and it presented 0.1 pA scale leakage current, a threshold voltage as low as 1.1 V, an ON/OFF ratio reaching 10^7 and negligible hysteresis with high stability and reproducibility. This work could open up new avenues for the discovery of new metal thiophosphate systems for future device applications.

Introduction

The emergence of two-dimensional materials has brought new opportunities to the scientific and industrial fields. The quantum confinement effect in the thickness direction of two-dimensional materials is prominent, demonstrating the advantages of high carrier mobility, channel regulation capability and rich properties in force, heat, sound, light, electricity and magnetism.[1–4] As a result, novel electronic and optoelectronic devices based on 2D materials are developed and studied, and this is still an active research field today.[5–7] The rapid development of 2D materials is beneficial for the discovery of novel 2D materials with exotic physical properties. For example, the discovery of 2D $CuInP_2S_6$ brings 2D ferroelectricity and the related device application to the center of the ferroelectric transistor and memory device field. The isolation of layered CrI_3 enables truly 2D ferromagnetic properties, attracting a lot of attention in the study of 2D magnetism. Layered ternary compounds such as Ta_2PdS_6,[8] $In_2P_3S_9$,[9] and Bi_2O_2Se[10,11] also provide new opportunities for the electronic and optoelectronic performance improvement for 2D material applications. There exist huge potential, opportunities and challenges for exploring new 2D material systems for application in future nanoelectronics and optoelectronics.[12,13]

For dielectric applications, SiO_2 is used as a dielectric layer typically, but traditional silicon-based field effect transistors (FETs) face various challenges when the device scales down to nanometer regime, the most prominent ones of which are reduced mobility and increased short-channel effects.[14] In order to mitigate these problems, novel dielectrics with remarkable

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properties have begun to appear. Advanced functional materials based on eco-friendly cellulose and sputtered multicomponent dielectrics can be processed at low temperatures, and were reported to be implemented as high-capacitance gate dielectrics, bringing new insights into flexible and low-cost transistors and the need to meet the constraints for better band-offset matching.[15,16] Moreover, 2D insulators are regarded as the ultimate solution for dielectric miniaturization.[17] Hexagonal boron nitride (h-BN) has been deemed as the most promising 2D vdW dielectric layer, while novel 2D materials suitable for using as dielectric layers are rarely reported. However, the low dielectric constant ($\approx$5.0) and excessive leakage current make h-BN unsuitable for ultrascaled FETs with low power consumption.[18,19] Therefore, it is important to find new materials to serve as reliable gate dielectrics in FETs.

Among the various 2D material systems, the novel 2D metal thiophosphate MP_2X_6 (M = metal, X = S or Se)[20] has received much attention due to its exceptional physical properties, including magnetic, electronic, ferroelectric, and optical characteristics.[21–23] Among the most extensively studied systems is the $Sn_2P_2S_6$ crystal with a considerable piezo effect, appropriate ferroelectric and nonlinear optic properties,[24,25] MPS_3 as a UV photodetector[26] which possesses magnetic order,[27] and $CuInP_2S_6$ heterostructures for non-volatile ferroelectric switches, memory devices and field-effect transistors.[28,29] In addition, SnP_2S_6, a stable semiconductor material with a sizable indirect band gap of 2.23 eV,[30] is also of importance to be investigated as a member of this family. SnP_2S_6 exhibits a unique nonporous structure as it lacks half of the metal ions compared to the parent $Sn_2P_2S_6$ structure. Due to the intrinsic 2D nanoporous structure, these days have witnessed more theoretical research studies on SnP_2S_6,[24,30–32] despite the recent experimental study of a strong nonlinear optical response related to its inversion symmetry broken structure.[33,34] A recent theoretical study has predicted that SnP_2S_6 could have high carrier mobility,[20] good switching stability, excellent insulation performance and gate-control ability. The measured dielectric constant is higher than that of the extensively used h-BN substrate.[35] Thus, it demonstrates great potential to be used as a channel or dielectric layer material in field effect transistors.

In this work, SnP_2S_6 is proposed for the first time as a dielectric layer, the electronic and optoelectronic characteristics of which have been systematically investigated. Field effect transistors with excellent performance are successfully constructed, which verifies the feasibility of SnP_2S_6 as a dielectric layer material and provides new reliable building blocks for 2D materials based electronic devices.

Materials characterization

Layered SnP_2S_6 shows a rhombohedral layered structure (as shown in Fig. 1(a and b)), which belongs to the *R*3 space group (No. 146) with a rhombohedral symmetry,[30,36] and only contains one formula unit[20] of one metal cation Sn^{4+} and one anionic $[P_2S_6]^{4-}$. As depicted in Fig. 1(a and b), the ternary SnP_2S_6 has a van der Waals layered structure and the interlayer spacing is about 0.65 nm, as reported in the literature.[33] Raman spectra were recorded using a 532 nm laser under ambient conditions. As shown in Fig. 1(c), three distinct peaks

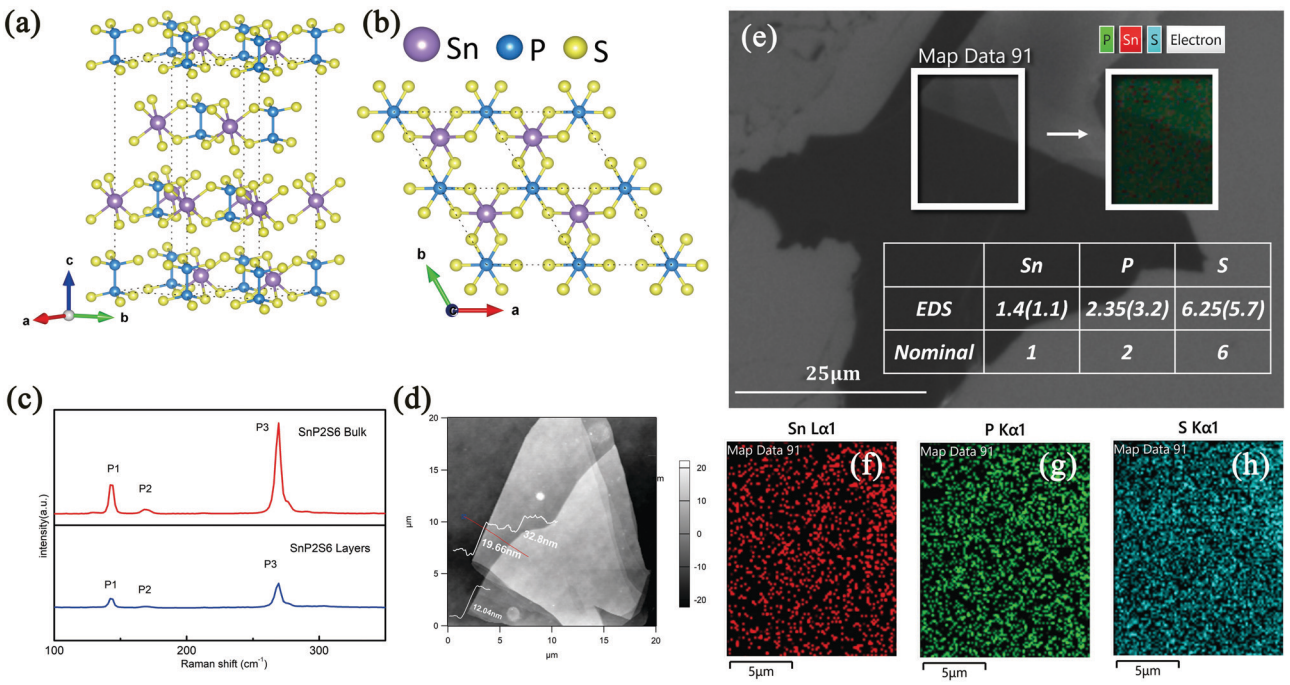

Fig. 1 Characterizations of the 2D material SnP_2S_6. (a and b) Crystal structure of layered SnP_2S_6. (a) Side and (b) top views. Purple, blue and yellow spheres represent Sn atoms, P atoms and S atoms, respectively. (c) Raman spectra of bulk and few-layer SnP_2S_6. (d) AFM topography of SnP_2S_6 of different thicknesses. The thicknesses are around 12.04, 19.66 and 32.80 nm, respectively. (e) EDS results and elemental mappings of Sn (f), P (g) and S (h) for a typical SnP_2S_6 crystal, which show a homogenous distribution of the three elements.

P_1(≈142 cm^{-1}), P_2(≈168 cm^{-1}) and P_3(≈269 cm^{-1}) can be identified in both bulk and layered SnP_2S_6. Specifically, the three peaks are related to the internal stretching vibrations of S–P–S bonds,[9] which are consistent with previous reports.[33,37] As the thickness increases, the intensity varies while the positions of all peaks hardly change, which might be due to the weak interlayer interaction. In addition, as shown in Fig. 1(e), it is noted that the atomic ratios of the SnP_2S_6 sample are 14 : 23.5 : 62.5 and 11 : 32 : 57 (total 100), which are close to the stoichiometric ratio of 1 : 2 : 6, and the uniform distribution of elements Sn, P, and S is shown in Fig. 1(f–h), as confirmed by energy dispersive X-ray spectroscopy characterization (details in Fig. S1, ESI†).

Optoelectronic properties of SnP_2S_6 thin flakes

The SnP_2S_6 phototransistor is fabricated on the standard SiO_2/Si substrate (see the Methods section for details), and the schematic illustration of the device is shown in Fig. 2(a). The transfer and output curves of the SnP_2S_6 based transistor are shown in Fig. 2(b and c). A linear relationship between I_{ds} and V_{ds} was observed. However, the transistor shows very low electron mobility, and the mobility ($\mu = Ld/W\varepsilon_0\varepsilon_r V_{ds} \times dI_{ds}/dV_{bg}$) under a drain bias of 2 V was calculated to be 2.17×10^{-5} cm^2 V^{-1} s^{-1}. The electronic performance of the device with various thicknesses of SnP_2S_6 was also studied (details in ESI† Fig. S2 and S3), demonstrating a similar insulating behaviour. The good insulating behaviour makes SnP_2S_6 suitable for using as a dielectric layer, as discussed in detail in the next section.

The I_{ds}–V_{ds} curves shown in Fig. 3(a) are linear and symmetric while sweeping bias voltages, indicating an ohmic contact. The device shows an increase of drain current by several orders of magnitude once the device is illuminated. The typical optical image of the devices is shown in the inset of Fig. 3(a) and in Fig. S2 (ESI†). Furthermore, the power dependent photocurrent is plotted using a log–log scale method in Fig. 3(b). As the incident light power increases from 0.1 to 50 mW, the photocurrent I_{ph} increases monotonically from 8.3×10^{-12} to 1.2×10^{-10} A with a bias of 5 V, indicating that the photocurrent is linearly proportional to the incident light power following I_{ph}–P^{β}. Moreover, as the bias voltage shifts from 0.1 to 5 V, the value of β increases from 0.23 to 0.44. The great loss of photocurrent represented by the non-unity exponent relationship and a low value of β suggests that the photocurrent is influenced by complex processes including the absorption of photons, generation of free carriers, recombination of the photogenerated free carriers, charge trapping by the defects and charge impurities in SnP_2S_6 flakes, scarcely lateral photoeffect[38] and the adsorbed molecules at the SnP_2S_6/SiO_2 interface.[39–41]

Meanwhile, the photoresponsivity R and photo-gain G at a drain voltage of V_{ds} = 5 V exhibit a strong dependence on the illumination power, as shown in Fig. 3(c). The photoresponsivity R is one of the most important features for a photodetector.[42] $R = I_{ph}/PS$, where P is the incident light power density and S is the effective illuminated area. As shown in Fig. 3(c), the photoresponsivity increases with the decrease of light power, which is possibly attributed to the less frequent carrier recombination and longer carrier lifetime under weaker illumination. This is consistent with the photoconductor-based photodetector previously reported.[8,43] Photogain (G) is another parameter to evaluate the performance of a phototransistor, which can be calculated using the formula: $G = (I_{ph}/q)/(PS/h\nu) = h\nu R/q$,[44] where I_{ph} is the photocurrent, q is the electron charge, h is Planck's constant, ν is the light frequency, and R is the responsivity. The value of G was estimated to reach up to 3.74 at a power of 0.1 mW.

The gate voltage dependent photoresponse of SnP_2S_6 is also investigated. The transfer curves under the light on and off conditions are shown in Fig. 3(d), where an incident illumination of 80 mW is applied. The curves show an increase of drain current by nearly two orders of magnitude once the device is illuminated, indicating that the photocurrent dominates in the entire operating range of the device. As can be seen from Fig. 3(d), the photocurrent shows an ambipolar behaviour with large gate-tunability.

In order to study the stability and photoresponse speed of the SnP_2S_6 photodetector, the time–current curves with 532 nm laser switching on and off were measured. For three different bias voltages (1 V, 1.5 V and 2 V), as shown in Fig. 3(e), the time dependent photocurrent varies periodically with regular illumination, suggesting a stable and reversible photoresponse. The response speed is evaluated according to a typical rise time/decay time, which is defined as the time span over which

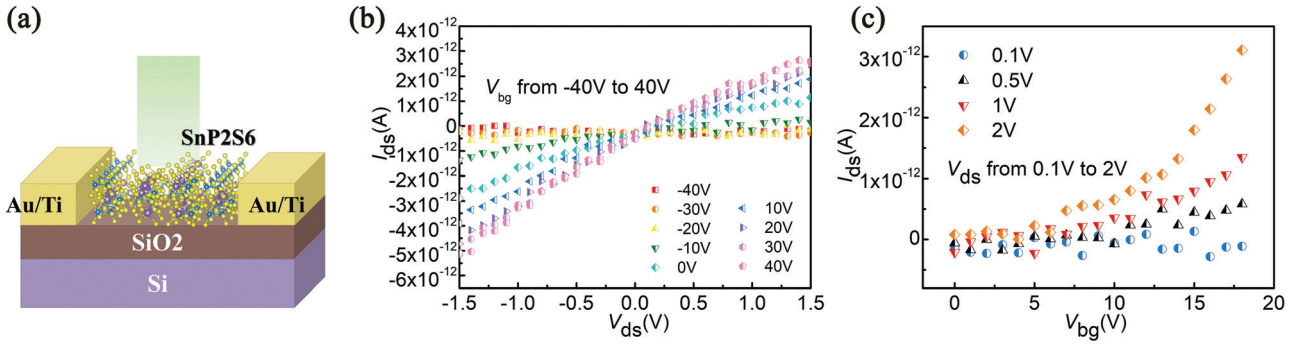

Fig. 2 Electronic properties of back-gated FETs using SnP_2S_6 as the channel. (a) Schematic of the SnP_2S_6 photodetector on the SiO_2/Si substrate, which provides the convenience of back gating. (b) Output curves (I_{ds}–V_{ds}) under various V_{bg} ranging from −40 V to 40 V. (c) I_{ds}–V_{bg} curves of SnP_2S_6 with different V_{ds} bias ranging from 0.1 V to 2 V.

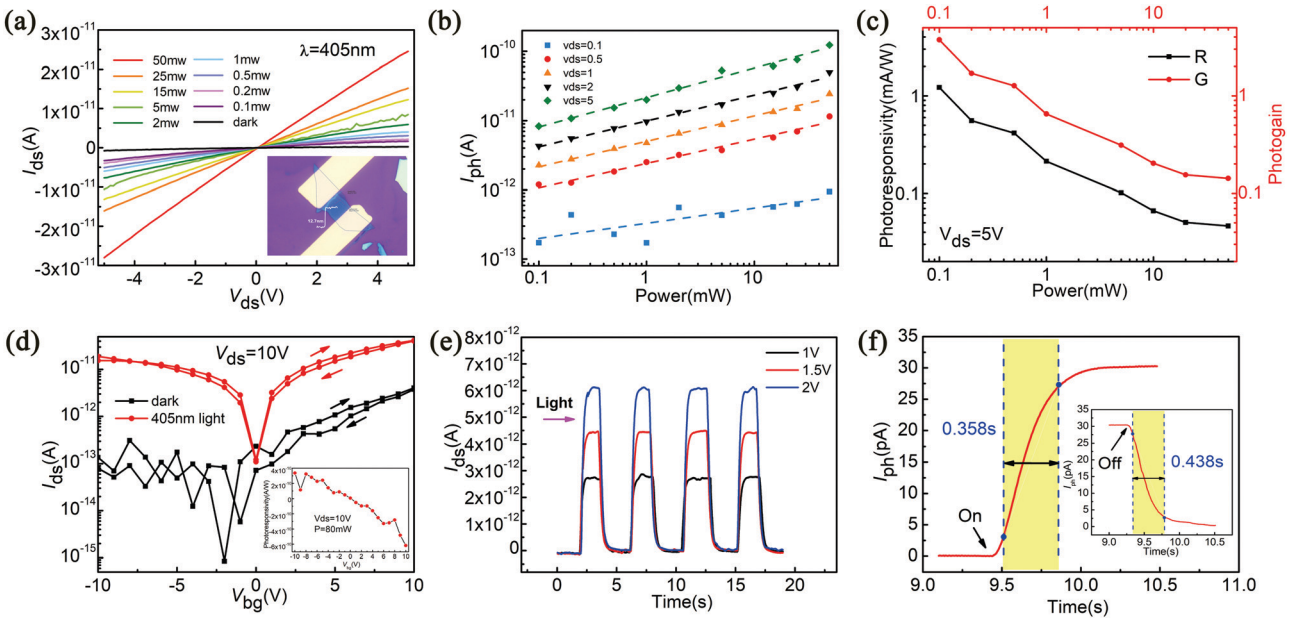

Fig. 3 Optical properties of the SnP_2S_6 photodetector. (a) I_{ds}–V_{ds} curves of SnP_2S_6 at different light powers. Inset: The optical image of the device with a thickness of 12.7 nm. (b) Photocurrent (I_{ph}) varies with light power and V_{ds}. (c) Photoresponsivity (R) and photogain (G) varying with light power. R_{max} = 1.22 mA W^{-1}, G_{max} = 3.74. (d) I_{ds}–V_{bg} curves in the dark and under 405 nm light. The dark current could be reduced to the pA regime. Under light conditions, the current hysteresis box becomes small. Inset: Photoresponsivity varies with V_{bg}, under V_{ds} = 10 V, P = 80 mW. (e) The ON/OFF test of photocurrent under 532 nm light and a bias from 1 V to 2 V. The ON–OFF ratio $>10^3$. (f) The exponential fitting of the dynamic response of photocurrent for the rise and decay time. The deduced rise (τ_{rise}) and decay (τ_{decay}) time constants are about 0.358 s and 0.438 s.

the photocurrent increases from 10% to 90% (or decreases from 90 to 10% analogously) when the laser is switched on and off. Fig. 3(f) shows the results of the rise and decay times of τ_{rise} = 0.358 s and τ_{decay} = 0.438 s for V_{ds} = 2 V, where the rising and falling parts of the curve can be fitted with an exponential function $I = I_0 + Ae^{t/\tau_{rise\ or\ decay}}$, where $\tau_{rise\ or\ decay}$ is the rise or decay time constant.

Dielectric properties of the SnP_2S_6 film

We first studied the temperature dependent dielectric permittivity at different frequencies. For this, bulk samples of SnP_2S_6 with a size of 5 × 5 × 0.05 mm^3 were obtained from the gas phase. Silver paste deposited on opposite planes of the test sample was used as the electrodes. The measurements were carried out at the frequency range of 10 Hz to 50 kHz and the temperature range of 80 to 400 K. Meanwhile, a GW INSTEK LCR-819 meter and an immersed liquid nitrogen cryostat with a temperature measurement accuracy of 0.001 K were adopted. The cooling rate was 0.1 K min^{-1} at a measuring field strength of 1 V cm^{-1}. As can be seen in Fig. 4(a and b), when the SnP_2S_6 crystals are cooled, a monotonic decrease trend in the permittivity (a) and dielectric losses (b) is observed. At high temperatures, low frequency ε' and ε'' increase strongly, which is most likely caused by an increase in the conductivity of the sample. The dielectric value of SnP_2S_6 ($\approx$23) is much higher than that of h-BN ($\approx$5.0), which is comparable with or higher than those of traditional high-k oxide dielectrics such as Al_2O_3,[45] HfO_2,[46] and ZrO_2.[47]

Considering that the SnP_2S_6 film has excellent insulating property, good chemical stability and a high dielectric constant,

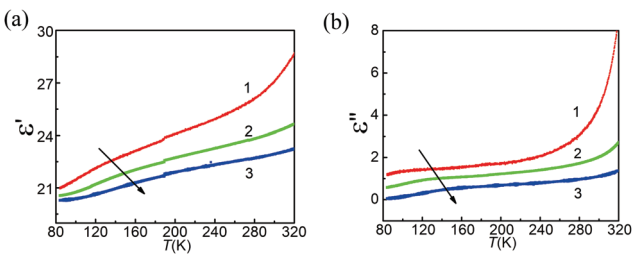

Fig. 4 Temperature dependence of the SnP_2S_6 crystal dielectric permittivity of the real (a) and imaginary (b) parts at frequencies 1(1 kHz), 2(10 kHz), and 3(40 kHz).

it shows great potential for integrating into 2D FETs as a dielectric layer to modulate the carrier density of semiconducting channel. To demonstrate its advantages in this regard, we fabricate 2D FETs and evaluate the gating effect of SnP_2S_6 as top-gate dielectrics.

The well-studied 2D semiconductor MoS_2 was chosen as a representative channel material. Initially, we build MoS_2/SnP_2S_6 FETs on SiO_2/Si substrate (the corresponding schematic is provided in ESI† Fig. S5A), but the result shows that the hysteresis window of the devices is too big (ESI† Fig. S5C). Here, in order to reduce the hysteresis window, we use h-BN as the substrate, which can be prepared with a very uniform thickness and an atomically flat surface,[48] and this method is proven to be effective in improving the performance of MoS_2 FETs.[49,50] The schematic illustration of our device is shown in Fig. 5(a) (optical image in ESI† Fig. S6 and S7D).

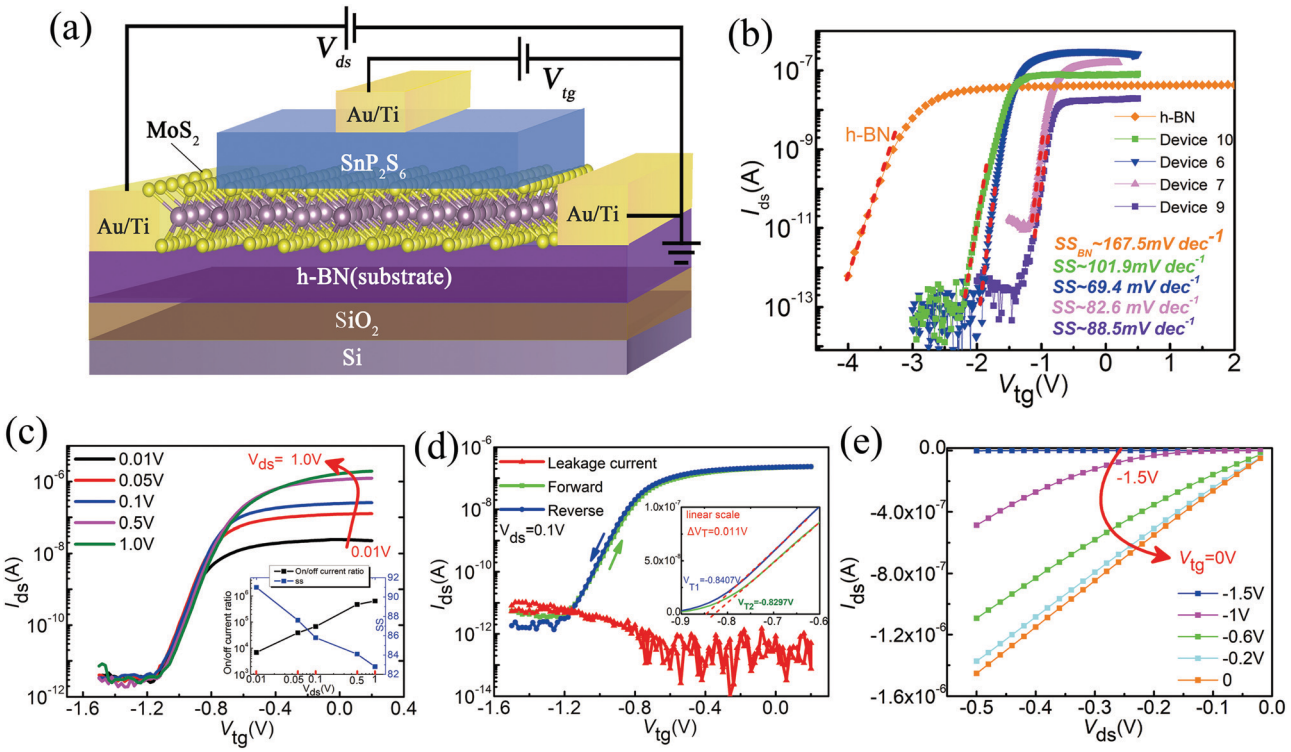

Fig. 5 Electronic properties of top-gated MoS_2 FETs using SnP_2S_6 as a gate dielectric. (a) Schematic of SnP_2S_6/MoS_2 FETs using h-BN as a substrate. (b) I_{ds}–V_{tg} curves of MoS_2 FETs at 300 K. The orange points represent the I_{ds}–V_{tg} curve of h-BN/MoS_2 FET as a contrasting device, in which h-BN is thinner than SnP_2S_6. Others are the I_{ds}–V_{tg} curves of SnP_2S_6/MoS_2 FETs which exhibit a subthreshold slope (SS) down to 69.4 mV dec^{-1}. (c–e) The best performance of the SnP_2S_6/MoS_2 FET (Device 7). (c) I_{ds}–V_{tg} characteristics measured at a drain bias ranging from 0.01 V to 1 V, and the inset shows the ON/OFF current ratio and SS extracted at different V_{ds} values. (d) Double-sweep I_{ds}–V_{tg} curves with a small hysteresis and leakage current, and the inset exhibiting the current on a linear scale (hysteresis gap $\Delta V_T \approx 0.011$ V). (e) I_{ds}–V_{ds} characteristics measured at different V_{tg} values.

The thin-film 2D materials are obtained through a mechanical exfoliation process (see ESI† Fig. S7A–C). Through the process described in the methods, 7 devices based on SnP_2S_6/MoS_2 flakes with various thicknesses were fabricated. The optimal electric performance was observed in the devices with the thickness of SnP_2S_6 about 49.7 nm (details in ESI† Fig. S6 and S8). Meanwhile, a top-gate h-BN/MoS_2 FET was also fabricated for comparison according to the schematic in ESI† Fig. S9C, in which h-BN (with a thickness of about 23.44 nm) is thinner than SnP_2S_6 (optical and AFM images in ESI† Fig. S6). Fig. 5(b) shows the top-gate transfer (I_{ds}–V_{tg}) characteristics of the h-BN/MoS_2 FET (the orange points) and four SnP_2S_6/MoS_2 FETs on the insulating h-BN substrate (see ESI† Fig. S7D). For the former one, a subthreshold slope (SS) value of 167.5 mV dec^{-1} and an ON/OFF ratio of 10^5 were obtained. While for the latter, SnP_2S_6/MoS_2 FETs, a small subthreshold slope (SS) value as low as 69.4 mV dec^{-1} of device 6 (blue points) was achieved at a drain bias of 0.1 V, which is close to the limit value[51] of 60 mV dec^{-1}. The device could even reach a high ON/OFF ratio of 10^7 and a high carrier mobility of 28.498 cm^2 V^{-1} s^{-1} at a higher drain bias (ESI† Fig. S10(A)). The threshold voltage (V_t) is a useful parameter to describe how much voltage is needed to initiate the channel conduction. Here, V_t of the fabricated device is as low as −1.1 V (ESI† Fig. S10(B)). Thus, the FETs with a smaller SS value, low on voltage and low threshold voltage can achieve effective switching at a low V_{ds}, thereby reducing the leakage current and power consumption of FET devices. It is remarkable for our SnP_2S_6 based FET to have such an excellent SS. In order to unravel the underlying mechanisms, we have carried out the following discussions. The contrast above indicates that thicker SnP_2S_6 films with thickness from 47.7 nm to 49.7 nm show the best performance and they have stronger gate control capability and low leakage current compared with 23.44 nm-thick h-BN. Thus, it means SnP_2S_6 owns a larger capacitance value than h-BN in MoS_2 FETs ($C_{SnP_2S_6} > C_{h\text{-}BN}$), though SnP_2S_6 is thicker than h-BN ($d_{SnP_2S_6} > d_{h\text{-}BN}$). According to the equation

$$C = \varepsilon_0\varepsilon_r/d$$

where C is the capacitance value per unit area of the gate dielectric, ε_0 is the permittivity of vacuum and ε_r is the relative dielectric constant. This confirms the high dielectric constant of SnP_2S_6 and the advantages of integrating an SnP_2S_6 nanosheet with semiconductor crystals to design FETs compared with h-BN, demonstrating the potential of 2D SnP_2S_6 as a high-k dielectric for low-power-consumption and miniaturized electronics.

As shown in Fig. 5(c and d), the typical SnP_2S_6/MoS_2 device exhibits a high ON/OFF ratio and steep SS simultaneously. The effect of the increasing drain bias, resulting in an augmented drive current and steeper SS value, is displayed in (Fig. 5(c)).

It can be seen that the best transistor performance is achieved at V_{ds} = 1 V, with a maximum measured on-state current of ~1 μA, ON/OFF current ratio close to 10^6, SS value as small as 82.6 mV dec^{-1} (inset of Fig. 5(c)) and the leakage current as low as ~10^{11} A (Fig. 5(d)). The corresponding hysteresis stability of the device is demonstrated in Fig. 5(d). To describe the hysteresis stability, we introduce the hysteresis window (ΔV_T), which is defined as the difference between the forward and reverse sweep threshold voltage.[52] As obtained on a linear scale in the inset of Fig. 5(d), $\Delta V_T = |V_{T1} - V_{T2}|$ was determined as low as 0.011 V, which is a fairly small value in FETs. However, the hysteresis window became larger after two days in a glove box (ESI† Fig. S11D–F) and different hysteresis behaviours were observed in some of our devices (ESI† Fig. S11A–C). The hysteresis variation may be associated with flake quality or fabrication process in a laboratory environment, which can lead to charge trapping at the interface, adsorption/desorption of ambient molecules or atmospheric moisture in the exposed active layers.[50,53] The small hysteresis could indicate that the fabricated SnP_2S_6/MoS_2 device shows an atomic flat and sharp interface. The corresponding output (I_{ds}–V_{ds}) characteristics measured in the case of different V_{tg} values (Fig. 5(e)) show linear I_{ds}–V_{ds} characteristics at low drain bias and saturated current at a high drain bias.

The breakdown electric field (V_{bd}) is another important parameter to evaluate the strength of the insulating layer. To test the current leakage and breakdown threshold, SnP_2S_6 is sandwiched between two electrodes to build a vertical device as shown in the inset of Fig. S12 (ESI†). At room temperature, V_{bg} is fixed at 0 V, and V_{ds} is swept.[54] The I_{ds}–V_{ds} curve is plotted in Fig. S12 (ESI†), where the initial low current increases slowly as the V_{ds} value increases. The current increases dramatically once V_{ds} approaches V_{bd}. After the breakdown, the device is permanently destroyed as a large current flows across SnP_2S_6. V_{bd} is estimated to be about 5 V (with a thickness of 26.5 nm), and the corresponding breakdown electric field F_{bd} could reach as high as 1.9 MV cm^{-1}.

Furthermore, to investigate the optoelectronic properties of our FETs, we put one of our SnP_2S_6/MoS_2 FETs (Device 9, its optical image in the inset of Fig. 6(b)) under 405 nm laser irradiation of 80 mW. The output and transfer characteristics in the dark (black), under 405 nm irradiation (blue) and after irradiation (red) are separately depicted in Fig. 6(b and c). Under illumination, the output characteristic of the device remains linear while the reduced electrical resistance of the semiconductor was obseved due to the photoconductive effect (PC effect), where the extra free carriers are generated by the photon absorption (Fig. 6(b)). Meanwhile, as shown in Fig. 6(c), a significant change in the threshold voltage was also observed when illuminated by 405 nm light. The shifting of the threshold voltage to the negative V_{tg} side is known as the photogating effect (PG effect). The PG effect is a phenomenon in which photogenerated holes get trapped and then attract more electrons, thus gradually increasing the channel conductivity.[55,56]

In Fig. 6(c), compared with the initial device in the dark, the off-state current after irradiation is dramatically increased by more than five orders of magnitude at the same V_{tg}, implying a long-time decay of the photoconductive state. As shown in

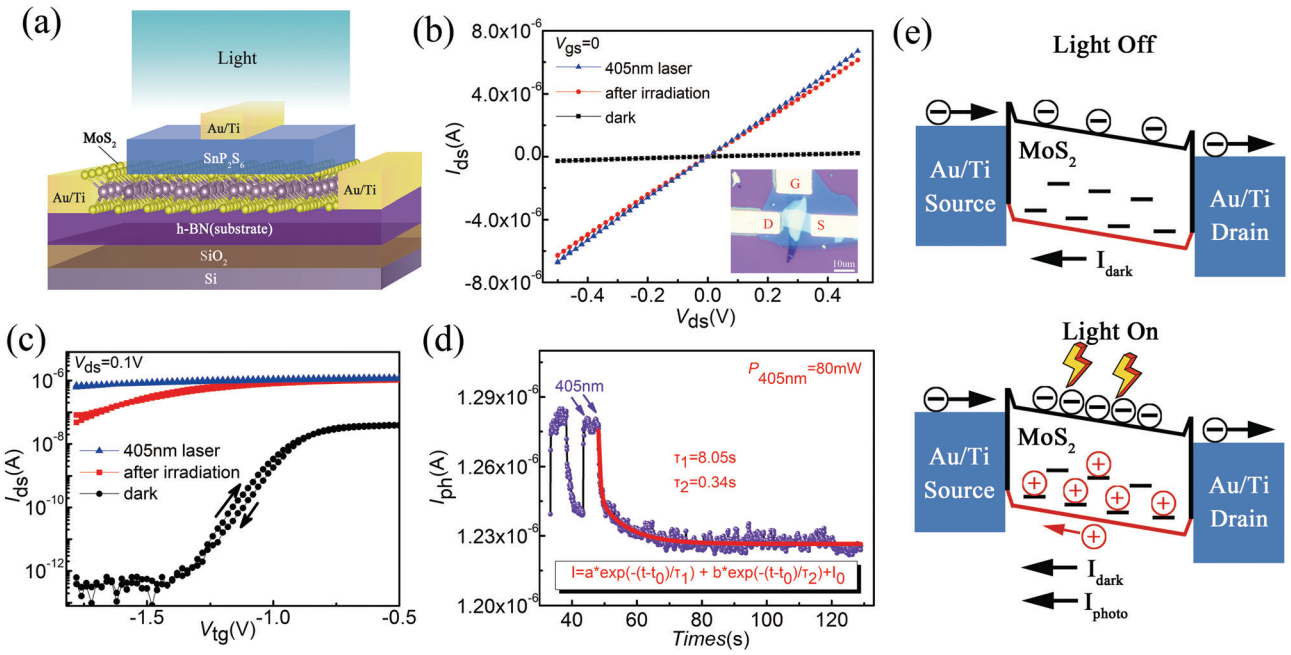

Fig. 6 Optical properties of top-gated SnP_2S_6/MoS_2 FETs. (a) Schematic diagram of photogating dominated SnP_2S_6/MoS_2 FETs (Device 9). (b) Typical I_{ds}–V_{ds} characteristics of Device 9 in the dark (black), under illumination (blue) and after irradiation (red), and the inset showing the optical image of the FET. (c) I_{ds}–V_{tg} characteristics showing transfer curve shifts in the negative V_{tg} direction under and after irradiation. (d) Photocurrent decay after a longer light pulse with longer (τ_1 ~ 8.05 s) and shorter (τ_2 ~ 0.34 s) time constants, which corresponds to (b) and (c). (e) Band diagram of the device without (top panel) and with light (bottom panel), showing hole trapping in shallower and deeper trap states close to the valence band.

Table 1 Comparison of SnP_2S_6 performance with other new 2D dielectrics

Materials	Dielectric constant	SS value [mV dec^{-1}]	ON/OFF ratio	Ref.
Ta_2O_5	15.5	61	10^6	58
Bi_2SeO_5	21	75	10^5	59
CaF_2	8.43	90	10^7	53
$In_2P_3S_9$	24	88	10^5	9
Sb_2O_3	11.5	64	10^8	60
SnP_2S_6	23	69.4	10^7	This work

Fig. S13 (ESI†), SnP_2S_6 has little effect on the optical response and persistent photocurrent of the device. Therefore, to explore the photocurrent decay of the device, we then check the transient characteristics by measuring the source–drain current at a fixed V_{tg} = 0 V in Fig. 6(d). An abrupt increase in I_{ds} was observed under 405 nm laser illumination, as a result of photoexcitation, followed by a much slower current increase. A very slow decay of the current can be observed when the light was switched off. This is because the trapped charges in the PG effect cause long sustained conductivity.[56] In order to quantify the trapping time constant, transient data were fitted with a biexponential equation[57]

$$I = I_0 + Ae^{(t-t_0)/\tau_1} + Be^{(t-t_0)/\tau_2}$$

where τ_1 and τ_2 are the two relaxation time constants, possibly corresponding to two different photoresponse mechanisms. The fast part is potentially due to the photoconductivity effect. The slow part could be regarded with the defect trapping or photogating effect. I_{ds} decays exponentially from $\sim$1.27 μA and saturates after 35 s with a longer time constant $\tau_1 \sim 8.05$ s and a shorter time constant $\tau_2 \sim 0.34$ s. (See the detailed parameter values in the ESI† Table S2 and time constants for different wavelengths in the ESI† Fig. S14). The shorter decay component could be attributed to the PC effect and shallower traps, while the longer decay component due to the PG effect might be caused by deeper (middle gap) traps in Fig. 6(e), as elucidated by Furchi *et al.*[55] Simultaneously, the longer time constants of the devices on SiO_2/Si FETs are $\sim$6.814 s and $\sim$13.39 s, which are close to 5.05 s in the FETs on h-BN (see details in the ESI† Fig. S15). Consequently, we infer that the long persistent photocurrent measured in our devices is not likely due to the traps at the MoS_2/SiO_2 or MoS_2/h-BN interface since our SnP_2S_6/MoS_2 FETs fabricated on h-BN which have rare charge trapping.[50] Thus, it is conjectured that the defect trapping might have mainly originated from photo charge trapping associated with MoS_2 defects and the MoS_2/SnP_2S_6 interface. Therefore, improving the quality of MoS_2 and optimizing the MoS_2/SnP_2S_6 interface can be a reasonable approach to decrease this phenomenon.

Finally, the good stability, reliability and reproducibility of the devices are summarized as shown in Fig. S16–S19 (ESI†).

To highlight the performance of the SnP_2S_6 dielectric, the main set of achievements of the present study, such as the dielectric constant, SS value and ON/OFF ratio, are presented in Table 1. Compared with other new 2D dielectric materials, the excellent performance of SnP_2S_6 is comparable to or even better than those of these materials.

Conclusion

In this paper, we have systematically investigated the photoelectric and electrical properties of a novel 2D SnP_2S_6 crystal. Moreover, it was integrated into MoS_2 based FETs to serve as a top gate dielectric. The results demonstrate its excellent properties including a large dielectric constant ($\approx$23, compared with h-BN), a fairly small SS value (as low as 69.4 mV dec^{-1}), a high ON/OFF ratio (reaching 10^7), a negligible hysteresis, and a considerable breakdown voltage ($\approx$1.9 MV cm^{-1}). Due to its good photoelectric properties, good reliability and reproducibility (0.5 standard deviation of threshold voltage), SnP_2S_6 could become a potential candidate for the construction of advanced optoelectronic and electronic devices.

Methods

Material characterization

Raman spectra are recorded using a Horiba confocal Raman system with an excitation laser of 532 nm. The morphology characterization and thickness calibration of the SnP_2S_6 film as well as thickness measurement of h-BN and MoS_2 are carried out with an optical microscope and AFM instruments.

Fabrication of an SnP_2S_6 phototransistor and SnP_2S_6/MoS_2 FET devices

An SnP_2S_6 phototransistor was fabricated by exfoliating thin flakes onto heavily doped silicon substrates. The top electrodes are defined using a standard photolithography process followed by thermal evaporation of the Ti/Au metal, and a lift-off process. We have built three batches of SnP_2S_6/MoS_2 devices on a SiO_2/Si substrate and an h-BN substrate, respectively. Thin-film 2D materials are obtained through a mechanical exfoliation process first. Then, the 2D nanosheets of top-gate FETs are stacked up by a polydimethylsiloxane (PDMS) assisted transfer technique onto an h-BN nanosheet to develop heterostructures. The source–drain and gate electrodes Ti/Au of each device were patterned and deposited by photolithography and a lift-off process. Preparation methods for other devices including back-gate FETs and top-gate FETs on different substrates adjust according to their schematic.

Electrical and optical characterization measurements

We tested the device directly after fabrication. Electrical and photoelectrical characterization of devices including I_D–V_G, I_D–V_D and I_{ph}–t involved measurements were performed under vacuum condition at room temperature (300 K) using a probe station.

Author contributions

J. H. and A. Z. carried out the electrical and optoelectronic measurements. E. P., J. C. and R. B. assisted in the device fabrication and electrical measurement. E. P. carried out the

AFM measurement. J. L. and X. J. carried out the Raman characterization. A. M. and Y. V. conducted dielectric measurement and crystal growth. Q. L., G. C. and P. M. analyzed the data. J. H., A. Z. and F. L. wrote the manuscript. Q. L. and G. C. revised the manuscript. F. L. supervised the project. All the authors commented on the manuscript.

Conflicts of interest

There are no conflicts to declare.

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