

## REVIEW

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# Application of organic field-effect transistors in memory

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Organic semiconductors for electronic devices have attracted much attention in scientific research and industrial applications. In the past few decades, functional organic field-effect transistors (OFETs) have developed rapidly, especially OFETs with memory function. Here, through a detailed introduction of the background, memory mechanism and structure construction, we make a comprehensive summary of memory applications based on OFETs. Further, we describe four types of OFET memories, *i.e.* floating-gate OFET memory, electret OFET memory, ferroelectric OFET memory, and optoelectronic OFET memory. Finally, we put forward challenges in the development of OFET memory and look forward to the future trend of the development of OFET memory.

## 1. Introduction

Since the 1990s, electronic devices have become a part of our lives. Among them, memory is an indispensable component of various electronic information products (computers, mobile phones, game consoles, wearable devices, *etc.*). It is generally believed that huge value will be extracted from data in the future. In addition to the requirement for strong computing power, the massive storage of data is also critical to mining the value of the data. Therefore, with the advent of the internet of things, 5G, big data, and the artificial intelligence (AI) era, the memory semiconductor market has begun a new round of explosive growth.

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Traditional memory mainly uses optical, electrical or magnetic signals for information storage. The main storage technologies are divided into four types: (1) hard disk drives (HDDs) based on magnetic signals; (2) capacitor-based memory, including random access memory (DRAM) and read-only memory (ROM); (3) optical signal optical discs, whose products are mainly CD discs; and (4) flash memory based on FET devices, mainly including NOR flash memory and NAND flash memory.<sup>1</sup> Although these storage technologies are widely used in various electronic devices, they all have deficiencies. DRAM can support fast reading and writing, but the charge in the DRAM memory unit will decay and disappear within a few milliseconds. Therefore, it needs to be constantly refreshed and a large amount of electrical energy is consumed during the charge compensation process. Although the retention time of flash memory technology is longer than that of DRAM, the programming/erasing (*P/E*) speed is low, and the life of reading



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and writing is also limited. HDDs are the cheapest storage technology, but their access speed is relatively slow, and they are contact read, and hence it is very easy to cause damage to the surface of the disk. Currently, DRAM and NAND flash memory are the mainstream storage technologies for modern computing systems, smart phones, and data processing equipment. However, for computing systems, these two types of memory cannot exist alone. For example, an 8GB DRAM chip consumes about 20% of the power used for refreshing to maintain the stored content. If the power is cut off, the stored content will disappear, and it will not be restored even if the power is turned on again. Therefore, DRAM is not suitable for use as code storage for start-up and application programs. The system must be equipped with other non-volatile memories (NVMs) to perform code storage functions. The data stored in flash memory based on FET devices can be kept for many years even if the power is off. NOR flash memory is much more expensive than DRAM, and the cost per byte is one or two orders of magnitude higher than that of NAND flash memory. NAND flash memory has long been known for its high density, low cost, and long-term memory. It is the dominant non-volatile storage technology in silicon materials. However, NAND flash memory has a fatal flaw. NAND flash memory can only be read sequentially and cannot access specific bytes. Computer operations require random addressing to read, so NAND flash memory must be paired with DRAM to be used for code storage.

In addition, NAND flash page writing is a slow and energy-intensive technology. It usually takes 300  $\mu\text{s}$  and 80  $\mu\text{J}$  to perform a page write. With the advent of the post-Moore era, silicon flash memory faces the quantum limit of the so-called Moore's law, that is, in the range of 10 nm, the charge stored in the floating gate structure easily leaks. Although there are some reports of 3-D NVM devices which can further reduce costs, that should also be a stopgap measure. Where is memory going? We have to turn our eyes to emerging storage technologies. Emerging storage technologies mainly include phase change PCM,<sup>2</sup> ferroelectric RAM,<sup>3</sup> magnetic RAM,<sup>4</sup> memristors,<sup>5,6</sup> and flash memory.<sup>7–13</sup> Compared with inorganic storage materials,

organic materials have many advantages as storage materials, such as low cost, large area processing, flexibility, and low temperature compatibility. The most important thing is that the molecular size of organic materials is about 1–100 nm (from small molecules to polymers), so the use of organic materials can increase the storage density and reduce the size of the memory. Compared with two-terminal memory,<sup>14–18</sup> three-terminal OFET memory has many advantages, such as one does not need to add other circuit components to select the target cell (to facilitate integration),<sup>19,20</sup> and one can perform accurate charge modulation, non-destructive readout and multi-bit storage. Furthermore, the reason why we value OFET devices is that, besides being memory, OFETs have many other functional applications, such as simulating nerve synapses<sup>7</sup> and constructing logic circuits.<sup>21</sup> When the light-emitting capabilities and switching performance are combined, light-emitting transistors (LETs)<sup>22</sup> can also be constructed. So, OFET memory opens up possibilities for multifunctional integrated circuits. Here, we mainly introduce various emerging storage technologies based on OFET memory. The structure of this review is as follows: first we briefly introduce the structure and principles of OFET-based memory, and then review the working principles and main research progress of OFET-based floating gate memory, electret memory, ferroelectric memory, and optoelectronic memory, and the last part gives the conclusions and outlook of the review.

## 2. Mechanism

A conventional OFET device is generally composed of four parts: a source–drain electrode, a semiconductor layer, a dielectric layer, and a gate electrode. The source–drain electrode is in direct contact with the semiconductor. The charge density in the semiconductor is determined by the vertical electric field provided by the gate, and the gate and the semiconductor are separated by a dielectric layer. In addition, because organic materials have poor heat resistance, and the deposition of the gate electrode and insulating layer films usually requires higher temperature, in order to prevent the organic layer from being damaged by high temperature, OFETs usually adopt a bottom gate structure. During device operation, the voltage applied between the source and drain electrodes is called the source–drain voltage ( $V_D$ ), and the current between the source and drain electrodes is called the source–drain current ( $I_D$ ), also known as the channel current. The  $I_D$  value is determined by the carrier mobility ( $\mu$ ) and the majority carrier in the channel. The voltage applied to the gate is called the gate voltage ( $V_G$ ), and a channel is created by bending the energy band, and the carrier density in the channel is controlled by the gate voltage.  $I_D$  vs.  $V_G$  and  $I_D$  vs.  $V_D$  are called transfer and output curves, respectively. In the curve of  $I_{D,\text{sat}}^{1/2}$  and  $V_G$ , its slope is the carrier mobility in the saturation region, and the intercept with abscissa  $V_G$  is the threshold voltage ( $V_{\text{th}}$ ), which can be understood as the transition from the OFF-state to the ON-state of the device. However, a conventional OFET device does not have storage functions. Once the operating voltage is removed, the



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charge accumulated in the channel will soon be depleted and return to the original state. Generally speaking, a storage material needs at least two different states to represent the “0” and “1” signals in binary. OFET memory can be divided into two categories according to the storage mechanism: ferroelectric transistor (FeFET) memory based on dipole orientation conversion,<sup>9</sup> memory based on charge traps, such as floating gate transistor memory,<sup>23</sup> electret transistor memory,<sup>24</sup> and phototransistor memory.<sup>12</sup>

Taking p-channel floating gate OFET memory as an example, by applying a negative voltage on the gate electrode, holes in the semiconductor channel cross the barrier into the floating gate and are captured in the floating gate layer. The charge trapped in the floating gate layer changes the distribution of carriers in the channel, resulting in a negative shift in the transfer curve and  $V_{th}$ . This process corresponds to “programming” (PGM). Conversely, if a positive gate voltage is applied, the transfer curve and  $V_{th}$  will shift positively. This process corresponds to “erasing” (ERS). The trapped holes return to the channel through tunnelling or recombination with the opposite charge (electrons) injected. The “read” operation is implemented by applying a small gate voltage to detect the programmed state (OFF-state) or erased state (ON-state) corresponding to the “1” state and “0” state of the memory, respectively. The mechanism of tunnelling is mainly divided into direct tunnelling and Fowler–Nordheim tunnelling.<sup>25,26</sup> The density of the tunnelling charge is mainly related to the barrier height and the applied voltage, which can be derived from the Wentzel–Kramers–Brillouin (WKB) approximation (eqn (1)).<sup>27,28</sup>

$$J = \frac{q^3 F^2}{16\pi^2 h^2 \Phi_B} [-4(2m_{ox}^*)^{1/2} \Phi_B^{3/2} / 3hqF] \quad (1)$$

where  $m_{ox}^*$  is the effective mass of the charge carrier in the forbidden gap of the dielectric layer,  $\Phi_B$  is the barrier height,  $q$  is the fundamental unit of charge,  $h$  is Planck's constant, and  $F$  is the electric field through the tunnelling dielectric layer.

The storage performance of OFETs is usually evaluated by the memory window, storage density,  $P/E$  speed, retention time and durability.

The memory window ( $\Delta V_{th}$ ) is the most critical factor of a memory device, which refers to the offset value of the threshold voltage in the programmed and erased states, as shown in eqn (2):

$$\Delta V_{th} = V_{th}^{PGM} - V_{th}^{ERS} \quad (2)$$

The storage density ( $\Delta n$ ) is generally determined by the memory window, which can be calculated from eqn (3):

$$\Delta n = \frac{\Delta V_{th}}{e} \times C_i \quad (3)$$

where  $C_i$  is the total capacitance per unit area and  $e$  is the elementary charge ( $1.602 \times 10^{-19}$  C).

The  $P/E$  speed refers to the tunnelling time of charge between the charge trapping medium and the channel. The faster the  $P/E$  speed and the shorter the access time, the more beneficial it is to improve the overall system performance of

modern computing systems. The retention time reflects the reliability of the device and it is usually extrapolated from the retention time plot. It is defined as the current in the ON-state until the device current reaches 50% of the initial value. It can be improved by increasing the dielectric constant  $\kappa$  of the blocking layer and reducing the thickness of the tunnelling layer. In addition, durability is also an important criterion for measuring device reliability. It refers to the ability of the memory to withstand repeated programming and erasing. In addition to the several evaluation methods above, the energy consumption of modern memory also needs to be carefully considered. For example, the memory unit maintenance power, read, write and erase power, *etc.* At present, the durability of OFET memory is generally between  $10^2$  and  $10^5$ . If one wants to replace DRAM as the main storage device, one needs to be able to repeatedly program and erase at least  $10^{12}$  times. If one wants to replace NAND flash as an auxiliary storage device, one needs to be able to program and erase at least  $10^6$  times. However, OFET memory devices also have their own advantages, such as low cost, light weight, *etc.* In addition, compared to inorganic FET memory devices, OFET memory devices will have good application prospects in future flexible devices. Therefore, the development of OFET memory is a promising thing.

### 3. Floating gate OFET memory

Since Kahng and Sze first used floating gate devices to obtain non-volatile memory in 1967,<sup>29</sup> floating gate memory has been widely used in various electronic devices. Compared with traditional transistors,<sup>30</sup> floating gate transistors have a floating gate layer, as shown in Fig. 1. When a gate voltage is applied for “programming” or “erasing” operations, electrons or holes are captured or released by the floating gate layer by direct tunnelling or Fowler–Nordheim tunnelling.<sup>25,26</sup> The trapped charges can shield the vertical electric field between the gate and the channel, resulting in a change of the threshold voltage. More importantly, the gate voltage can effectively regulate the amount of trapped charges in the floating gate.

The floating gate layer can be a metal or a semiconductor. Due to their compatibility with silicon devices, silicon or germanium particles were used as the floating gate layer at the beginning.<sup>31</sup> The common deposition techniques are vacuum deposition and ion beam synthesis. In principle, metal nanoparticles (NPs) should be superior to silicon nanocrystal memory, because metal particles have better electron affinity.<sup>26,32,33</sup>

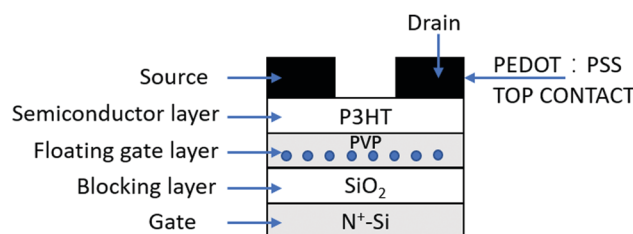


Fig. 1 Schematic of a top contact floating gate OFET memory device.

Gold NPs have high chemical stability and can be processed in solution. Varahramyan and co-workers integrated Au NPs into the gate dielectric of OFET transistors by self-assembly, resulting in a memory effect.<sup>26</sup> The device used poly(3-hexylthiophene-2,5-diyl) (P3HT) as the channel semiconductor, integrated Au NPs onto the surface of SiO<sub>2</sub> by self-assembly, and then used poly(4-vinyl phenol) (PVP) as a tunnelling layer, as shown in Fig. 1. However, the retention times of the devices using top and bottom contacts were quite different. The retention time of the device with the bottom contact was only 60 s. When the top printed PEDOT:PSS was used, the retention time could be extended to 200 s, but it was still very short. Because the PEDOT:PSS electrode was in direct contact with P3HT, the effect of traps in the P3HT film became unimportant; the longer retention time was not caused by the top contact structure. It might be caused by the increased distance between the source–drain electrode and the gate dielectric or the charge trapped in the dielectric/P3HT interface. However, no matter top contact or bottom contact structure, the retention time was still very short, which might be due to the rapid release of charge from the interface charge traps and the poor insulation performance of the PVP barrier layer. We can learn from the article that more gold nanoparticles can achieve a larger memory window. Although the device exhibits hysteresis without Au NPs, its memory window is very small. Beag *et al.* reported a solution-treated poly[[9,9-dioctylfluorenyl-2,7-diyl]-*co*-(bithiophene)] (F8T2) transistor with a bottom gate/top contact structure.<sup>34</sup> Au NPs were located between polystyrene (PS) and cross-linkable-cPVP by means of thermal deposition. The change of the threshold voltage was directly related to the number of Au NPs deposited. The larger the number of Au NPs, the greater the change of the threshold voltage at the same operating voltage. By application of high gate fields ( $\pm 70$  V  $V_G$  sweep), a flexible nano-floating-gate memory (NFGM) device with 1 nm thick Au thermal deposition showed an  $I_{\text{on/off}}$  ratio and memory window of *ca.* 10<sup>3</sup> and 40 V, respectively. The OFET characteristics of the device were very dependent on the existence of the PS intermediate layer between cPVP and F8T2, which could be explained in the following ways: (i) the energy distribution of the trap states at the interface was reduced, and (ii) the passivation of the deep traps of the interface by the PS layer. In addition, the thermal deposition of precious metals is not a good method. On the one hand, the size of the nanoparticles cannot be accurately controlled. On the other hand, the nanoparticles also easily penetrate into the polymer during thermal deposition.

In addition to using Au NPs,<sup>26,31–33</sup> Ag, Cu, or Al NPs can also be used as the floating gate capture layer.<sup>35</sup> Kim and co-workers used poly 1,8-bis(dicarboximide)-2,6-diyl-*alt*-5,5'-(2,2' bithiophene) (P(NDI2OD-T2)) as a semiconductor, and systematically studied the effect of various metal NPs on the memory characteristics. These NPs were embedded within bilayers of various polymer dielectrics PS/PVP and PS/poly(methyl methacrylate) (PMMA). The device structure is shown in Fig. 2c. The results showed that the retention characteristics of NFGM devices are affected by the size, shape and spatial distribution of NPs, and the memory window is affected by the density of NPs.

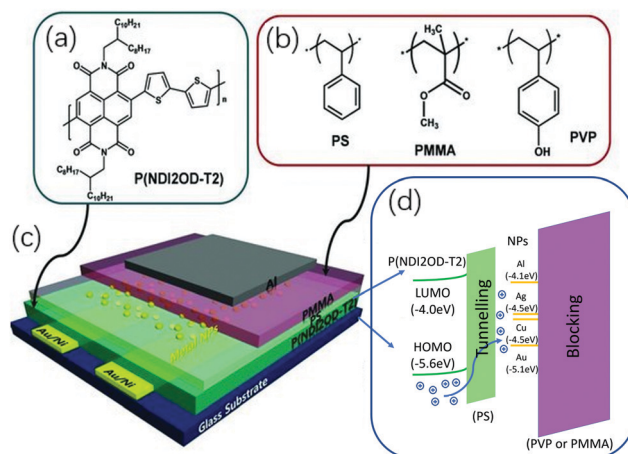


Fig. 2 Molecular structures of (a) the semiconductor P(NDI2OD-T2) and (b) the dielectric PS, PMMA and PVP. (c) Structure of an organic NFGM device based on TG/BC OFET geometry. (d) Schematic illustration of the charge transfer mechanism of the organic NFGM device shown in (c). Reproduced with permission.<sup>35</sup> Copyright 2013, John Wiley and Sons.

The Au NP device with the highest NP density showed the widest memory window  $\approx 52$  V. Al NPs had a very narrow memory window because of their large diameter and low density. However, the charge of NPs trapped at high surface density resulted in lower retention time due to leakage between adjacent NPs. The retention time of devices fabricated with Cu NPs was as high as 10<sup>8</sup> s, which might be mainly due to the small surface density of Cu NPs. They also studied the influence of different dielectrics on the device characteristics. By comparison, they found that devices using PMMA as a blocking layer had a retention time greater than devices using PVP as a blocking layer. The reason might be due to the relatively long charge relaxation time of PMMA.

Using metal oxides as nanoparticles is also a good choice. For example, Katz and co-workers reported an OFET memory using ZnO as the floating gate capture layer.<sup>36</sup> The device had a ZnO film coated on the surface of SiO<sub>2</sub>, and then a pentacene film deposited on it. By adjusting the thickness of ZnO, the device exhibited n-channel, bipolar, and p-channel characteristics. The highest electron mobility was 7.2 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>, and the  $I_{\text{on/off}}$  ratio was 70. When the ZnO layer was very thin, the transistor showed a very high reversible hysteresis p-channel behaviour. After applying a voltage of +100 V for 1 s, its retention time was 200 s.

In addition, ferritin nanoparticles can also be used as a floating gate capture layer. Cho and co-workers reported an OFET memory device using discrete ferritin nanoparticle-based gate dielectrics.<sup>37</sup> Ferritin multilayer films were deposited by the successive Layer-By-Layer (LBL) deposition of cationic poly(allylamine hydrochloride) (PAH) and anionic ferritin NPs onto 200 nm-thick SiO<sub>2</sub> insulator-coated or 50 nm-thick Al<sub>2</sub>O<sub>3</sub>-coated plastic substrates at room temperature. The device structure is shown in Fig. 3a. Pentacene acts as a semiconductor layer. When using SiO<sub>2</sub> as the gate dielectric layer, the device could generate a memory window of 20 V and an  $I_{\text{on/off}}$  ratio of 10<sup>4</sup> at

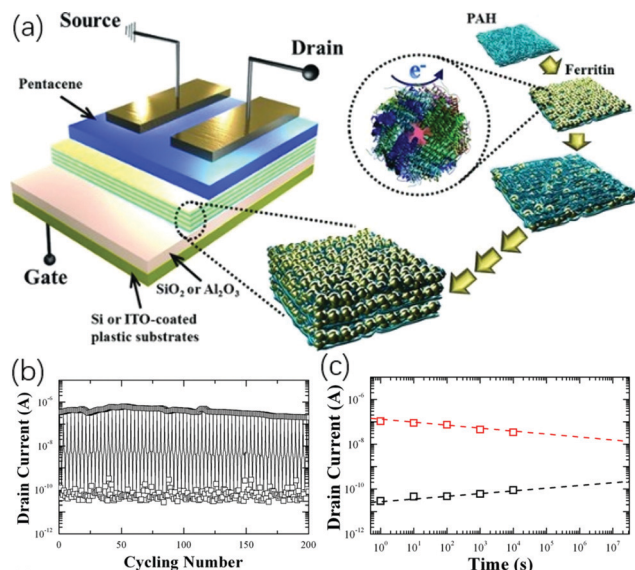


Fig. 3 (a) Schematic representation of the OFET memory device with LBL-assembled (PAH/ferritin NP)<sub>n</sub> multi-layered gate dielectrics. (b) Cycling and (c) retention time tests for devices with (PAH/ferritin NP)<sub>40</sub> multi-layers. Reproduced with permission.<sup>37</sup> Copyright 2013, John Wiley and Sons.

an operating voltage of  $\pm 100$  V and a bias voltage time of 1 s. After 300 cycles of testing, the *P/E* state is well maintained with a retention time of  $10^4$  s, as shown in Fig. 3b. Through calculations, the total charge captured was  $2.5 \times 10^{12} \text{ cm}^{-2}$ . After using high- $\kappa$   $\text{Al}_2\text{O}_3$  as the gate dielectric layer, the operating voltage could be greatly reduced. Using an operating voltage of  $\pm 20$  V, the memory window also was 7.14 V, and the  $I_{\text{on/off}}$  ratio was  $1.3 \times 10^2$ . After applying an operating voltage of  $\pm 50$  V, it was comparable to the memory window of Si-based devices. Organic materials can also be used as a nano-floating gate in OFET memory devices.<sup>38–40</sup> Wang and co-workers reported an OFET memory device using sputtered carbon-nanoparticles (C-NPs) as a nano-floating gate.<sup>41</sup> The carbon nano-floating gate is applied not only to pentacene-based p-type OFETs but also to *N,N'*-ditridecyl-3,4,9,10-perylenetetracarboxylic diimide (PTCDI- $\text{C}_{13}\text{H}_{27}$ )-based n-type OFETs. The device structure is shown in Fig. 4. Sputtered C-NPs are a good floating gate trapping material due to their low cost, simple fabrication process, and the ability to form uniform and discrete charge trapping sites. In p-type devices, when only PS was used as the electret material, the device had only a 10 V memory window at an operating voltage of  $\pm 80$  V. When the density of C-NPs was increased, the memory window was greatly increased. After sputtering for 2 min of C-NPs, the memory window reached the maximum value of 35 V and the  $I_{\text{on/off}}$  ratio was also increased to  $10^6$ . By extrapolating the retention data, the storage of data could be kept for several years. After  $10^3$  *P/E* cycle tests, the device performance did not decrease significantly. As shown in Fig. 5, n-type devices also have relatively good performance. Chen and co-workers reported an OFET memory device using polyfluorene (PF) and poly(fluorene-altbenzo[2,1,3]thiadiazole) (PFBT) as the floating gate layer, whose diameter was between 50 and 70 nm,<sup>42</sup> poly(methacrylic acid) (PMAA) was used as a tunnelling layer, and pentacene as a

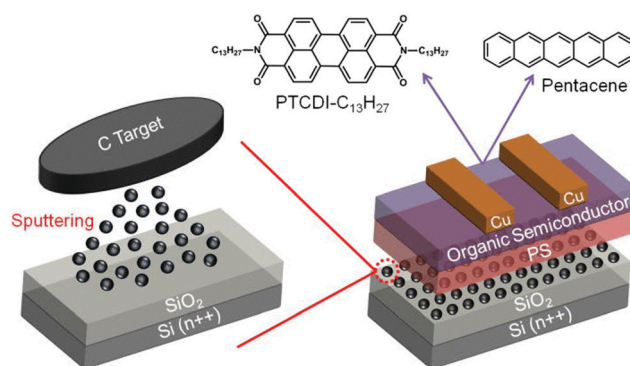


Fig. 4 Schematic representation of a pentacene-based or PTCDI- $\text{C}_{13}\text{H}_{27}$ -based floating gate OFET memory device (right), in which a PS layer and sputtered C-NPs (left) on top are employed as a tunnelling dielectric and nano floating gate, respectively. Reproduced with permission.<sup>41</sup> Copyright 2014, AIP Publishing.

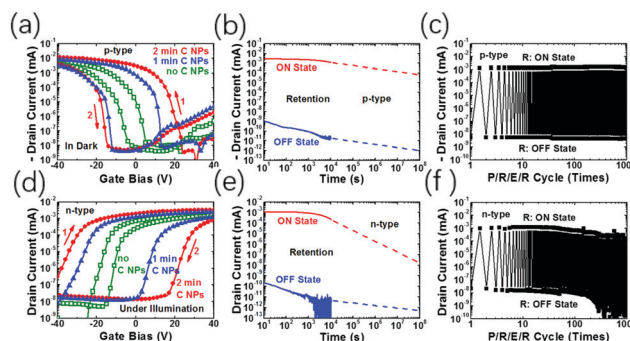


Fig. 5 (a) Transfer curves (scan from  $V_G = 80$  V to  $V_G = -80$  V and then back to 80 V,  $V_D = -3$  V, measured in the dark) of pentacene-based floating gate OFET memory without C-NPs (open squares), and with C-NPs sputtered for 1 min (triangles) and for 2 min (circles). (b) Retention curves (reading in the dark at  $V_G = 0$  V and  $V_D = -3$  V, the dashed line is extrapolation of the experimental data) after *P/E* in the dark and (c) *P/R/E/R* endurance of the device with a C sputtering time of 2 min shown in (a). (d) Transfer curves (scan from  $V_G = -80$  V to  $V_G = 80$  V and then back to  $-80$  V,  $V_D = 3$  V, measured under illumination) of PTCDI- $\text{C}_{13}\text{H}_{27}$ -based floating gate OFET memory without C-NPs (open squares), and with C-NPs sputtered for 1 min (triangles) and for 2 min (circles). (e) Retention curves (reading in the dark at  $V_G = 0$  V and  $V_D = 3$  V, the dashed line is extrapolation of the experimental data) after *P/E* under illumination and (f) *P/R/E/R* endurance of the device with a C sputtering time of 2 min shown in (d). Reproduced with permission.<sup>41</sup> Copyright 2014, AIP Publishing.

semiconductor layer. Compared with PF, PFBT-10 nm could make the trapped charge more stable due to the lower LUMO. Under an operating voltage of  $\pm 50$  V, a 35 V memory window could be generated. The retention time was longer than  $10^4$  s, and the on/off ratio was greater than  $10^4$ . The particle size of the NPs also had an important impact on the device performance. Only when the most suitable particle size of NPs is selected can the device get better performance. 6,13-Bis(triisopropylsilyl-ethynyl)pentacene (TIPS-PEN) is reported as a floating gate capture layer.<sup>43–45</sup> Wang and co-workers reported a P3HT based OFET nonvolatile memory.<sup>43</sup> The device used TIPS-PEN microdomains distributed in a matrix of polymer PS as a floating gate layer, P3HT as a semiconductor layer, PMMA as a blocking layer,

and SiO<sub>2</sub> or Al<sub>2</sub>O<sub>3</sub> as a tunnelling layer. Under an operating voltage of  $\pm 40$  V, the memory window was 14 V, the  $I_{\text{on/off}}$  ratio was higher than 350, the reliable memory endurance exceeded 500 cycles and the retention time exceeded 5000 s.

Recently, there was a report in which polysilicon is used as the floating gate capture layer. Yang and co-workers reported an OFET memory device with Poly-Si, polymethylmethacrylate, and pentacene used as a floating-gate layer, tunnelling layer, and active layer, respectively.<sup>46</sup> At an operating voltage of  $\pm 60$  V, there was a memory window of 9.28 V, an  $I_{\text{on/off}}$  ratio of  $10^2$ , and an  $I_{\text{on/off}}$  speed of 0.1 s, but the retention time was shorter, only 200 s.

Although with floating gate OFET memory devices one can accurately adjust the memory window, as well as a large  $I_{\text{on/off}}$  ratio, their operating voltage needs to be further reduced to reduce energy consumption. In addition, the retention time of the device is relatively short, which can be improved by reducing the thickness of the tunnelling layer and the blocking layer. For example, by using a vertical structure or combining an electret material with a floating gate structure to construct a device, the leakage of trapped charges is reduced or the ability to trap charges is increased, thereby increasing the retention time of the device.

## 4. Polymer electret OFET memory

Similar to floating gate OFET memories, the storage mechanism of polymer electret OFET memories is also based on charge traps. Electrets are dielectric materials with quasi-permanent charge or dipolar polarization, and have been widely used in the fields of sensors, memories, and gas filters. In this section, we will review the development history of electret OFET memory.

In 2002, Katz reported polymer electret OFET memory (PEM) for the first time, obtaining a transistor device similar to a floating gate structure.<sup>47</sup> Subsequently, the application of electrets in OFET memory has developed rapidly.<sup>48–50</sup> Charges trapped in polymer electrets can be generated by the following mechanisms: (i) charges trapped by structural defects and impurity centers; (ii) orientation of dipoles (in polar materials); and (iii) build-up of charges near heterogeneities such as grain boundaries (in polycrystalline materials) and amorphous-crystalline interfaces (in semicrystalline polymers).<sup>51</sup> In 2008, Kim and co-workers systematically studied the characteristics of various polymer electrets,<sup>51</sup> and concluded that only non-polar and hydrophobic polymers could be used as effective dielectrics, acting like floating gates in floating gate memories. Polar or hydrophilic polymer electrets would quickly dissipate in the conductive channels generated by dipoles, moisture and ions, and they didn't have the ability to store charges. A series of polymer electrets, including PS, P $\alpha$ MS, poly(4-methyl styrene) (P4MS), poly(4-vinyl phenol) (PVP), poly(2-vinyl pyridine) (PVPyr), poly(2-vinyl naphthalene) (PVN) and PVA, were used as the polymer electret layer in a conventional bottom-gate/top-contact pentacene FET device configuration. The polarity of the electret material is shown in Fig. 6a. By keeping the other

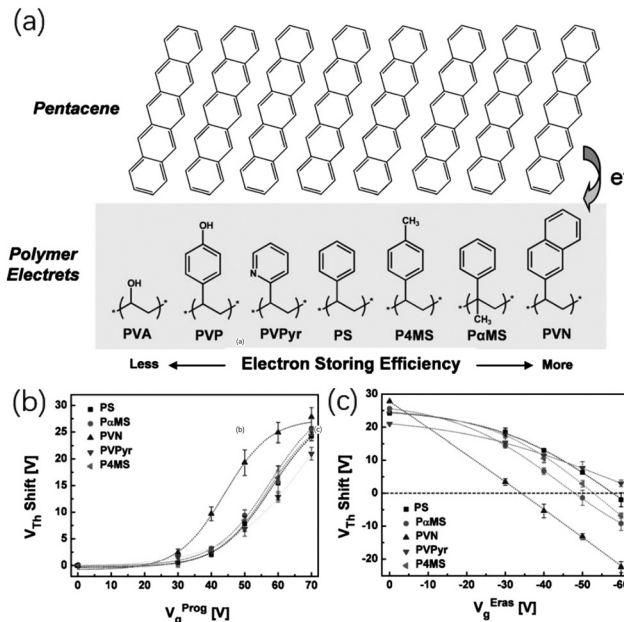


Fig. 6 (a) Schematic representation of the electron-storage efficiency of polymer electret materials estimated from the PEM characteristics. Shifts in  $V_{\text{th}}$  of PEM devices after the application of different gate biases during the (b) programming and (c) erasing processes. The dotted lines are fits to the measured points using a sigmoid function (Boltzmann fits). Reproduced with permission.<sup>51</sup> Copyright 2008, John Wiley and Sons.

parameters constant, it is concluded that the lower surface energy and bulk conductivity of the electret materials are the reasons for the stable memory. The additional electret layer does not reduce the performance of the OFET device. On the contrary, the polymer electret may improve the performance of the transistor by improving the pentacene morphology and interface electronic state. As the polarity of the polymer electret decreases and the surface hydrophobicity increases, the memory window of the PEM device is significantly improved, as shown in Fig. 6b and c. Table 1 lists the data of various PEM devices, such as  $\mu_{\text{FET}}$ ,  $V_{\text{th}}$ , degree of  $V_{\text{th}}$  shift, retention time, and  $I_{\text{on/off}}$ .

The memory window in PEMs with highly polar and hydrophilic polymers is very small and this can be explained by the difference in conductivity. The shorter retention time might be due to the rapid dissipation of charge in the conductive path, which formed by dipoles, moisture or ions.

Table 1 Measured fundamental PEM characteristics:  $\mu_{\text{FET}}$ ,  $V_{\text{th}}$ , degree of  $V_{\text{th}}$  shift, retention time, and  $I_{\text{on/off}}$

	$\mu_{\text{FET}}$ [cm <sup>2</sup> V <sup>-1</sup> s <sup>-1</sup> ]	$V_{\text{th}}$ [V]	$V_{\text{th}}$ shift [V]	Retention time [10 <sup>5</sup> s]	$I_{\text{on/off}}$
Bare SiO <sub>2</sub>	0.23 ± 0.05	-12.3 ± 2.0	Negligible	N/A	10 <sup>6</sup>
PS	0.26 ± 0.23	-7.1 ± 4.8	22.1 ± 2.8	5.2	10 <sup>5</sup>
P $\alpha$ MS	0.35 ± 0.15	-6.6 ± 3.4	26.0 ± 2.7	2.2	10 <sup>5</sup>
P4MS	0.25 ± 0.07	-10.4 ± 1.4	24.1 ± 1.2	2.1	10 <sup>5</sup>
PVP	0.21 ± 0.05	-12.1 ± 2.1	17.0 ± 1.1	0.24	10 <sup>5</sup>
PVPyr	0.12 ± 0.13	-11.5 ± 3.5	21.0 ± 1.7	0.42	10 <sup>5</sup>
PVN	0.61 ± 0.05	-11.6 ± 2.5	27.8 ± 1.8	3.4	10 <sup>6</sup>
PVA	0.07 ± 0.06	-13.1 ± 3.7	Negligible	N/A	10 <sup>5</sup>

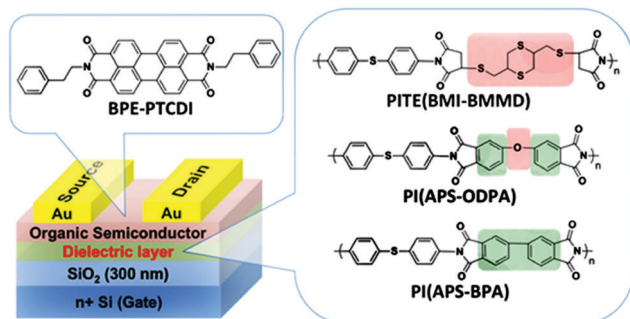


Fig. 7 Schematic diagram of the studied polymer electret OFET memory devices and the molecular structures of the studied PIs. Reproduced with permission.<sup>55</sup> Copyright 2014, John Wiley and Sons.

Recently, polyimide (PI) has become another emerging electret material due to the excellent electrical, thermal, and mechanical properties.<sup>52–55</sup> Chen and co-workers reported various PI electret n-type OFETs.<sup>55</sup> In this article, new PIs, polyimidothioether[4,4'-(diaminodiphenylsulfide)bismaleimide-2,5-bis(mercaptomethyl)-1,4-dithiane] (PITE(BMI-BMMD)), poly[bis-(4-aminophenyl)-sulfide-bipthalimide] (PI(APS-BPA)), and poly[bis-(4-aminophenyl)-sulfide-oxydipthalimide] (PI(APS-ODPA)), were designed and explored as electrets for n-type  $N,N'$ -bis(2-phenylethyl)perylene-3,4,9,10-tetracarboxylic diimide (BPE-PTCDI) transistor memories.

As shown in Fig. 7, by adjusting the strength of different electron acceptors, the synthesized PI molecules have different charge transfer (CT) capabilities, thereby exploring OFET memory from flash memory to write-once-read-many (WORM) type memory transformation. As shown in Fig. 8, because PITE (BMI-BMMD) has a higher electron-donating capability, it has the highest LUMO energy level among the three, making the device type change from flash memory type to WORM type. Due to the weak electron-withdrawing property of PITE (BMI-BMMD) and the high energy barrier between the LUMOs of PITE (BMI-BMMD) and BPE-PTCDI, this irreversible shift can be explained by the lack of recombination of the trapped holes in the PITE (BMI-BMMD) electret. In addition, PI(APS-BPA) is used as the electret device at an operating voltage of  $\pm 100$  V, showing a memory window of up to 81.49 V and an  $I_{\text{on/off}}$  ratio of  $4.6 \times 10^4$ . As shown in Fig. 8g, PI(APS-BPA) is used as the electret device, which shows the characteristics of the WORM transistor of multi-level storage.

In addition to using the electret material alone as the charge trapping layer, the electret material can also be used in combination with NPs to achieve better charge trapping capabilities. Chen *et al.* reported a p-channel non-volatile OFET memory with an asymmetric PS-*b*-P4VP diblock copolymer layer,<sup>56,57</sup> and added metal nanoparticles with different work functions to it and hydrophilic and hydrophobic fragments. The device structure is shown in Fig. 9a. In the diblock polymer polystyrene-*block*-poly(4-vinylpyridine) (PS<sub>56k</sub>-*b*-P4VP<sub>8k</sub>) layer, the memory window could be adjusted by changing the thickness of the micelle (P4VP-core, PS-shell). As the concentration of the solution increased, the thickness of the deposited film

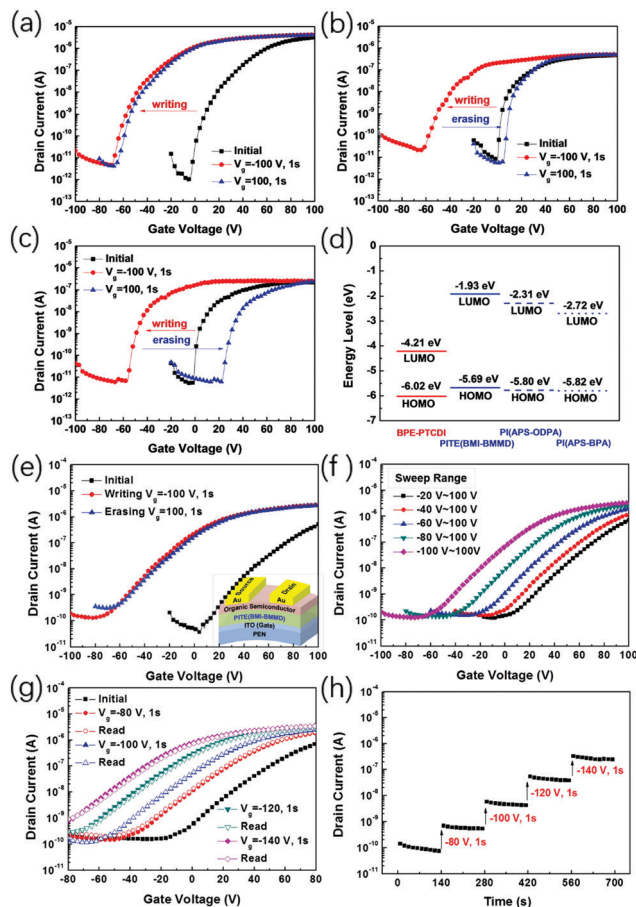
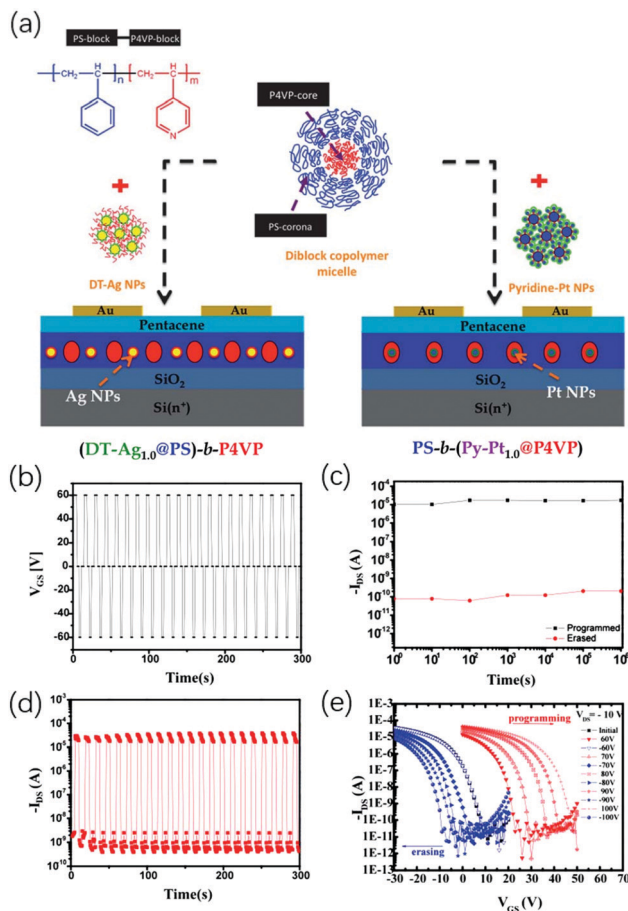


Fig. 8 Transfer curves of the studied polymer electret OFET memory devices using (a) PITE(BMI-BMMD), (b) PI(APS-ODPA), and (c) PI(APS-BPA). All currents were collected under  $V_D = 100$  V. (d) Energy level representation of BPE-PTCDI and the studied PIs. (e) Transfer curves of the studied polymer electret OFET memory using PITE(BMI-BMMD). Transfer characteristics of the device with (f) different sweeping ranges and (g) various programming voltages (solid marks) and the corresponding reading curves (empty marks). (h) The multi-level current responses read at a gate voltage of  $-10$  V when applying various programming gate voltages. All currents were collected under  $V_D = 100$  V. Reproduced with permission.<sup>55</sup> Copyright 2014, John Wiley and Sons.

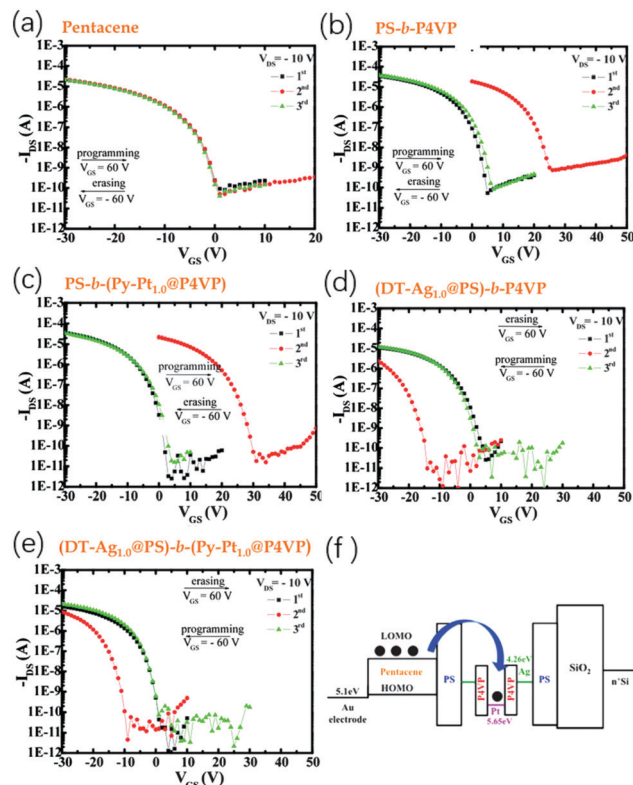
increased, but the memory window decreased from 21 V to 7.8 V. When the thickness of the PS<sub>56k</sub>-*b*-P4VP<sub>8k</sub> layer increased, the distance between P4VP core and PS shell decreased, attributed to the reason why they retained the cap-like structure. On the contrary, the thickness of the PS shell in the in-plane direction decreased, resulting in a decrease of the electron trapping ability of the PS<sub>56k</sub>-*b*-P4VP<sub>8k</sub> and the memory window of the devices. In addition, as shown in Fig. 10, after the addition of high work function Pt NPs, the threshold voltage of the OFET device transfer curve shifts positively, and a larger memory window is generated. Conversely, after adding the low work function Ag NPs, the threshold voltage of the OFET device transfer curve shifts negatively, and a smaller memory window is generated. At the same time, the article also tests the retention capacity and endurance of the added NPs. As shown in Fig. 9, the addition of NPs has no major impact on the



**Fig. 9** (a) Schematic illustration of the device structures of pentacene based OFET memory devices and the distributional positions of DT-Ag and Py-Pt NPs within them. Inset: Chemical structure of the PS-*b*-P4VP copolymer. Reproduced with permission.<sup>57</sup> Copyright 2012, Royal Society of Chemistry. (b) *P/E* bias pulses of  $-60$  V were repeatedly applied to the bottom-gate electrode for 5 s (programming:  $V_G = 60$  V and  $V_D = -10$  V and erasing:  $V_G = -60$  V and  $V_D = -10$  V). (c) The retention time for the 27 nm thick PS<sub>56k</sub>-*b*-P4VP<sub>8k</sub> memory device in the programmed/erased states under ambient conditions at room temperature. The dotted line is the extrapolation of the measurement data, which is used to determine the long-term reliability of the storage devices. (d) The 27 nm thick PS<sub>56k</sub>-*b*-P4VP<sub>8k</sub> thin film is used to realize the reversible switching of the on-off state of the polymer electret OFET memory. (e) Shifts in transfer characteristics at  $V_D = -10$  V for the 27 nm thick PS<sub>56k</sub>-*b*-P4VP<sub>8k</sub> polymer electret OFET memory device, where  $V_G = 60, 70, 80, 90,$  and  $100$  V and  $V_G = -60, -70, -80, -90,$  and  $-100$  V were applied for 3 s for programming and erasing, respectively. Reproduced with permission.<sup>56</sup> Copyright 2013, Royal Society of Chemistry.

retention capacity of the device, and it is still maintained above  $10^6$  s. After multiple *P/E* cycles, there is almost no degradation in device performance. The memory window increases with increasing programming voltage, showing its good application value.

In addition to problems similar to floating gate OFET memory, PEM devices also need reduced operating voltage, increased *P/E* speed, and reduced total power consumption to achieve practical value. To solve this problem, we can build a device by adopting a vertical structure or using light-assisted programming to reduce the operating current and increase the *P/E* speed.



**Fig. 10**  $V_{th}$  shifts in the transfer characteristics of the devices incorporating (a) bare SiO<sub>2</sub>, (b) PS-*b*-P4VP, (c) PS-*b*-(Py-Pt<sub>1.0</sub>@P4VP), (d) (DT-Ag<sub>1.0</sub>@PS)-*b*-P4VP, and (e) (DT-Ag<sub>1.0</sub>@PS)-*b*-(Py-Pt<sub>1.0</sub>@P4VP). (f) Schematic diagram of the carrier tunnelling through the polymer electret into the metal NPs. Reproduced with permission.<sup>57</sup> Copyright 2013, Royal Society of Chemistry.

## 5. Ferroelectric OFET memory

Ferroelectric OFETs (FeOFETs) have been widely used in the field of memory,<sup>58–66</sup> due to their advantages of lossless read-out, low power consumption, and fast operation speed.<sup>67–69</sup> The gate insulator in FeOFETs is made of a ferroelectric material that can be spontaneously polarized. The polarization state of the ferroelectric insulator is changed by applying an external voltage, thereby accurately adjusting the carrier concentration in the channel. Therefore, the “0” and “1” states can be read out with a lossless drain current. The spontaneous polarization of its internal dipole can be expressed by the following formula (4):

$$D = \epsilon_r E + P \quad (4)$$

where  $\epsilon_r$  is the relative permittivity of the dielectric material,  $D$  is the dielectric displacement,  $E$  is the electric field and  $P$  is the polarization.<sup>70</sup>

In 1921, after the discovery of ferroelectricity in Rochelle salt ( $\text{KNa}(\text{C}_4\text{H}_4\text{O}_6)_4 \cdot \text{H}_2\text{O}$ ), people directly recognized the possibility of polarization response technology for memory applications.<sup>71</sup> In 2004, Schroeder *et al.* reported for the first time all organic permanent memory transistors.<sup>58</sup> At that time, the necessary characteristics of low-power-rate memory device applications were shown: under an operating voltage of  $\pm 20$  V, there was a



20 V memory window, and the switch ratio was higher than 200 and the retention time was several hours. This has a positive impact on the continued research of FeOFET memory. For FeOFET memory, the retention time has always been the current primary issue, and non-volatile memory requires that data can be retained for 10 years or longer. Currently, the commonly used organic ferroelectric materials are poly(vinylidene fluoride) (PVDF) (and its copolymers).<sup>67,69,72,73</sup> However, due to the high roughness of the material itself, it will inevitably affect the electrical properties. Through annealing treatment, the ratio of the crystal phase and the ferroelectric phase of the ferroelectric material itself can be improved, the surface roughness and charge leakage can be reduced, and the charge mobility and the  $I_{\text{on/off}}$  ratio can be improved. For example, Lee *et al.* reported a FeOFET memory using pentacene and poly(vinylidene fluoride-co-trifluoroethylene) (PVDF-TrFE) (PVDF-TrFE = 70–30 mol%) as semiconductor and ferroelectric insulators, respectively.<sup>64</sup> In this work, the flat grain structure was obtained by tensile stress and annealing treatment, and the surface roughness and current leakage of the ferroelectric insulating film were greatly reduced.

By inserting an intermediate layer between the interface of the ferroelectric insulating layer and the gate electrode, the leakage current of the FeOFET memory device can also be greatly decreased, and the  $I_{\text{on/off}}$  ratio can be improved.<sup>65,74</sup> For example, Park and co-workers reported a bottom-gate OFET device using ferroelectric poly(vinylidene fluoride-co-trifluoroethylene) (PVDF-TrFE) as a ferroelectric insulating layer and pentacene as a semiconductor layer. The poly(styrene-random-methylmethacrylate) copolymer as an intermediate layer improves the  $I_{\text{on/off}}$  ratio of the device by two orders of magnitude, and the leakage current is reduced to  $10^{-11}$  A. The device structure is shown in Fig. 11a.<sup>65</sup> In this work, by adjusting the thickness of the P(S-*r*-MMA) layer, the roughness of the PVDF-TrFE interface is improved, and the leakage current is reduced. As shown in Fig. 11b–d, with the increase of the thickness, the leakage current decreases significantly. It can be seen that it is an effective solution to introduce an intermediate layer to improve the roughness of the ferroelectric insulating layer and to improve the electrical characteristics of the FeOFET memory device.

Compared with inorganic FET devices, organic FET devices can be solution processed, manufactured over a large area, and can be integrated, which can significantly reduce production costs.<sup>75–78</sup> For example, Takamiya and co-workers reported an OFET memory device using P(VDF-TrFE) and PI precursors as insulating inks and pentacene as a semiconductor layer. By printing, large-area preparation of organic flexible devices is achieved, and the device structure is shown in Fig. 12.<sup>75</sup> After simple packaging, the device retention time could be as long as 5 months, and the  $I_{\text{on/off}}$  ratio remained above  $10^3$ . By integrating two regular FETs and a FeOFET, and simply applying a voltage, the “0” or “1” stored in the IC could be read and retrieved without destroying the data or changing the ferroelectric’s polarization state. In addition, by combining with the most advanced silicon technology, the energy consumption was only  $10^7$  pJ per bit.

As Moore’s law approaches the limit, the market demand for high-density storage is becoming more and more urgent.

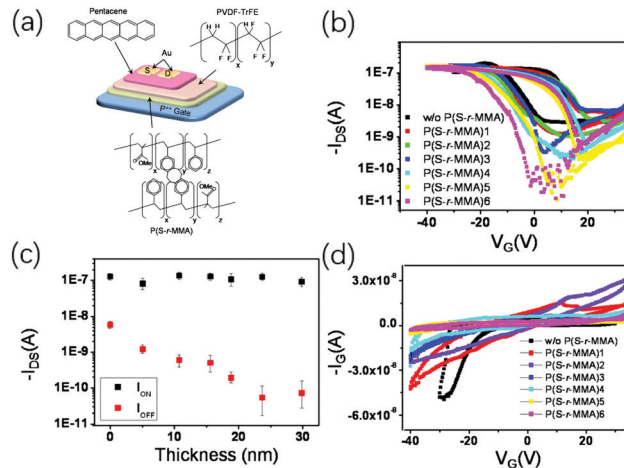


Fig. 11 (a) Schematic illustration of a bottom gate FeFET with pentacene as the active layer and bilayered PVDF-TrFE/P(S-*r*-MMA) as the gate dielectric. (b) Transfer curves ( $I_{\text{D}}-V_{\text{G}}$ ) at  $V_{\text{D}} = 5$  V of pentacene FeFETs with six different P(S-*r*-MMA) interlayers. The transfer curve of the pentacene FeFET without a P(S-*r*-MMA) layer is also plotted for comparison. (c) Plots of  $I_{\text{on/off}}$  as a function of the P(S-*r*-MMA) interlayer thickness. While  $I_{\text{on}}$  remains similar,  $I_{\text{off}}$  gradually decreases with the interlayer film thickness up to approximately 25 nm. (d)  $I_{\text{G}}-V_{\text{G}}$  characteristics of the FeFETs simultaneously obtained with the transfer characteristics showing that the gate leakage current becomes significantly reduced with the thickness of the interlayer. Reproduced with permission.<sup>65</sup> Copyright 2009, Elsevier.

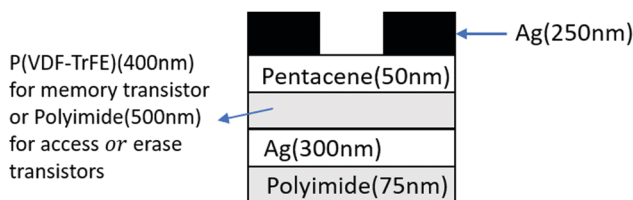
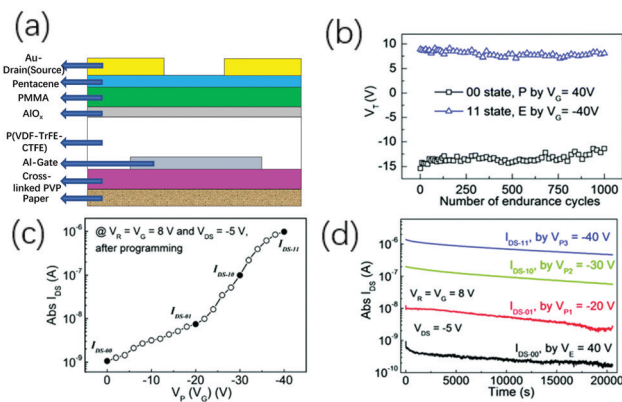


Fig. 12 Schematic diagram of ferroelectric transistors and printed transistors.

Although it can be achieved by reducing the size of the device and performing 3D stacking,<sup>72</sup> both methods need complicated and expensive micro/nano processing technology. Another strategy is multi-level storage.<sup>55,79–81</sup> For example, Wang and co-workers reported a multi-level OFET memory device using ferroelectric tripolymer poly(vinylidene-fluoride-trifluoroethylene-chlorotrifluoroethylene) [P(VDF-TrFE-CTFE)] as a ferroelectric insulating layer and pentacene as a semiconductor layer, and the device structure is shown in Fig. 13a.<sup>82</sup> In this work, the channel conductance is modulated by changing the magnitude of the gate voltage. Taking 40, –20, –30 and –40 V as “00”, “01”, “10” and “11” states, respectively, the device realizes multi-level storage, as shown in Fig. 13d. The multi-level storage function was mainly attributed to the controllable dipolarization of the ferroelectric terpolymer P(VDF-TrFE-CTFE). In addition, the article also tests its retention time and endurance. It has very reliable and consistent 4-level data storage within 1000  $P/E$  cycles, as shown in Fig. 13b and c.

Ferroelectric materials have the advantages of good stability, short  $I_{\text{on/off}}$  time and large  $I_{\text{on/off}}$  ratio. However, similar to the floating gate structure, as the thickness of the ferroelectric film

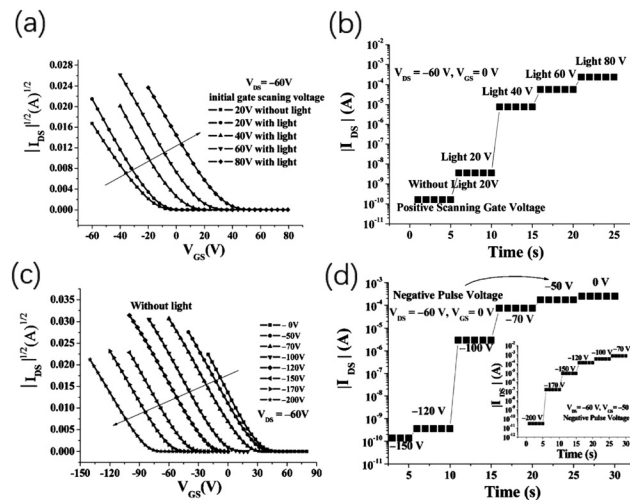


**Fig. 13** (a) Schematic illustration of the multi-level OFET-NVM fabricated on a paper substrate. (b)  $P/E$  switching endurance cycles between the 00 and 11 states, indicated by the programming and erasing  $V_{th}$ , respectively. (c) Time dependent data retention curves. (d) Reading  $I_D$  achieved at a reading state of  $V_R = V_G = +8$  V and  $V_D = -5$  V after various programming  $V_G$  values ranging from 0 to  $-40$  V with an increase step of  $-2$  V, respectively. Four different  $I_D$  results ( $I_{D-00}$ ,  $I_{D-01}$ ,  $I_{D-10}$  and  $I_{D-11}$ ) of  $V_G$  at  $-40$ ,  $-20$ ,  $-30$  and  $-40$  V are used for the four different states of multi-level memory. Reproduced with permission.<sup>82</sup> Copyright 2019, Royal Society of Chemistry.

decreases, the depolarization effect becomes stronger, and the memory window is greatly reduced. Moreover, ferroelectricity may also be adversely affected by other factors, and the charge may be trapped inside the ferroelectric or at the interface defect layer, and the retention time may be reduced. Therefore, it is necessary to manufacture new types of ferroelectric devices and develop new types of ferroelectric materials to break through these limitations. For example, by constructing a junctionless FET, the size of the device is greatly reduced. Therefore, the device can bypass the unfavorable factor that the depolarization effect becomes stronger due to the reduced thickness of the ferroelectric layer, and this structure can also reduce the influence of external factors. In addition, the method of plasma treatment at the interface can greatly improve the interface defects, thereby increasing the retention time of the device.

## 6. Optoelectronic OFET memory

An OFET device is a three-terminal device, so it has the potential to expand sensory stimulation, such as photon memory,<sup>83–86</sup> thermal memory,<sup>87</sup> and tactile memory.<sup>88,89</sup> Similar to the voltage between the gate and the source, the photo-generated carriers in the floating gate layer form an additional internal electric field that affects the carriers in the conductive channel. Due to the adjustability of the light intensity, photon storage devices have developed rapidly in multi-level storage,<sup>79,83,84,90–92</sup> wearable sensors<sup>93</sup> and other applications. For example, Liu and co-workers reported a multi-level storage device using PS or PMMA as a modified layer (modified  $\text{SiO}_2$ ) and pentacene or copper phthalocyanine (CuPc) as a semiconductor layer.<sup>83</sup> Under light-assisted program, through 20 V, 40 V, 60 V, and 80 V programming operations on the memory device, the device achieved 5-level storage and kept stable over 100 cycles of testing, as shown in Fig. 14. Conversely, if there is no light-assisted



**Fig. 14**  $I-V$  curves of devices with light-assisted programming (the initial scanning gate voltage is  $V_{G,Start} = 20$  V, 40 V, 60 V, and 80 V,  $V_D = -60$  V, and with the visible-light intensity increased with the arrowhead). (a)  $|I_D|^{1/2}$  versus  $V_G$  and (b) the corresponding different current levels at  $V_G = 0$  V and  $V_D = -60$  V in the process for OFETs with a PS modifying layer. (c) Different transfer characteristics of the devices using voltage programming ( $V_{G,Pro} = -50$  V,  $-70$  V,  $-100$  V,  $-120$  V,  $-150$  V,  $-170$  V, and  $-200$  V,  $V_D = 0$  V,  $t = 1$  ms) without light, and (d) the corresponding different current levels at  $V_G = 0$  V,  $V_D = -60$  V and  $V_G = -50$  V,  $V_D = -60$  V (inset graph) in the process. Reproduced with permission.<sup>83</sup> Copyright 2009, John Wiley and Sons.

condition, a programming voltage of up to  $-200$  V is required to achieve 5-level storage. Naito and co-workers further demonstrated a light-assisted programming multi-level storage device using TIPS-PEN as a floating gate capture layer and P3HT as the semiconductor layer.<sup>90</sup> The memory window of the device was greater than 30, and the retention time was longer than  $10^6$ , as shown in Fig. 15. The experimental results showed that the memory window of the optoelectronic OFET memory mainly depended on the photocarrier generation efficiency of the organic semiconductor and the charge storage capacity of the floating gate. In addition, unlike the Liu group, it was proved in this article that multi-level storage could be realized only by changing the light intensity, and the light only had the function of assisting programming, not the function of assisting erasure.

Although multi-level storage can be realized with the aid of optical-assisted programming, the span of the light intensity is large, which limits the further development of optoelectronic storage devices. Fundamentally speaking, this is mainly because of the low light responsiveness of light-responsive materials, so it is urgent to find materials with high responsiveness. As we all know, inorganic perovskite quantum dots (QDs) have excellent light responsiveness and charge trapping ability.<sup>94,95</sup> Mixing them with organic semiconductors may produce good performance. Yang and co-workers demonstrated a vertical optoelectronic storage device based on a mixture of poly[1,2,5]thiadiazolo[3,4-*c*]pyridine-4,7-diyl[(4,4-dihexadecyl-4*H*-cyclopenta[2,1-*b*:3,4-*b'*]dithiophene-2,6-diyl)[1,2,5]thiadiazolo[3,4-*c*]pyridine-7,4-diyl[(4,4-dihexadecyl-4*H*-cyclopenta[2,1-*b*:3,4-*b'*]dithiophene-2,6-diyl) (PCDTPT) and inorganic perovskite QDCsPbBr<sub>3</sub>. The device structure is shown in Fig. 16a.<sup>79</sup> The vertical structure enables the device to have

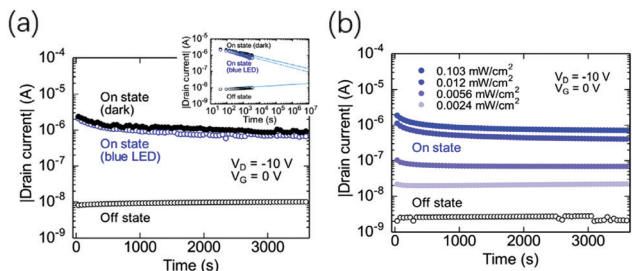


Fig. 15 (a) Retention curves of drain currents measured at  $V_G = 0$  V and  $V_D = -10$  V in the dark and under blue light illumination (469 nm,  $1.06 \text{ mW cm}^{-2}$ ) before and after programming with blue light. (b) Retention curves measured in the dark before and after programming ( $V_G = +60$  V, 3 s) with blue light at different intensities. Reproduced with permission.<sup>90</sup> Copyright 2019, Elsevier.

ultra-short channels and good gate voltage control capabilities, thereby effectively reducing the leakage of trapped charge, reducing the erase voltage, speeding up the electrical erasing speed, and increasing the retention time of the device.

By the close combination of organic semiconductors and inorganic perovskite quantum dots, the optoelectronic memory realizes 8-level storage with low light intensity ( $0.05\text{--}0.5 \text{ mW cm}^{-2}$ ), and it has a large memory window of 66.5 V with a retention time of up to  $10^8$  s, and the device remains stable during more than 1000  $P/E$  cycles, as shown in Fig. 16b and c.

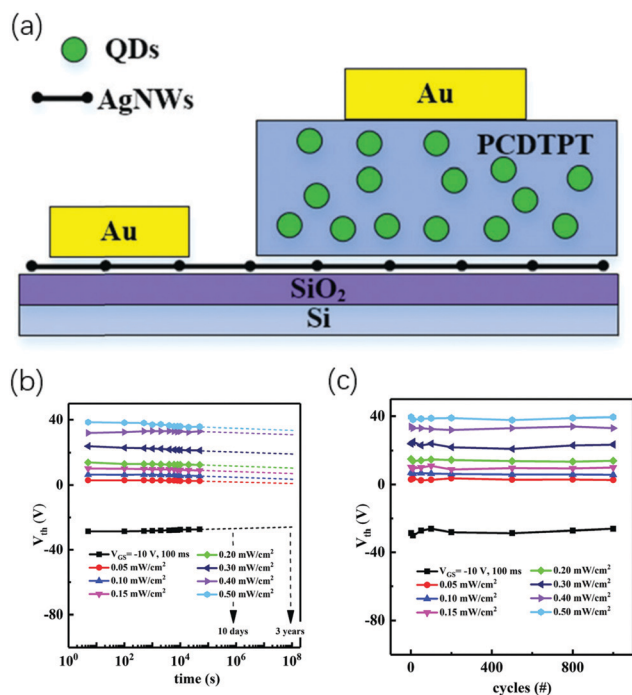


Fig. 16 (a) Schematic illustration of the photonic memory transistor. The retention curves of  $V_{th}$  (b) and the endurance curves of  $V_{th}$  (c) of photonic memory devices after light programming under light illumination (300 nm) with different light intensities for 0.5 s and after electric erasing with gate bias  $V_G = -10$  V for 100 ms. Reproduced with permission.<sup>79</sup> Copyright 2020, Royal Society of Chemistry.

In addition, it should be noted that if the mixing ratio of perovskite quantum dots is too high, aggregated perovskite quantum dots will be formed, and photo-generated electron pairs will rapidly recombine, affecting the device's light responsiveness and reducing the retention capacity.

Under the action of light, organic materials can undergo a variety of reversible bistable processes, such as photochromic reactions, photothermal phase transitions, and photothermal aggregation state transitions. Although these organic reversible bistable processes can be used for NVM devices, due to defects such as poor stability, low durability and long response times, they cannot meet industrial needs. However, Leydecker *et al.* reported an OFET memory device using P3HT and photochromic diarylethene blended as a semiconductor layer, as shown in Fig. 17a and b.<sup>84</sup> By modulating the photo-cyclization bistable process, the DAE-Me-o and DAE-Me-c structures are interchanged to optically control the electrical transmission. Under light of 313 nm, the HOMO energy level of DAE-Me-c is located within the band gap of P3HT and can accept holes. The HOMO energy level of the open DAE-Me-o is outside the P3HT band gap. Under illumination of 546 nm, the captured holes will be released. This allows up to 256 (8-bit) different current levels, and a minimum of 3 ns laser illumination to switch its storage state. In addition, the device had a durability of more than 70  $P/E$  cycles and a retention time of more than 500 days. This work demonstrated the good application of photochromic molecules in optoelectronic OFET memory.

In addition to using a variety of optoelectronic materials and organic semiconductor doping to improve the performance of optoelectronic OFET devices, a variety of devices combined together can also draw on their respective strengths to create

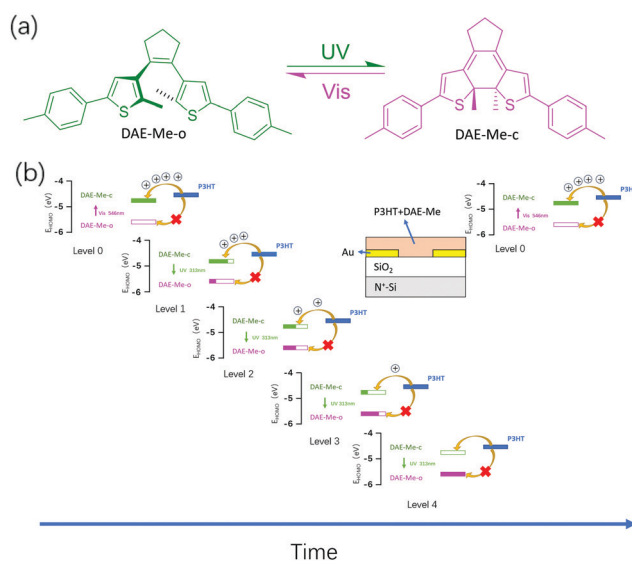
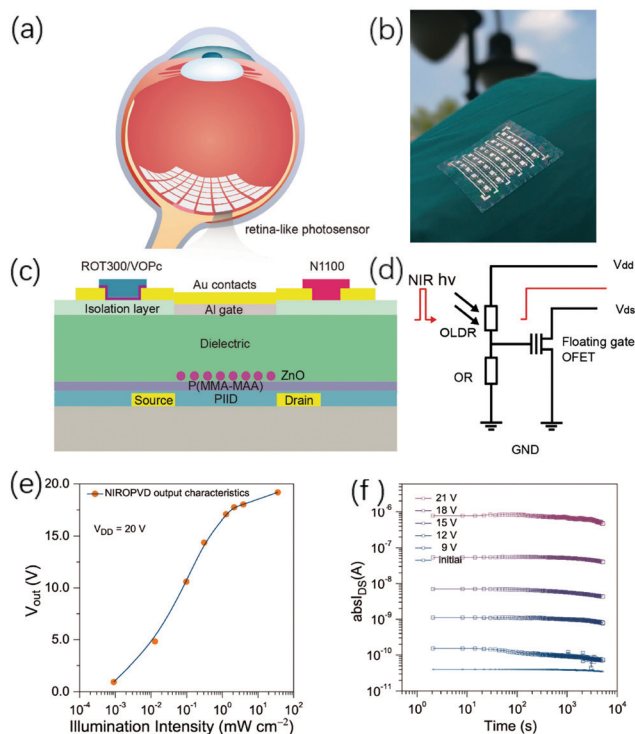


Fig. 17 (a) Chemical structure of the used DAE, in its open and closed form. (b) Middle: Structure illustration of the devices on a SiO<sub>2</sub> substrate. Schematic diagram of a multi-level storage device. With the increase of the 313 nm ultraviolet light irradiation time, the device gradually changed from level 0 to level 4, and then by 546 nm visible light irradiation, the device returned to level 0.



**Fig. 18** (a) Schematic illustration of a mammalian eye's imaging process. Cone cells absorb photons and convert them into signals in the form of energy, which are transmitted to the brain through the optic nerve. (b) Photograph of the as-fabricated, retina-like photosensor array attached to nitrile gloves. (c) Cross-sectional schematic illustration of the retina-like photosensor, which indicates the active layers' composition. (d) Electric illustration of an organic retina-like photosensor. Under NIR (850 nm) irradiation, the photosensor is capable of transmitting optical signals into OFET memory. (e) Output curves of a NIR voltage divider as a function of NIR incident light intensity. (f) Retention time tests of the programmed states. A conductance range of nearly  $10^4$  is obtained in the intermediate states. Reproduced with permission.<sup>91</sup> Copyright 2017, John Wiley and Sons.

devices with better performance. Liu and co-workers demonstrate a new type of circuit that integrates photosensitive devices with floating gate OFET memory, which has a sharp colour recognition capability. The device structure and equivalent circuit are shown in Fig. 18c and d.<sup>91</sup> The device provided two readout channels (p-type memory and n-type switch) to distinguish colours. The minimum reading voltage was  $-1$  V, and the on/off state switching required only 100 nW of energy consumption, and it had a high  $I_{\text{on/off}}$  ratio of  $10^5$  and a retention time of  $10^6$ . In addition, due to the application of photosensitive materials in the voltage divider, the device can achieve multi-level storage under different lighting conditions, as shown in Fig. 18e and f. This work is a good demonstration of the integration of optoelectronic OFET memory with other circuits.

The importance of optoelectronic OFET memory devices is not only reflected in multi-level information storage, but also in optical data recording systems.<sup>96–98</sup> Ren *et al.* reported a photovoltaic device using an air-stabilized organic semiconductor dinaphtho-[2,3-*b*:2',3'-*f*]thieno[3,2-*b*]thiophene (DNIT) (3 eV) with a large band gap as the active layer material and PS/SiO<sub>2</sub>

as the mixed dielectric.<sup>98</sup> By combining lighting with  $V_{\text{GS}}$ ,  $I_{\text{DS}}$  shows a change on the order of  $10^7$ , with a dynamic range of up to 23 bits and a light sensitivity of  $420 \text{ A W}^{-1}$ , which can be directly used in multi-level data storage devices and optical sensors. In conventional phototransistors or photodiodes, they can provide a direct response to light input without information storage characteristics. In this paper, the authors used a large band gap active layer to inject these photo-excited charges into the electret through the applied  $V_{\text{GS}}$ . In addition, the amount of trapped charge could be further controlled by adjusting the intensity of incident light at a specific  $V_{\text{GS}}$ . The long retention time of the charges in the electret layer made these devices usable as optical memories, and multi-level information storage could be achieved by changing the light intensity.

As demonstrated previously, this excellent optoelectronic device research has made significant contributions to the development of optoelectronic OFET memories, but currently optoelectronic devices still have some major challenges: (1) better durability; (2) having good sensitivity in the  $P/E$  process; (3) having good stability at room temperature; and (4) there are few light-responsive materials for a broadband spectrum.

## 7. Conclusions and outlook

In the past few decades, OFET memory has experienced rapid development, with the introduction of various design and implementation methods, and great efforts have been made to realize industrial applications. OFET-based memory has developed tremendously due to its good stability, relatively controllable test parameters and clear operating mechanism. We have discussed the latest advances in OFET-based memories, including floating gate OFET memories, electret OFET memories, ferroelectric gate OFET memories, and optoelectronic OFET memories. Table 2 lists a comparison of various types of OFET memory. Each memory device has its own advantages and disadvantages. Floating gate OFET memories usually have large  $I_{\text{on/off}}$  ratios and controllable and stable channel conductance, but these devices usually require larger operating voltages. Although the operating voltage can be reduced by reducing the thickness of the insulating layer and the high- $\kappa$  insulating medium, this will cause stability problems. These problems may be solved by using vertical structures or electret materials combined with floating gate structures. Electret OFET memory has a similar situation to floating gate OFET memory, and the  $P/E$  speed also needs to be improved. The use of light-assisted programming or vertical structures may be the key to solving these problems. Ferroelectric OFET memory has the advantages of good stability, short  $I_{\text{on/off}}$  time, and large  $I_{\text{on/off}}$  ratio. However, similar to the floating gate structure, as the thickness of the ferroelectric film decreases, the depolarization effect becomes stronger, and the memory window is greatly reduced. Moreover, ferroelectricity may also be adversely affected by other factors, and the charge may be trapped inside the ferroelectric or at the interface defect layer, and the retention time may be reduced. The use of a junctionless FET

Table 2 Materials and performance comparison of different types of OFET memories

	Materials	W/L ( $\mu\text{m}$ )	P/E (V)	$V_{\text{th}}$ (V)	$I_{\text{on/off}}$ speed	Retention time (s)	$I_{\text{on/off}}$	Energy consumption	Ref.	
Floating gate OFET memory	Semiconductor:P3HT; Floating gate:Au NPs	1000/30	$\pm 50$	18	N/A	200	28	N/A	26	
	Semiconductor:F8T2; Floating gate:Au NPs	1000/20	$\pm 70$	40	N/A	N/A	$10^3$	N/A	35	
	Semiconductor: P(NDI2OD-T2); Floating gate:Au NPs	1000/10	$\pm 80$	52	N/A	$10^7$	$10^3$	N/A	36	
	Semiconductor:pentacene; Floating gate:ZnO NPs	2500/50	$\pm 100$	N/A	N/A	200	N/A	N/A	37	
	Semiconductor:pentacene; Floating gate:ferritin nanoparticle	800/100	$\pm 20$	7.14	1 s	$10^4$	130	N/A	38	
	Semiconductor:pentacene; Floating gate:C NPs	750/50	$\pm 80$	35	N/A	$10^6$	$10^3$	N/A	42	
	Semiconductor:pentacene; Floating gate:PFBT	1000/50	$\pm 50$	35	N/A	$10^4$	$10^4$	N/A	43	
	Semiconductor:P3HT; Floating gate:TIPS-PEN	1000–100	$\pm 40$	14	N/A	5000	350	N/A	44	
	Semiconductor:pentacene; Floating gate:Poly-Si	4000–240	$\pm 60$	9.8	0.1 s	200	100	N/A	47	
	Polymer electret OFET memory	Semiconductor:pentacene; Electret: PS	4000/50	$\pm 70$	22.1	10 s	$5.2 \times 10^6$	$10^6$	N/A	52
		Semiconductor:pentacene; Electret: PzMs	4000/50	$\pm 70$	26.0	10 s	$2.2 \times 10^6$	$10^5$	N/A	52
		Semiconductor:pentacene; Electret: P4Ms	4000/50	$\pm 70$	24.1	10 s	$2.1 \times 10^6$	$10^5$	N/A	52
		Semiconductor:pentacene; Electret: PVP	4000/50	$\pm 70$	17.0	10 s	$0.24 \times 10^6$	$10^5$	N/A	52
		Semiconductor:pentacene; Electret: PVPy	4000/50	$\pm 70$	21.0	10 s	$0.42 \times 10^6$	$10^5$	N/A	52
Semiconductor:pentacene; Electret: PVN		4000/50	$\pm 70$	27.8	10 s	$3.4 \times 10^6$	$10^6$	N/A	52	
Semiconductor:pentacene; Electret: PVA		4000/50	$\pm 70$	Negligible	10 s	N/A	$10^5$	N/A	52	
Semiconductor:BPE-PTCDI; Electret:PITE(BMIBMMD)		4000/50	$\pm 70$	64.4	N/A	$10^5$	$9.0 \times 10^5$	N/A	56	
Semiconductor:BPE-PTCDI; Electret:PI(APS-ODPA)		4000/50	$\pm 70$	61.2	N/A	$10^5$	$9.3 \times 10^4$	N/A	56	
Semiconductor:BPE-PTCDI; Electret: PI(APS-BPA)		4000/50	$\pm 70$	81.5	N/A	$10^5$	$4.6 \times 10^5$	N/A	56	
Semiconductor:pentacene; Electret:PS <sub>56k</sub> -b-P4VP <sub>8k</sub>		2000/250	$\pm 60$	21.1	N/A	$10^6$	$10^5$	N/A	58	
Semiconductor:pentacene; Electret:PS-b-(Py-Pt <sub>1,0</sub> @P4VP)		2000/250	$\pm 60$	26.4	N/A	$10^6$	$10^5$	N/A	57	
Ferroelectric OFET memory		Semiconductor:pentacene; Ferroelectric materials:P(VDF-TrFE); Middle layer material: P(S-r-MMA)	300/30	$\pm 40$	—	N/A	5 months	$10^5$	$10^7$ pJ per bit	76
		Semiconductor:pentacene; Ferroelectric materials:P(VDF-TrFE); Middle layer material: P(S-r-MMA)	200/50	$\pm 90$	45.6	N/A	N/A	$10^3$	N/A	66
	Semiconductor:pentacene; Ferroelectric materials:P(VDF-TrFE-CTFE)	1000/100	$\pm 40$	25	1 s	$2 \times 10^4$	N/A	N/A	83	
Optoelectronic OFET memory	Semiconductor:pentacene; Electret:PS or PMMA	3000/50	0–80 light assist	55	2 s	$2 \times 10^4$	$10^6$	N/A	84	
	Semiconductor:P3HT; Floating gate:TIPS-PEN	1200/10	$\pm 60$ light assist	> 30	3 s	$10^6$	$10^5$	N/A	91	
	Semiconductor:PCDTPT; QDs:CsPbBr <sub>3</sub>	Length: 0.05, Width: N/A	–10 light assist	66.5	0.1 s	$10^8$	$10^4$	N/A	80	
	Semiconductor:P3HT; Dopant:DAE-Me-o	10 000/20	–60–20	—	3 ns	500 days	N/A	N/A	85	

Table 2 (continued)

Materials	W/L ( $\mu\text{m}$ )	P/E (V)	$V_{\text{th}}$ (V)	$I_{\text{on/off}}$ speed	Retention time (s)	$I_{\text{on/off}}$	Energy consumption	Ref.
Semiconductor:PIID; Photosensitive material:ROT300/ VOPc	4500/50	$\pm 15$	5	1 s	$10^6$	$10^4$	100 nW	92
Semiconductor: DNNT; Photosensitive material: DNNT	2000/100	$\pm 150$	63.7	10 s	$10^7$	$10^5$	N/A	98

structure or plasma treatment may have unexpected effects. Compared with traditional non-volatile memory, an important advantage of optoelectronic OFET memory is that it is more convenient for multi-level data storage. When performing multi-level data storage, because each state is close, the first consideration is to ensure the stability of the state. Electret memory can show multi-level storage capacity under different programming voltages, but it is easy to cause incorrect reading and data loss; Meanwhile, multi-level ferroelectric memory is based on different polarization states, and the stability of the state is even worse. An optoelectronic OFET device can be optically programmed and electrically read out, which effectively improves the stability of the state. Therefore, these years have made great progress. But there are still some challenges in future applications: (1) good durability; (2) good sensitivity in the P/E process; (3) good stability at room temperature; and (4) few light-responsive materials for a broadband spectrum. Therefore, future research needs to address these weaknesses of OFET memory to achieve high-performance memory devices. All in all, with the rapid development of new organic materials and the rational design of device structures, high density, long retention time, fast  $I_{\text{on/off}}$  speed and long endurance OFET memory will become a major complement to flexible, wearable non-volatile memory.

## Conflicts of interest

There are no conflicts to declare.

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