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Cite this: *Mater. Horiz.*, 2024, 11, 949

Received 3rd November 2023,
Accepted 1st December 2023

DOI: 10.1039/d3mh01834b

rsc.li/materials-horizons

3D simulation of conductive nanofilaments in multilayer h-BN memristors *via* a circuit breaker approach

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A 3D simulation of conductive nanofilaments (CNFs) in multilayer hexagonal-BN memristors is performed. To do so, a simulation tool based on circuit breakers is developed including for the first time a 3D resistive network. The circuit breakers employed can be modeled with two, three and four resistance states; in addition, a series resistance and a module to account for quantum effects, by means of the quantum point contact model, are also included. Finally, to describe real dielectric situations, regions with a high defect density are modeled with a great variety of geometrical shapes to consider their influence in the resistive switching (RS) process. The simulator has been tuned with measurements of h-BN memristive devices, fabricated with chemical-vapour-deposition grown h-BN layers, which were electrically and physically characterized. We show the formation of CNFs that produce filamentary charge conduction in our devices. Moreover, the simulation tool is employed to describe partial filament rupture in reset processes and show the low dependence of the set voltage on the device area, which is seen experimentally.

New concepts

In this manuscript we present a new 3D memristor simulator based on circuit breakers (CBs). Previous simulators are 2D; therefore, it means a step forward in the description of memristor operation and the resistive switching processes. The CBs can be switched between different resistance values depending on the voltage between their terminals or on the CB temperature. By means of these mechanisms, which reflect the physics and chemistry involved in the operation of memristors, we are able to reproduce experimental data obtained in h-BN memristors and describe the conductive nanofilament formation and rupture that make the device operate. Moreover, we can reproduce reset processes where the current *versus* voltage curve presents several steps (partial nanofilament rupture). We can also describe defect regions in the dielectric (our simulation domain), allowing the study of pristine dielectrics and the corresponding resistive switching operation. The particularities of 2D materials (in this case, the dielectric of our devices is hexagonal boron nitride) have been considered in the simulator and they helped to understand the operation and experimental measurements of our devices.

I. Introduction

Memristive devices have been intensively studied in Academia and industry in the last decade.[1–3] These devices show great potential both for standalone and embedded non-volatile memory applications;[4–8] in fact, they have already been incorporated in different industrial products.[3] Their features make them fit the market needs (in general, as storage-class memory) and they are CMOS fabrication technology compatible (some memristive devices have a $4F^2$ footprint, where "F" is the minimum technology half-pitch).[8]

Although memristor-based non-volatile memory applications are the most commercially advanced,[9–11] these devices play an important role in other fields such as neuromorphic computing.[12–21] The neuromorphic engineering approach[22] allows the acceleration of matrix-vector multiplication (a key operation in Artificial Intelligence (AI) algorithms) that can be implemented through memristive device crossbar arrays.[3,17] This approach can get over some of the hurdles of von Neumann's bottleneck, which are linked to the constant data movement between the memory and the processor. Memristive devices, in this neuromorphic computing context, mimic biological synapses to permit the fabrication of hardware neural networks.[12–16,18–20,23] In this respect, due to the inherent redundancy of neural circuits, the device requirements do not need to be as strict as in non-volatile memory applications since AI methodologies allow a greater margin of variability and endurance.[17]

Resistive switching memristors are fabricated with a thin layer of dielectric sandwiched between metal electrodes; their

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electrical and thermal features are closely linked to the materials employed. Different authors have described switching and charge conduction making use of the dynamics of metallic ions, oxygen vacancies and other defects, whose concentration evolves with time in the device active part.[24–30] In particular, for filamentary conduction, the formation and destruction of CNFs is a stochastic process that leads to cycle-to-cycle (C2C) variability.[6,7,31–33] This inherent variability (in addition to device-to-device (D2D) variability[31]) has to be minimized for memory applications; however, it could be beneficial in some cases for deep neural network training to avoid overfitting.[34] Variability is key for hardware cryptography (an entropy source that allows the fabrication of physical unclonable functions and random number generators).[35–39] C2C variability is linked to CNF morphological changes in each RS cycle, where the CF is created (set process) and ruptured (reset process) successively.[24–26,29,30] The device C2C and D2D variability, and switching dynamics can be tackled from different simulation and modeling approaches, such as kinetic Monte Carlo (kMC) simulation,[24,26,28,40,41] advanced statistical modeling[42,43] and compact modeling (for circuit simulation and design).[2,44–50] A different approach, although complementary, is based on RRAM simulation by means of circuit breakers (CB).[7,51–56] These CB-based simulators are bidimensional; nevertheless, a 3D approach is needed if CNFs (in the case of filamentary operation) are to be described correctly, see ref. 57 for a study on the appropriateness of a 3D description in comparison with a 2D approach based on a kMC simulation tool. CB-based simulation poses a numerical technique in between kMC and compact modeling for circuit simulation in what is referred to as complexity, although it allows a reasonable description of variability and current *versus* voltage curves.

In this work, we present a 3D CB-based simulator that can describe the CNF evolution (that facilitates RS operation) and the charge transport in the filamentary operation regime. Apart from common features for these CB-based simulation tools,[7,51–54] we include quantum effects implemented through the quantum point contact model, the use of circuit breakers with four conductivity stages and a device series resistance. We also consider 3D regions of different shapes within the simulator domain to model dielectric zones with high defect density formed at the fabrication stage that evolve as the RS unfolds. This latter feature is hardly ever taken into consideration in simulation tools.

We have tuned our simulator making use of experimental measurements from hexagonal boron-nitride memristive devices[58] that we have fabricated. The devices characterized here have been studied previously,[18,59] and physical and electrical experimental characterization was employed. Devices with some similarities in the layer stack were also analyzed from different viewpoints.[60] All these works were purely experimental. In this work, we present an analysis where a strong simulation approach was introduced. The 3D modeling employed was implemented by means of a new CB-based simulator that allows the assessment of different physical effects on the RS operation and the role of high defect density regions in the dielectric on device variability and reliability.

It is important to draw attention to the fact that there exist different physical characterization techniques to visualize

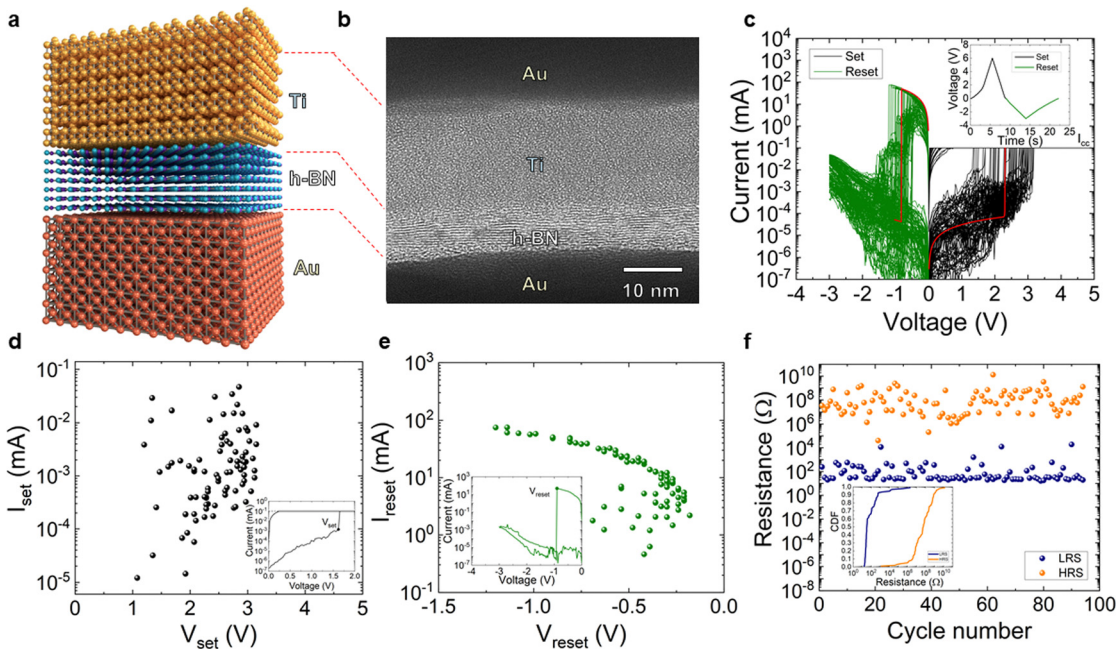

Fig. 1 (a) Device layer scheme, (b) cross-section TEM image of the dielectric and surrounding layers in the device stack. In the h-BN dielectric, we have approximately 18 layers that were transferred from Cu foils. (c) Current *versus* voltage measured in the ramped voltage stress operation regime; see the voltage *versus* time signal in the inset. (d) Set current *versus* set voltage for the curves shown in (c); the set point definition is shown in the inset. (e) Reset current *versus* voltage for the *I*–*V* curves in (c); in the inset is shown the criterion established to define the reset voltage. (f) HRS and LRS resistance values *versus* cycle number in the resistive switching series obtained in (c) (the data are read at 0.1 V). Inset: Cumulative distribution function (CDF) of the HRS and LRS resistance values.

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conductive nanofilaments.[61–63] They are based on the use of conductive atomic force microscopy (C-AFM) and transmission electron microscopy (TEM). These techniques allow outstanding analyses that give us information about the CNF composition, size, shape, charge transport features, *etc.* This information can be used in the development of models and simulation tools. They are also important for the model and simulator calibration, in addition to electrical measurements. Once the simulators are tuned, they can complement C-AFM and TEM by providing an exact map of the temperature and the electric field in the simulation domain (usually the dielectric, although it could include the electrodes), the progress in the CNF formation, the influence of high defect density regions on RS, quantum effects, and charge transport processes.

The measurements have been correctly fitted and different operational particularities have been explained in full. In particular, in Section II, we introduce the fabrication and measurement details; the simulator description is presented in Section III and the results and discussion is given in Section IV. Finally, the main conclusions are drawn in Section V.

II. Device fabrication and measurement setup

The memristive devices used in our study have been introduced previously.[18] The electrodes are made of a bilayer of 40 nm Au/10 nm Ti (E-beam evaporation is employed). The bottom electrode is deposited on a Si wafer, with 300 nm SiO_2 on top of the Si. Then, a h-BN multilayer (18 layers approximately, see Fig. 1a and b) film was placed on top of the bottom electrode by wet transfer from a Cu foil where it was grown by chemical vapor deposition. In Fig. 1c, RS *I–V* curves are shown. They are obtained with a B1500A Keysight semiconductor parameter analyzer and a probe station (Karl Suss); ramped voltage stress (RVS) is used for the measurement of long RS series with consecutive set and reset cycles. RS operation is filamentary.[18]

In Fig. 1d and e, we plot the set and reset parameters, and the low and high resistance states (LRS/HRS) are plotted in Fig. 1f. It is clear that the resistance ratio (R_{HRS}/R_{LRS}) allows non-volatile memory applications (see the cumulative distribution functions of R_{HRS} and R_{LRS} in the inset in Fig. 1f, a reasonable variability is obtained).

It is interesting to highlight that CVD grown polycrystalline h-BN multilayers, such as the one employed here, work well for RS devices since they include insulating 2D layered regions and clusters of defects that are more conductive (these clusters of defects may be related to lattice distortions that propagate from one layer to another[60,64]). Other options, such as exfoliated h-BN, do not exhibit RS.[65]

III. Simulator description

The simulation tool that we developed, based on CBs, allows the analysis of RRAM RS, charge conduction and variability. CNF creation and destruction can be modeled to describe both unipolar and bipolar device operations. A 3D approach is followed, and therefore, it means a step forward with respect to 2D CB tools[7,51–55] (see Fig. 2a). Following the simulation scheme unfolded in ref. 55, CBs with several conductance levels are included (Fig. 2b). Quantum effects in the charge

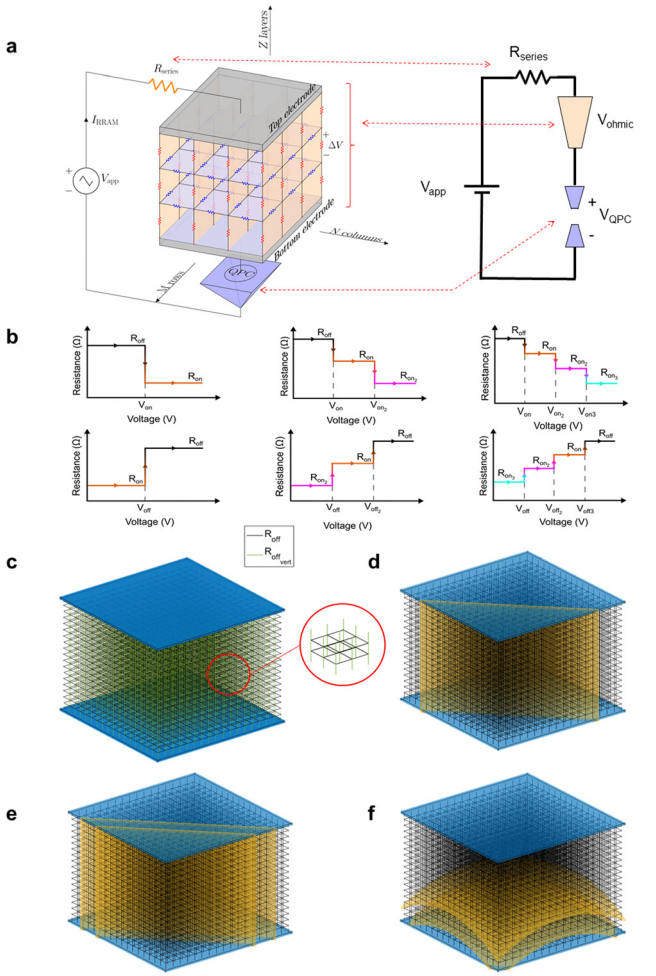

Fig. 2 (a) Schematics of the 3D CB network diagram that depicts the internal electric circuitry included in the simulator to model the device. The horizontal CBs symbolize B vacancies embedded within the percolation path. The CBs are differentiated by blue and red colors, describing conduction in the h-BN layers (with lower associated resistances) and in the perpendicular direction of the BN planes (corresponding to much higher resistance in our model). The top and bottom electrodes are connected to an external voltage source. The model includes a series resistance that accounts for the metal pads and electrode resistances, and it is obviously in series with the resistance network that represents the dielectric. Quantum effects related to potential barriers along the charge conduction path are taken into consideration by means of the QPC model. A single module for the QPC model is employed in series with the resistance network. (b) The CB internal resistance values for the set (or forming) process are categorized into two levels (R_{off} and R_{on}), three levels (R_{off}, R_{on}, and R_{on2}) and four levels (R_{off}, R_{on}, R_{on2}, and R_{on3}). Similarly, for the reset process, the CB internal resistance structure is described for two, three or four levels. (c) Schematic of the 3D CB network incorporating two types of CBs to address the resistivity in-layer and out-of-layer in the h-BN. In this case, the horizontal CBs are represented in black, while the vertical CBs are denoted in green to better visualize them. (d) 3D CB network including a 2D vertical plane (in yellow) to model a region with a higher defect density, (e) 3D vertical plane and (f) a 3D curved plane in the CB domain to represent regions of different shapes with a higher defect density.

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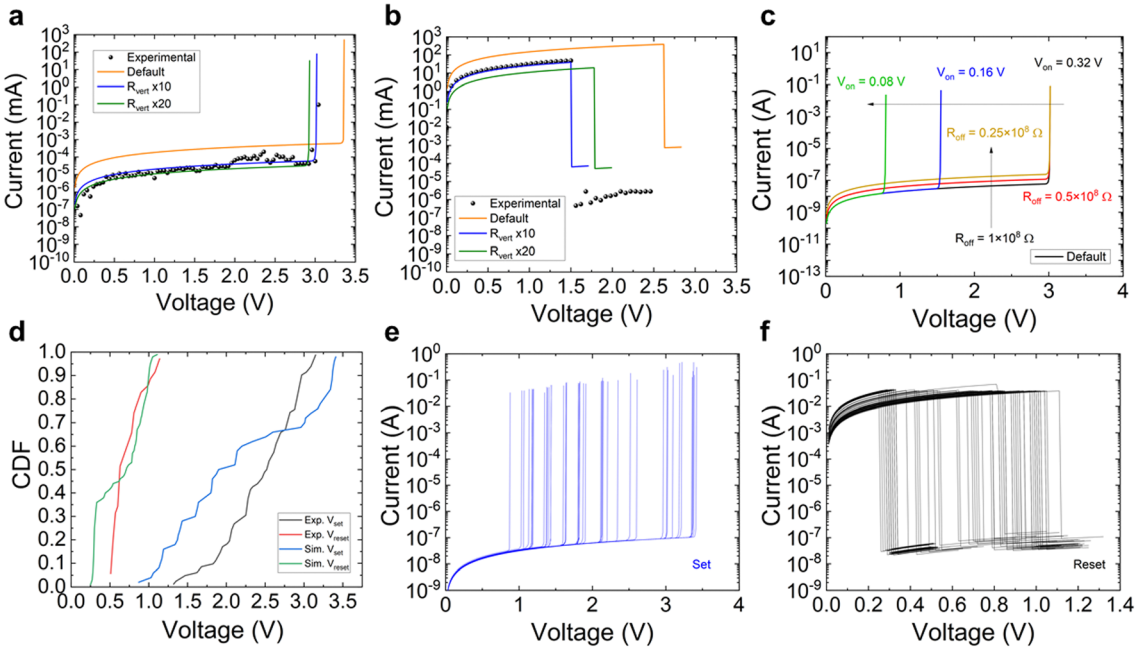

Fig. 3 (a) Current *versus* voltage absolute value curve of simulated data (solid lines) and experimental data (black symbols) for a set process and (b) for a reset process. An 18 × 18 × 18 resistor array was employed to obtain this simulation using CBs with two resistance levels: $R_{off} = 1 \times 10^8\ \Omega$ and $R_{on} = 0.5\ \Omega$. The model parameters in relation to Fig. 2 are: $V_{off} = 0.195$ V and $V_{on} = 0.32$ V. A 10 scale factor was employed between horizontal (lower) and vertical (higher) resistances. This corresponds to the blue line, a scale factor of 20 was used in the green line. The default curve (orange) stands for CBs with similar resistance values for the vertical and horizontal directions. (c) Simulated current *versus* voltage set curves. The model parameters employed were those of panel a, for the default curve. Other curves obtained by changing some of the model parameters are shown for comparison, to assess their influence in the simulation tool. (d) CDFs for the experimental (c) and simulated (panels e and f) set and reset voltage (absolute value) points extracted from the *I*–*V* curves. (e) and (f) Simulated set (reset) cycles obtained for different probabilities for the defect density included in the geometry described in Fig. 2e (a thick plane). The simulation parameters are the same as in Fig. 3a and b. Voltage absolute values were considered for the reset processes.

conduction are considered by means of the quantum point contact (QPC) model,[66,67] also the effects of metal pads and electrodes are included through a series resistance[68] (Fig. 2a).

The particularities of the h-BN dielectric are considered by utilizing two types of CB resistance values: in-plane CBs, represented in blue in Fig. 2a, that account for charge conduction in the BN layers, and out-of-plane CBs (red ones) that represent charge conduction in the dielectric vertical direction. The resistance values are described as plotted in Fig. 2b, selecting two, three or four levels. In whatever case, the red CBs are scaled with respect to the blue ones due to the different nature of the transport in a h-BN plane or in the perpendicular direction of the multilayer stack (*c*-axis).

At the beginning of the simulation (corresponding to a pristine dielectric), we can select the probability of having some CBs in the low resistance values (in case of two levels, the R_{on} value) in all the dielectric volume. In addition, we can define a 3D region, described by its geometrical equation, where the probability of having defects is higher than in the rest of the dielectric (this is modeled by increasing the CB probability of being in the low resistance value at the beginning of the simulation). Within the regions selected, determining a certain geometry (a single plane, Fig. 2d, a thick plane Fig. 2e, including several layers of CBs; a curved surface of different thickness, Fig. 2f), the initial probability can be changed (usually higher) with respect to the rest of the dielectric. This assumption can help to consider different pristine dielectrics or changes along a switching cycle series, and, therefore, direct the CNF formation through this region. If we consider three or four resistance levels for each CB, we can also select between other low resistance levels (R_{on}, R_{on2}, R_{on3}) as the CNF is getting formed along a set or forming process. The CB high-resistance component represents a defect-free dielectric region where charge transport is not enhanced by any means and the h-BN works as an ideal dielectric. The CB low-resistance component could be associated with the presence of a Ti atom inside the h-BN stack. Ti^{X+} ions move toward the cathode across the dielectric leading to CNF formation through the h-BN multilayer. These CNFs short the electrodes and strongly reduce the device resistance. The ions are expected to diffuse preferentially at locations where the lower density of the material and the larger density of B and N vacancies favor their migration. Under negative bias (the bottom electrode is assumed to be always grounded), Ti^{X+} ions may diffuse back to their original positions leading to CNF rupture, *i.e.*, a reset event.[18,60]

The switching between the CB resistance values is performed when V_{on} (also V_{on1} and V_{on2}) or V_{off} (also V_{off1} and V_{off2}) are overpassed (see Fig. 2b). Additionally, a fully thermal simulation can be performed by controlling the CB switching through temperature calculations, as described in ref. 55 and 69.

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IV. Results and discussion

We have simulated the devices tdescribed in Section II. An 18 × 18 × 18 matrix of resistors was employed since the 6 nm-thick dielectric consists of 18 layers approximately of h-BN.[16,18] We have employed a two-value CB resistance model, although higher complexities are allowed in the simulation tool (see Fig. 2b). As a reference, the scale between the values of the blue (in-plane CBs), see Fig. 2a, and red (out-plane CBs, higher resistance) resistances assumed in the simulation was 10. In this case, the best fit of the experimental curve was performed (blue curve, Fig. 3a and b). For a scale factor of 20 the green curve for the set *I–V* curve is obtained (Fig. 3a and b). We have also included for the sake of comparison a simulation where no distinction between the horizontal and vertical CBs is assumed (orange curve corresponding to CBs with equal resistance values). In this latter case a very different *I–V* curve is obtained. Due to the h-BN material structure, a distinction between in-plane and out-of-plane CBs is needed.

The fitting of the *I–V* experimental curves is shown in Fig. 3a and b. Some simulated curves are shown in Fig. 3c for different model parameters. See how the current level and the set voltage depend on the model parameters. A comparison between the set and reset voltage CDFs obtained from experimental and simulated curves is given in Fig. 3d. The group of simulated curves is obtained by changing the thickness of the geometry shown in Fig. 2e, and the probability linked to the CBs within this geometry in the low resistance state at the beginning of the simulation (see Fig. 3e and f where the group of simulated *I–V* curves is shown). In spite of the approximations performed in the modeling implemented in the simulator, the curve fitting is reasonable (Fig. 3d). In this respect the cycle-to-cycle variability can be described with our simulation tool.

In Fig. 4a we have plotted a simulated set current *versus* voltage. Different points have been marked along the curve in order to follow the CNF evolution. The low resistance value circuit breakers (R_{on}) are shown in red in Fig. 4b–e (assuming two resistance values CBs); these panels correspond to the simulation points shown in symbols in Fig. 4a. Notice how the CNF is formed as the set process unfolds until (in Fig. 4e) it shorts the electrodes and constitutes a fully-formed conduction path. The latter points (2–4) correspond to the sudden current rise that is seen both in simulated and experimental curves close to the set point, where a positive feedback process linked to the CNF formation is triggered.[24]

Some of the experimental curves measured present a stepped-like shape (see Fig. 4f) due to a CNF rupture in several stages. Our simulator can reproduce this behavior. In this respect, a single CNF could be broken in steps, or two CNFs (formed in a previous set event) can go through a reset process and get broken at different times. Experimental and simulated curves are shown in Fig. 4f to illustrate this effect.

The simulator can also be used to study large area devices. For instance, 100 nm × 100 nm area devices are simulated maintaining the number of CBs per nanometer that corresponds to the description of the h-BN layers of the dielectric described above. In this respect, millions of CBs are taken into consideration (see Fig. 5a and b for plots of a large area device simulation CB network). In this case, big matrix processing acceleration techniques have been implemented. In Fig. 5c we have shown arbitrary *I–V* curves simulated for devices with different areas. In this case no regions of high defect density were assumed. The probability of finding CBs in the low resistance value at the beginning of the simulation (1% in these examples) was the same in all cases; notice that a different random distribution is generated at the start of each simulation. We have scaled the *I–V* curves by a factor $\text{Area}_{\text{smallest_area_simulated}}/\text{Area}_{\text{actual_device_area}}$ in order to fairly compare the curves taking into consideration the purely resistive network that we have employed to model the device. It is seen that, although the current curves are close together, the set voltage varies in each of the device areas employed. This parameter depends on the initial random distribution of low resistance CBs. We have plotted the set voltage *versus* device area in Fig. 5d, and it can be seen that as the area increases the set voltage decreases. This effect is linked to the higher probability (for the higher area devices) of finding a pre-formed subpath with the random initial CB configuration to let the CNF be created. As can be seen, as the area increases, the set

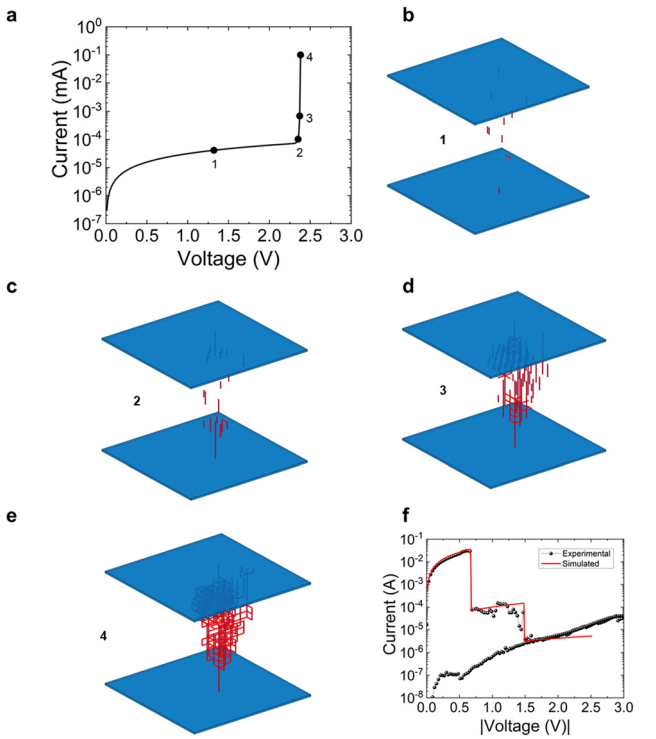

Fig. 4 (a) Simulated current *versus* voltage in a set process. See different points along the *I–V* that correspond to different CNF formation stages (the CNFs are plotted in panels (b)–(e)). An 18 × 18 × 18 network was employed to obtain this simulation using CBs with two resistance levels: R_{off} = 65.5 × 10^6 Ω, R_{on} = 0.24 Ω. The model parameters in relation with Fig. 2 are: V_{off} = 0.11 V, V_{on} = 0.25 V. A 10 scale factor was employed between horizontal (lower) and vertical (higher) resistances. (f) Simulated and experimental current *versus* voltage in a set process. A clear stepped curve is seen due to the partial CNF rupture along the reset process.

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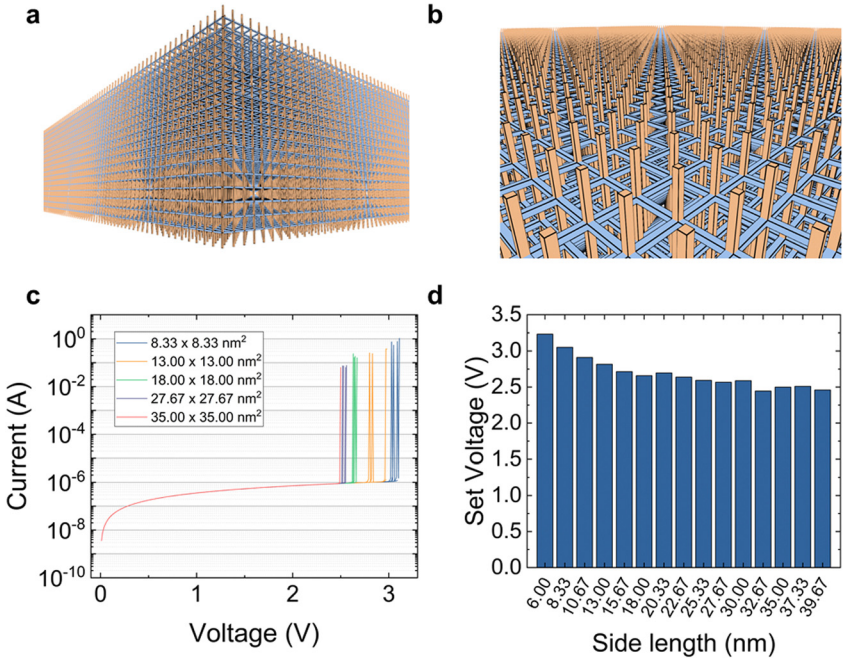

Fig. 5 (a) Resistance network corresponding to a great area (100 nm × 100 nm) device. (b) Resistance network corresponding to a great area (100 nm × 100 nm) device (zoomed-in view). (c) Several simulated set $I-V$ curves for different device areas (the current values are scaled with respect to the lowest area shown in the plot, *i.e.* (8.33 nm × 8.33 nm)). (d) Set voltage *versus* device side length (assuming a device square area obtained as (side length)^2).

voltage reduction saturates, as it is expected for devices where charge conduction is based on filamentary switching (Fig. 5d).

V. Conclusions

A 3D simulation tool based on CBs is developed for the first time to describe RS in multilayer h-BN memristors. It is based on CBs that can be modeled with two, three and four resistance states; in addition, a series resistance and a module are included to account for quantum effects. The simulator has been tuned with measurements of h-BN memristive devices. The influence of the model parameters has been shown in the simulator tuning process. We also show the CNF formation that accounts for filamentary charge conduction in our devices, explaining the current abrupt change when the set event takes place. In doing so, the particularities of the material have been taken into consideration. Moreover, the simulation tool is employed to describe partial filament rupture in reset processes. Finally, the dependence of the set voltage with the device area is described by means of simulations with a massive number of CBs.

Data available on request from the authors

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflicts of interest

There are no conflicts of interest to declare.

Acknowledgements

We acknowledge project PID2022-139586NB-44 funded by MCIN/AEI/10.13039/501100011033 and by the European Union NextGenerationEU/PRTR. F. M. G.-C. thanks project PP2022. PP-13 funded by "Ayudas del Plan Propio UGR 2022". M. L. acknowledges generous support from the King Abdullah University of Science and Technology.

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