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A brief overview of anodic memristors: fundamentals, classification and properties

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Memristors have emerged as a promising technology for next-generation memory and neuromorphic computing due to their ability to mimic synaptic behavior and retain previous resistance states, while showing potential as future energy-efficient devices. Various materials have been investigated for resistive switching applications, including valve metals, Hf, Nb, Ta, Ti, *etc.*, which stand out due to their ability to form stable oxide layers with tuneable oxide growth and ability for controlled defect engineering. These properties are crucial for obtaining reliability and scalability in memristive devices. A significant advantage of anodic memristor fabrication in comparison to other methods is the anodization process. It is a simple, cost-effective electrochemical method, which can ensure precise control over the oxide thickness, composition, and intrinsic defect structuring. By adjusting anodization parameters, it is possible to influence oxygen vacancy distribution and interfacial properties, thus enhancing resistive switching capabilities such as formation voltage, switching voltage, endurance, and retention. This review provides a detailed evaluation of memristive devices based on anodic oxides, from their fabrication, resistive switching mechanisms, and defect structuring to applications in memory and neuromorphic computing. Furthermore, a comparison of various valve metals and their alloys is presented, identifying their individual advantages and limitations in memristive performance.

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1. Introduction

Memristors, also known as memory resistors, have become one of the most important advancements in non-volatile memory technologies. Memristors were first predicted in 1971 by Leon Chua, as the missing fourth fundamental passive circuit element, along with resistors, capacitors, and inductors.[1] Memristors can store information based on their resistive states, offering memory and logic in a single device. Their resistance can be regulated by the history of applied voltage or current.[2] This concept remained mostly theoretical until 2008, when Strukov *et al.* at HP Labs reported resistive switching in nanoscale TiO_2 crossbar arrays inspiring modern research on the topic. Since then, over the last two decades, memristor development has gained significant interest, due to their potential applications in fields such as neuromorphic computing,[3] artificial intelligence,[4] and data storage.[5] Within this broad field, anodic memristors are relevantly new devices, whose oxides are grown by electrochemical anodization of a valve metal, rather than by using vacuum techniques, such as sputtering and atomic layer deposition (ALD). One of the first anodic memristors was reported in 2010 by Miller *et al.*, whose devices showed bipolar memristive switching in thin TiO_2.[6] Building on these studies, many research groups have since explored anodization parameters in order to optimize anodic memristive devices and materials. This is done by varying the oxide thickness, electrolyte composition, applied voltage, time, and temperature to tune switching voltages, ON/OFF ratios,

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endurance, and device-to-device variability. These efforts have jointly proven anodic oxidation as a versatile method for fabrication of memristive devices and provided an alternative route toward simplified fabrication. More recently, combinatorial studies on valve metal alloys have enabled systematic screening of memristive behaviour in the corresponding mixed anodic oxides, allowing for a fast route to map the composition to property relationships and further identify promising material systems.[7]

The foundation of memristors lies in the metal–insulator–metal (MIM) structure, which consists of a thin insulating layer of an oxide, active from the memristive point of view, sandwiched between two metal electrodes.[8] This configuration allows the devices to display resistive switching behavior *via* changes in the resistance across the oxide layer by application of an external voltage.[8] The electric field enables oxygen vacancies or metal ions to migrate within the oxide layer, causing localized changes in the material's conductivity. The ion migration is reversible and therefore opens the possibility of switching between a low resistance state (LRS) and a high resistance state (HRS).[9] In binary logic, the HRS represents level "0" or the OFF state, while the LRS describes the "1" or ON state.[2] Several different fabrication pathways for memristive devices are actively being researched. Here, different approaches lead to significantly different switching mechanisms and overall behaviour. Understanding and being able to influence these parameters are the key to improved device performance. Most methods are based on physical or chemical vapor deposition methods, where the metal oxide is deposited directly or through reactive deposition methods. The so-formed layers are then either stacked, as, for example, in bilayer devices, or chemically altered after the fabrication in order to improve their performance.[10,11] Examples for these can be structural changes, like from an amorphous to a crystalline phase or the change of the underlying substrate. Another possibility is the introduction of defects in order to alter the memristor behaviour.[12,13] Amidst these classes of memristors, anodic memristors have drawn attention due to their simple structure, easy fabrication, robustness, and scalability.[14,15]

In the process, thin films of valve metals, such as Hf,[16] Nb,[17–19] Ta,[20,21] and Ti,[22–24] are deposited on a substrate and then anodized to form an oxide layer.[15] The valve metal oxide then acts as an active insulating layer in the MIM structure.[15] The properties of the anodic oxide, such as its thickness, composition, and defect concentration, can be closely controlled *via* the adjustment of process parameters such as applied voltage,[21] anodization time,[17] and electrolyte composition.[16] It additionally allows the precise control of defects such as oxygen vacancies, which play a critical role in the switching mechanism of memristors, therefore allowing fine-tuning of the electrical properties of the devices, such as switching voltage and retention.[25,26] Furthermore, during the anodization, it is possible to incorporate additional dopants, intrinsic defects, and multilayered structures, expanding their range of applications.[19]

In the present work, a concise overview of anodic memristors is given. General concepts detailing the memristive structure and resistive switching characteristics are reviewed and particularities of anodic oxides are emphasised. Filamentary, interfacial and hybrid resistive switching types are described and the relevance of the electrochemical nature of the active anodic oxide film is related to the device performance. The possibility of intrinsic defect engineering provided by the electrochemical route of oxide fabrication is evaluated and its influence on the memristive behaviour in terms of stability, reliability and reproducibility is discussed. A large number of alloys providing functional anodic memristors upon anodization is shown from data available from high throughput combinatorial studies. Finally, an overlook of the main potential application categories such as memories, neuromorphic computing and sensors is provided for understanding the currently underestimated relevance of the electrochemical anodization as a tool for memristive device fabrication.

2. Fabrication and operation principles of anodic memristors

2.1 Metal–insulator–metal structure for anodic memristors

A simple MIM structure is essential for many electronic devices, including resistive random-access memories (ReRAM) and memristors in general. The configuration consists of a thin insulating/dielectric active layer sandwiched between two metallic electrodes, usually referred to as the top electrode (TE) and the bottom electrode (BE) due to their most common vertical stacking. A general representation of the MIM architecture in the case of anodic memristors is shown in Fig. 1.[9]

This structure is relevant for resistive switching devices, since the changes in resistance that occur in the active layer (AL) are responsible for their memory effects. Simple yet effective, the MIM structure is used for fabrication of nanoscale resistive switching devices, as the switching is based on changes in the conductive properties of the active layer.[8] An electrical field is applied between the TE and the BE across the insulator, allowing the device to switch from the ON to OFF resistive state. The MIM architecture allows for scalability and

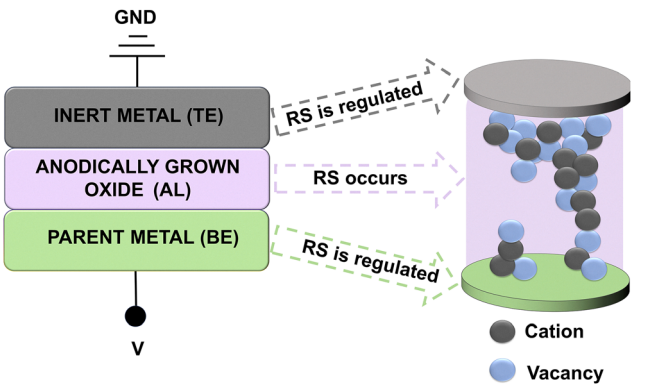

Fig. 1 General metal–insulator–metal structure (adapted from ref. 9).

high-density memory structures.[27] The correct choice of TE and BE is vital for a functioning memristor.[8] Apart from applying the electric field, the role of the TE is to initiate and control the resistive switching (RS). In general, metals such as Pt, Ag, and Au are typically used as they are chemically stable, resistant to oxidation, and excellent electrical conductors.[28,29] The most common choice for a TE is Pt, due to its inertness and convenient Schottky barrier height when in contact with most anodic oxides. It does not react with the AL during operation, ensuring stable switching behaviour following a large number of switching cycles (10^3–10^8). Similar to the TE, the BE must have good electrical conductivity in order to be able to readily transport charges through the insulating/active layer.

In the case of anodic memristors, common valve metals (Al, Hf, Nb, Ta, Ti, W, and Zr) are used as the BE.[16] These metals are known to form stable oxides through anodization,[30] which are further employed as the active layers of the MIM structures.[23] The good electrical conductivity of valve metals, along with their ability to form oxides capable of maintaining resistive switching while exhibiting outstanding dielectric properties, makes them ideally suited for use as BEs.[30] From the fabrication point of view, an anodic memristor is a MIM structure where the active oxide layer is not deposited using conventional thin film deposition techniques but is rather grown from the BE parent metal/alloy. In Fig. 2(a), the steps involved in fabrication of anodic memristors (MIM devices) are presented.[31] Following its deposition, the parent metal BE is anodized in an electrochemical cell containing a chosen aqueous electrolyte as the source of O^{2-} ions necessary for oxidation. Anodization is typically performed with a three-electrode setup, where the parent metal is used as the working electrode (WE), in combination with an inert counter electrode (CE) and a reference electrode (RE). Similar to any other memristive device, a patterning process (shadow masking, lithography, *etc.*) is involved in obtaining the Pt TEs. To further emphasize the relevance and simplicity of anodization among other routes for fabricating the AL in MIM devices, a comparison with three other commonly used alternatives is shown in Fig. 2 and Table 1. Fig. 2(b) shows the traditional steps used in the sol–gel route. There, a metal–organic or salt precursor solution is deposited, typically by spin-coating or dip-coating, after which it is converted into an oxide film by drying and thermal annealing. The sol–gel approach is also an attractive alternative, as it requires only very simple equipment and inexpensive precursors to cover large or even flexible substrates.[32] However, as summarized in Table 1, sol–gel ALs often suffer from higher roughness, cracking and pinholes. As a result, the final microstructure and stoichiometry are sensitive to solution chemistry and annealing, which can lead to larger device-to-device variability. Fig. 2(c) schematically shows the ALD route for AL

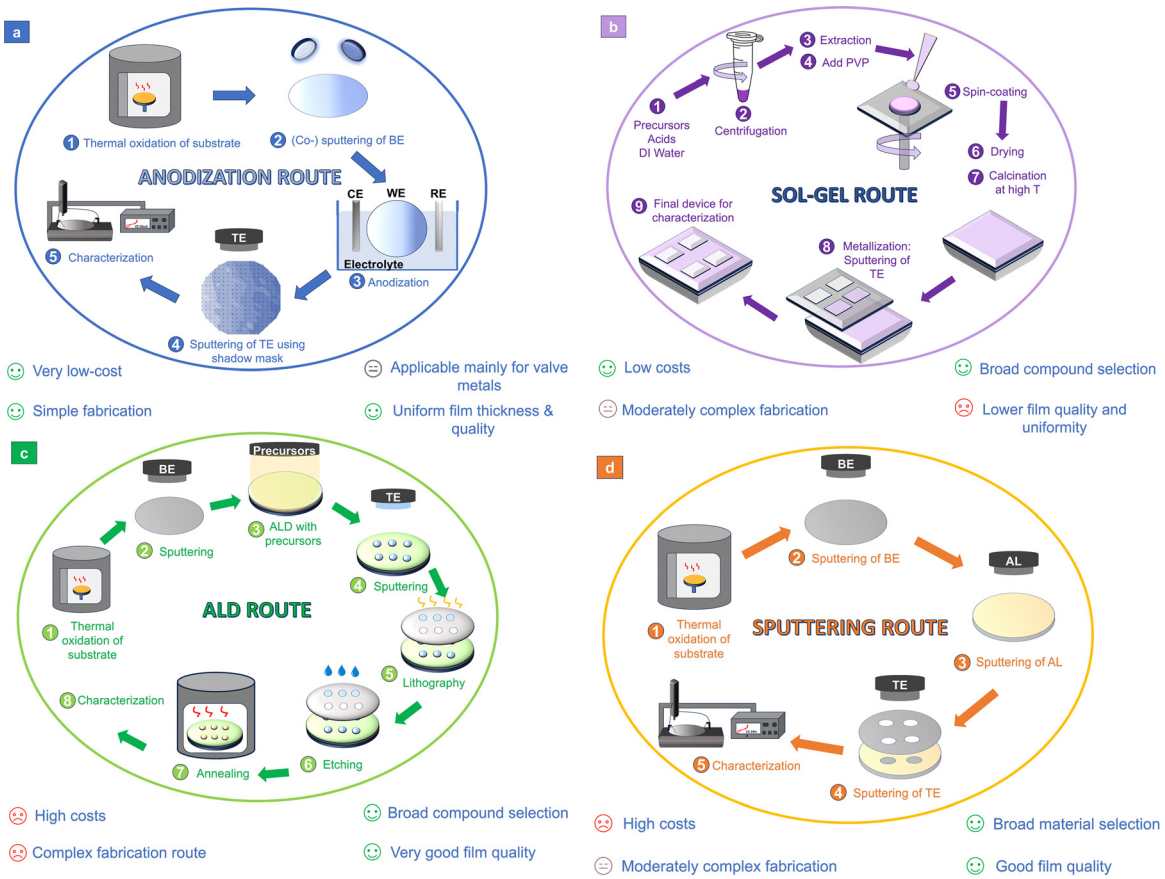

Fig. 2 Typical fabrication steps of the AL by (a) anodization,[31] (b) sol–gel,[32] (c) ALD,[101] and (d) sputtering[102] routes.

Table 1 Comparison of fabrication routes used to obtain the AL in memristive devices

AL fabrication	AL materials	Costs	Fabrication complexity	Time and throughput	Film quality and uniformity	Ref.
Anodization	Limited: mainly applicable for valve metals	Very low: electrolyte, potentiostat, electrodes needed	Very simple: basic electrochemical knowledge needed	Very fast: oxide growth can occur in tens of nm s^{-1} and parallel on large areas	High: thickness control *via U, t*, and electrolyte selection. Uniformity can also be controlled *via* conditions and electrolytes	39
Sol–gel	Wide variety: binary and complex oxides	Low: spin-coater, hotplate/furnace, precursors needed	Medium: chemically complex, mechanically simple	Medium: deposition is fast, bottleneck is drying and high-T annealing, as well as multiple coatings for thicker films	Low: can cover large areas; but more prone to thickness variations, cracking/peeling, pinholes vs vacuum films and anodization	40–42
Sputtering	Wide variety: binary and complex oxides, perovskites, *etc.*	Medium: vacuum system, targets and wafers needed	Medium: vacuum system handling and optimization needed	Fast: deposition rates at nm min^{-1}	Medium: good thickness and composition uniformity on flat wafers; but line-of-sight poor step coverage in deep 3D structures	35–38 and 43
ALD	Wide variety: binary and complex oxides	High: very expensive reactors and precursors; slow cycles increase per-wafer cost	Medium to high: precursor handling, temperature windows, and nucleation layers add complexity	Slow: 0.5–1 Å per cycle; hundreds of cycles for 5–10 nm thickness and long process times, especially for high volumes	High: atomic-scale thickness control, excellent conformality in high-aspect-ratio features, very uniform between devices	33, 34 and 44

fabrication. In this case, the AL is grown by alternating, self-limiting surface reactions, allowing atomic-level thickness control and excellent conformality even in high-aspect-ratio structures. This approach yields very uniform, compositionally well-defined switching layers and is very beneficial for 3D integration and precise vacancy/interface engineering. However, most ALD tools and precursors are expensive, the growth rates are relatively low, and process integration can be more complex.[33,34] For these reasons the overall cost per device is higher than that for the other mentioned routes. Fig. 2(d) depicts the sputtering route, where the insulating oxide is deposited in a vacuum chamber by physical sputtering from a ceramic or metallic target. Magnetron sputtering is commonly used in microfabrication lines, as it offers reasonable throughput and can be combined with standard lithography and etching, making it a very practical choice for CMOS-compatible ReRAMs. On the downside, the step coverage is poorer than that in ALD, as it produces very thin layers. Sub-nanometre thickness control can then become more challenging, and uniformity in complex 3D geometries is limited by the line-of-sight nature of the process when no reactive conditions are provided.[35–38] In contrast, anodization relies on a simple electrochemical oxidation step carried out in a liquid electrolyte, using inexpensive equipment and operating at or near room temperature. It naturally produces well-defined metal/oxide interfaces and can yield highly uniform films over large areas with any degree of complex 3D geometries with minimal process complexity.[39] Overall, the comparison in Fig. 2 and Table 1 underlines that anodization is the simplest and most affordable of the four routes for forming the active insulating layer, while still offering competitive film quality and device performance, especially when compatible valve-metal systems are involved.

2.2. Resistive switching characteristics

Generally, memristive devices exhibit two main types of switching behavior: either unipolar or bipolar switching between a HRS and a LRS. In most cases, a forming process is first employed by applying an electric field under certain current limitations for obtaining a stable device before the actual memristive operation. Switching to an ON state (LRS) is known as the SET process. This process requires higher voltages than the RESET process, which returns the device to the OFF state (HRS). In contrast, the RESET process demands a higher current than the SET process. Unipolar switching refers to a switching between the HRS and the LRS, where the polarity of the voltage itself is irrelevant. In this case, only the magnitude is significant for the switching process, which occurs in a single *I–V* quadrant. In contrast, bipolar switching is defined by having voltages of opposite polarity for the SET and RESET processes. The current–voltage characteristics of unipolar and bipolar memristors can be seen in Fig. 3(a) and (b), respectively. For both switching modes, the switching is induced by electrical stimulation.[13] Key factors influencing the process are Joule heating and the applied electric field. The former is more common for unipolar devices, while the latter is attributed to bipolar switching devices as they are primarily driven by electric-field-induced redox reactions.[45]

While unipolar and bipolar switching are typically treated as distinct resistive switching mechanisms, certain memristive devices exhibit a hybrid behavior. This phenomenon is known as mixed switching and involves the coexistence or transition between unipolar and bipolar switching characteristics under different operational conditions, as for Nb_2O_5.[18] For instance, the set current compliance (CC) can significantly affect the type of resistive switching. Altering the CC during device operation can cause a transition between unipolar and bipolar switching. At lower CCs, the device may predominantly exhibit bipolar switching, characterized by the polarity-dependent formation and rupture of conductive filaments. Unipolar switching may become dominant at higher CCs, likely due to thermal effects facilitating filament dissolution independent of polarity.[18,46,47]

When the memristor is grown anodically from its parent metal (or alloy), the hybrid switching behaviour may also be

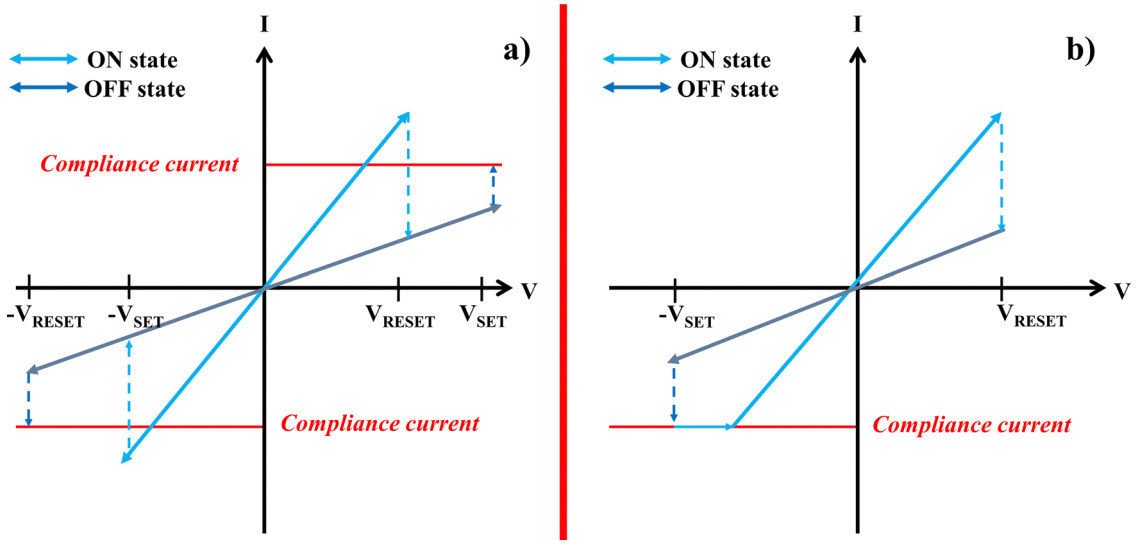

Fig. 3 *I–U* curve for (a) unipolar and (b) bipolar switching of memristive devices (redrawn from ref. 45).

related to the electrolyte used for anodization. Generally, in any electrochemical anodization process, a finite (usually negligible) amount of electrolyte species may be trapped inside the growing oxide due to the high field-induced ionic movement necessary for the actual formation of new oxide. If most applications of anodic oxides tend to neglect this incorporation, this is not always the case of anodic memristors.[19,21] Common electrolyte species such as those containing C, Na, P, B, *etc.*, may form regions preferentially used for the reversible formation of filaments (for bipolar switching) or regions with enhanced Joule effects (for unipolar switching). An example of hybrid switching is found in HfO_2-based anodic memristors, where a balance of oxygen vacancy dynamics and Joule heating determines the mode of operation. Such hybrid devices allow multi-functional and multi-level switching, enabling applications in reconfigurable circuits and neuromorphic computing.[16]

Following the idea of atomic scale modification of a memristive oxide for improved properties, the concept of a composite anodic memristor was recently introduced and refers to active anodic oxides that consist of amorphous/crystalline oxide mixtures and/or a combination of different oxide chemistries. A very good example of anodic composite memristor is found when anodizing Hf/Ta superimposed films. In Fig. 4, such a situation is presented with atomic resolution and an amorphous Ta_2O_5 column may be observed as surrounded by crystalline HfO_2. The memristive behaviour of such a composite structure obtained exclusively by anodization showed

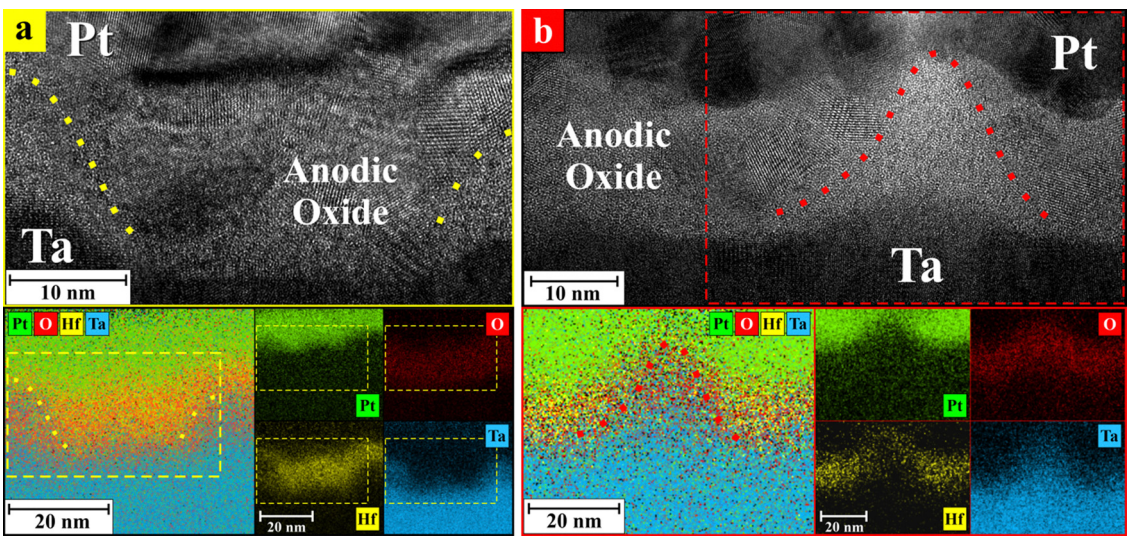

Fig. 4 Composite Hf/Ta oxides of anodic memristors grown (a) in citrate buffer and (b) in phosphate buffer together with the correspondent elemental energy-dispersive X-ray spectroscopy maps. The approximate position of the amorphous Ta_2O_5 nanocolumns surrounded by the polycrystalline HfO_2 matrix is highlighted with dotted lines.[48]

improved properties when compared to classic memristors, especially in terms of very high HRS/LRS ratios and switching cycles. Moreover, unipolar or bipolar switching was reproducibly demonstrated by the appropriate selection of current limitation.[47,48] In devices with composite or mixed-oxide layers (*e.g.*, HfO_2/Ta_2O_5), regions within the oxide matrix can favour one switching mechanism over the other. The relative contribution of these regions to the overall switching behavior can shift based on external factors, such as the applied voltage or current level.[48]

During the SET process, the memristor transitions from the HRS to the LRS through the application of voltage, which typically causes the formation of conductive filaments in traditional memristors. In valve metal oxide memristors, this can occur due to the movement of oxygen vacancies, which create conductive pathways and increase the material's conductivity. The SET process enables the storage of information by physically altering the device. On the other hand, the RESET process reverses this by transitioning the device from the LRS back to the HRS, effectively erasing the stored information. This happens when an opposite-polarity voltage causes the oxygen vacancies to disperse, increasing the resistance.[49,50]

The HRS and LRS can represent binary data, with the HRS corresponding to "0" showing no formation of filaments and the LRS corresponding to "1",[2,50] with a conductive filament or a lowered Schottky barrier.[7] A greater difference in resistance between these two states improves the device's data storage capacity and ensures a clearer distinction between the different states. If a memristor can maintain stable resistance states without power, it is classified as non-volatile, whereas volatile memristors lose their stored states without a continuous electric field. In the case of volatile devices, the resistance state returns from the LRS to the HRS once the electrical bias is removed, usually within microseconds to nanoseconds.[51]

Non-volatile memristors can retain both the LRS and the HRS for prolonged periods without applied bias. This stability makes non-volatile devices effective for memory/storage applications, where long-term data retention is needed. This type of switching is typically governed by ion or oxygen vacancy migration which "holds" the state until the next switching is possible. The distinction between volatile and non-volatile devices can be found in neuromorphic computing as well. Volatile memristors still exhibit memory behavior, but they revert to their original state once the electrical stimulus is removed, making them useful for neuromorphic computing, where they mimic synaptic behaviours such as "forgetting", thus simulating the short-term memory of the human brain. In contrast, non-volatile memristors are ideal for applications requiring stable "memory" over time, simulating the long-term memory of our brain.[52]

In the broader classification of resistive switching devices, volatile and non-volatile behavior represent the two fundamental memory models. Volatile switching, characterized by a spontaneous return to the HRS once the voltage is removed, is often attributed to conduction mechanisms such as charge carrier trapping/de-trapping or reversible ionic movements.[52] In contrast, non-volatile switching involves the retention of the LRS after voltage removal, mainly due to conductive filament formation. Threshold switching, however, is typically classified as a volatile phenomenon, as the resistance state reverts to the HRS once the applied voltage drops below a critical threshold.[53] This feature separates threshold switching from non-volatile switching, where the LRS is preserved independent of the applied voltage.[53] Thus, volatile memristors can be classified as threshold switching types (digital) and analog switching types.[52] Digital-type devices exhibit abrupt resistance changes with high HRS/LRS ratios and fast switching speeds in the range of nanoseconds, making them suitable for high-speed devices and logic circuits.[52] In contrast, analog-type memristors display gradual conductance changes with lower HRS/LRS ratios, making them more suitable for neuromorphic computing and mimicking of synapsis.[52]

Threshold switching in anodic memristors has been reported not only for mixed anodic oxides[7,46,54] but also for Nb_2O_5 and TiO_2.[55] In the case of Nb, where both non-volatile and threshold mechanisms are reported based on the O content, the switching behavior is heavily influenced by the oxygen stoichiometry within the Nb_2O_5 layer. A higher oxygen vacancy concentration typically promotes filamentary switching, enabling non-volatile memory characteristics. In contrast, a more stoichiometric oxide with fewer oxygen vacancies results in threshold switching. With accurate oxygen vacancy control, devices based on Nb can be designed to be more suitable for either non-volatile memory or neuromorphic applications.[19,54] This duality arises because the oxygen content directly affects the defect density, which governs the formation and dynamics of conductive filaments. Devices with oxygen-deficient oxides provide sufficient active sites for filament formation, allowing stable and permanent resistive states. On the other hand, stoichiometric oxides have limited vacancy pathways, favouring transient, volatile switching. The volatile nature of threshold switching makes it particularly beneficial for applications like neuromorphic computing, where transient behavior can mimic the spiking dynamics of biological neurons.[56]

As already discussed, resistive switching allows the memristors to alter their resistance, thus enabling them to retain and recall information. The mechanism causing the memory effects depends on the device's conductivity, which is modified by the formation of conductive filaments or interfacial effects in the oxide layer of the MIM structure. The former is known as filamentary switching (FS), while the latter is an interfacial switching (IS). In both cases, with the application of voltage, oxygen ions and vacancies experience a promoted migration within the oxide layer. This leads to the formation or breakdown of conductive pathways, allowing the memristor to alter its resistance.[57]

2.3. Filamentary resistive switching

The most common mechanism for the RS in memristive devices is FS, which depends on the formation of conductive filaments. They are highly conductive paths inside the oxide layer of the MIM structure. The filaments are composed of

metal ions or oxygen vacancies. They can extend along the entire dielectric layer, connecting the gap between the TE and the BE. This allows the memristor to switch between OFF and ON states. When a conductive filament is formed, the device goes from the OFF to ON state; conversely, when a filament is ruptured, the device goes back into the OFF state. The most common FS mechanisms are the electrochemical metallization mechanism (ECM) and the valence change mechanism (VCM). In the ECM, the conductive paths are formed by electrochemical reduction and metal ion migration, while the VCM depends on oxygen vacancy migration, resulting in local redox reactions. Both mechanisms have a highly localized nature, allowing for low power consumption, as the switching occurs in a small volume of material. Furthermore, FS devices exhibit fast switching, endurance from 10^6 to 10^9 cycles, and long retention times.[25] This makes the FS devices suitable for non-volatile memory applications. Filament stability and control over the formation/rupture dynamics are critical for both the ECM and the VCM. These challenges will be discussed in the following sections.[49,57]

2.3.1. Electrochemical metallization mechanism. Memristors based on the ECM rely on forming and dissolving metallic filaments within a solid electrolyte to regulate the transition between the HRS and the LRS. The ECM is associated with cationic devices, having an active electrode, such as Ag and Cu.[58] The switching behavior is driven by redox reactions at the electrodes, making ECM-based memristors suitable for a wide range of memory applications.[57] They are particularly applicable in the context of next-generation memory technologies aiming for high density, fast operation, and low power consumption. In ECM cells, metal cations migrate under an applied electric field towards an inert electrode, such as Pt and W. This begins with the application of a positive bias towards the active electrode, causing the anodic dissolution of the metal at the interface. The metal cations are introduced into the insulating layer, accumulating at the opposite electrode due to the high electric field present. When reaching the opposite electrode, the metal cations are reduced, forming the conductive metallic filament, which acts as the bridge between both electrodes in the MIM structure.[57] In this way, the device can switch to the ON-state, represented by a low resistance. In Fig. 5, a schematic representation of the atomic level processes occurring during SET and RESET operations of an ECM memristor is presented. During the initial OFF state (Fig. 5(1)), no metallic deposit occurs on the inert electrode, and thus the device has a high resistance. When a positive bias is applied to the active electrode (Fig. 5(2)), the metal atoms begin to dissolve and move through the insulating layer, and the reduction of the metal ions then results in the formation of conductive filaments (Fig. 5(3)). Filament formation is influenced by electrochemical kinetics, ion mobility and the strength of the applied electric field. The insulating layer is critical for the transport of metal cations. Valve metal oxides, such as those used in anodic memristors, are suitable for this, as they have excellent stability, high dielectric strength, and the ability to support controlled ionic transport, which are essential for reliable memristive switching. Furthermore, once the filament connects the two electrodes, the device transitions into an ON state, which has low resistance (Fig. 5(4)). If the voltage polarity is reversed, the filament is then dissolved, returning the device into the initial OFF state (Fig. 5(5)).[59]

Apart from binary switching between the LRS and the HRS, ECM memristors are known for having multilevel switching capabilities.[59] This characteristic allows the devices to exhibit multi-bit data storage, instead of a binary model. By controlling the CC, intermediate resistance states can be programmed. With varying currents during the SET process, the thickness and continuity of the filaments are altered. Thus, ECM-based memristors exhibit outstanding data storage capabilities. Despite the advantages multi-level switching devices possess, filament control is challenging. The initial electroforming needed to create the conductive paths can require high

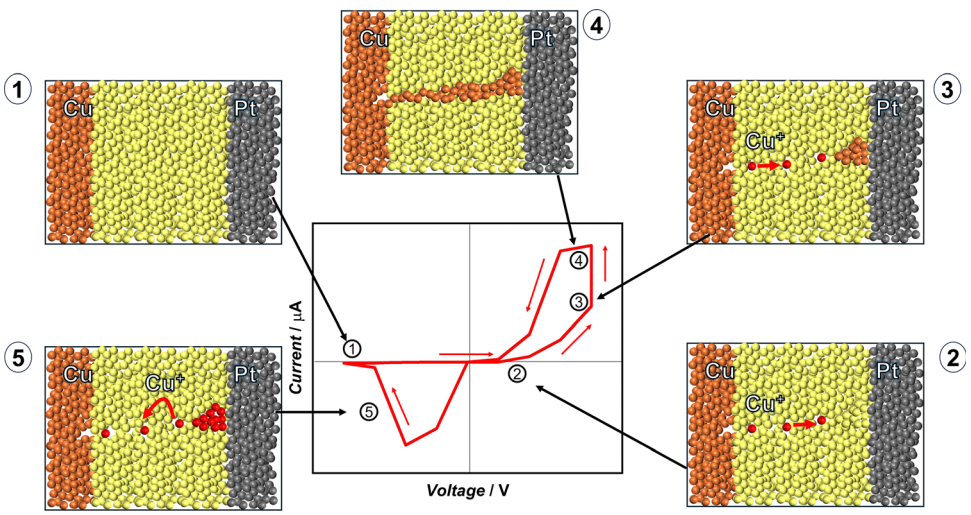

Fig. 5 Schematic representation of steps of the SET ((1)–(4)) and RESET (5) operations of the electrochemical metallization mechanism (redrawn from ref. 59).

voltages, which can further lead to variability in the device's performance or even breakdown of the film.[27] Furthermore, the retention and endurance in ECM devices may be problematic, as the stability of the metallic filaments over extended periods of time can lead to breakdown due to the constant thermal stress by the Joule effect occurring during the measurements.[59]

The ECM has not yet been fully studied for anodic valve metal oxides. For instance, an ECM-based memristor was demonstrated in devices with a heterojunction structure made of SiO_2/Ta_2O_5. Here, the conductive filaments are formed and dissolved within the Ta_2O_5 layer under an applied electric field. The conductive filaments are composed of metal cations originating from the active electrode, which, in this case, is Ag. The SiO_2 layer serves as a crucial buffer, regulating the growth direction and confinement of the filaments, ensuring uniform switching behavior. ECM memristors exhibit exceptional electrical performance, at low operating voltages (<0.3 V), while still maintaining high stability and reproducibility. The inclusion of the SiO_2 layer helps to prevent uncontrolled filament overgrowth and improves the overall switching reliability. This shows that with appropriate design, valve metal oxides, such as Ta_2O_5, can effectively support ECM-based switching, creating energy-efficient memory technologies with enhanced performance characteristics.[60]

Even though at the moment, there are no studies on anodic memristors exhibiting the ECM, the potential is very big. For such anodic memristors, one should consider that the inclusion of an additional metallic ion should be a part of the anodization process itself. The electrochemical community is familiar for a long time with the fact that electrolyte species are always embedded in the growing anodic oxides and exactly this trait will likely be explored. Recent reports have already discussed the presence of electrolyte species inside anodic memristors, positively impacting their stability and resistive switching.[16,19,21,24]

2.3.2. Valence change mechanism. The VCM is another possible mechanism driving the resistive switching behavior. Similar to the ECM, it is based on the formation and dissolution of conductive filaments. The filaments are driven by the creation and migration of oxygen vacancies and oxygen ions. Again, similar to the ECM, this process begins with an electroforming step, where a high electric field is applied to the device, causing a soft breakdown of the dielectric. During electroforming, the O^{2-} ions in the oxide layer migrate from their lattice positions toward the anode, leaving behind oxygen vacancies in the lattice. The O^{2-} ions could either react with the anode material to form an interfacial oxide layer or be oxidized and discharged as neutral oxygen.[23] The migration of O^{2-} ions toward the anode creates a negative charge buildup at the electrode/oxide interface while leaving behind positively charged oxygen vacancies in the oxide layer. This charge redistribution can significantly influence the electrical properties of the material, such as resistance switching in memristors. When enough oxygen vacancies have accumulated, the conductive filaments can form. In this way, the filaments create a connection between the TE and the BE, switching the device from OFF to ON and allowing current conduction through the device. The filament formation is governed by redox reactions *via* the relocation of oxygen ions under the influence of the electric field. The vacancies allow the formation of the conductive paths, resulting in a SET process in the LRS. Conversely, the RESET process causes the oxygen ions to return to the oxide layer from the anode interface. In this way, a recombination of oxygen ions and vacancies occurs, which then leads to complete or partial filament rupture, returning the device to the HRS. The reversible switching between the two states by formation and rupture of oxygen-based CFs enables the VCM-based memristors to retain and recall resistive states without the need for external power.[9,49]

In Fig. 6, a visual representation of the conductive filaments within an anodic HfO_2 oxide layer is depicted. Their formation is localized, displaying the highly conductive pathways that extend through the oxide layer, connecting the TE and BE. This demonstrates the filamentary nature of the switching mechanism. Oxygen vacancies build up under an electric field to create pathways, enabling the device to transition between resistive states. In addition, concurrency is visible, which refers to the simultaneous existence and interaction of multiple conductive filaments within the oxide layer. This phenomenon can result in multilevel resistance states, where the concurrent activity of multiple filaments allows the device to exhibit intermediate resistance levels. This multilevel behavior is more common for filamentary type switching but has been reported for interfacial memristors as well.[16]

Valve metal anodic memristors are predominantly governed by the VCM due to the intrinsic properties of their oxide layers and the anodization process. The anodic oxidation of valve metals such as Hf, Ta, Nb, and Ti results in the formation of dense, stable, and insulating/semiconducting oxide films such as HfO_2,[16,61,62] Ta_2O_5,[63] and Nb_2O_5.[19,62] These oxides are characterized by high dielectric constants and localized oxygen vacancies.[30] During anodization, an electric field drives O^{2-} ions or hydroxyl species toward the metal, creating an oxygen-deficient oxide layer with vacancies. These vacancies act as active species in the formation of conductive filaments, facilitating the redox reactions that define the VCM. Unlike the ECM, which relies on the migration of metallic cations (*e.g.*, Ag^+ and Cu^{2+}), the VCM operates without significant cation contributions.[9,49,64]

VCM-based switching in anodic memristors was also demonstrated by $Nb/NbO_x/Au$ memristors, resulting in an amorphous structure with oxygen vacancies distributed throughout the oxide. These oxygen vacancies served as active defects governing the resistive switching behavior. Quantized conductance steps observed during electrical testing confirmed the formation and rupture of atomic-scale conductive filaments, composed of oxygen vacancies, under applied electric fields. The precise control over filament dynamics was attributed to the uniform defect distribution achieved through anodic oxidation. Additionally, the Nb/NbO_x interface acts as a reservoir for oxygen vacancies, facilitating their migration during the SET and RESET processes. This dynamic interaction

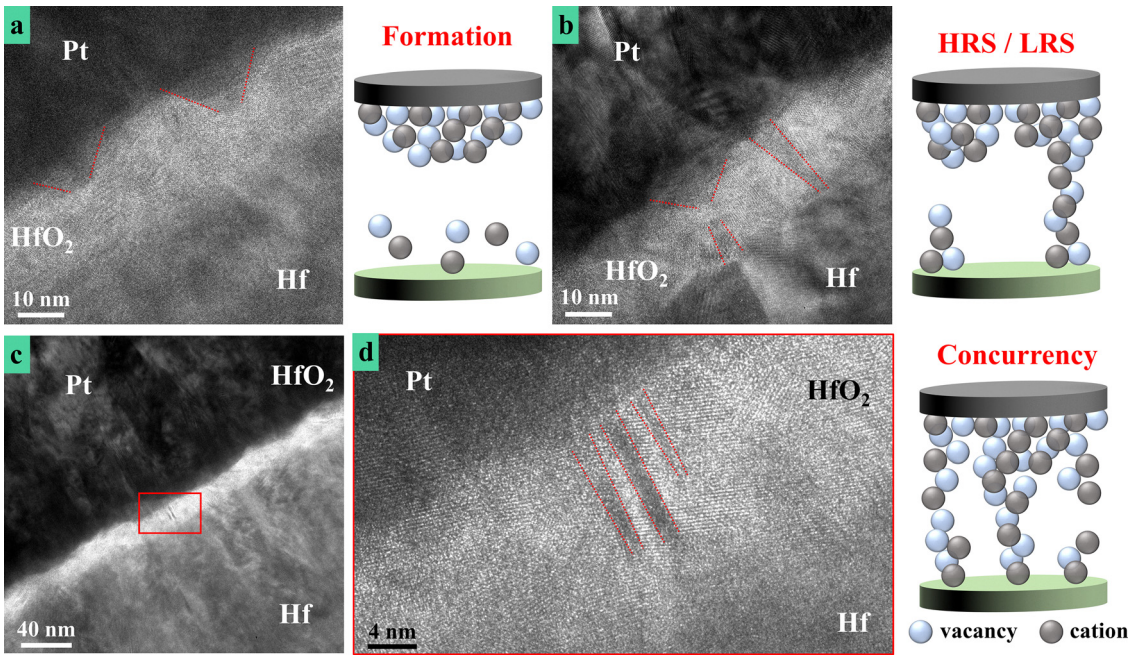

Fig. 6 Anodic Hf memristor showing (a) vacancy accumulation, (b) complete and interrupted filaments representing the LRS and HRS and (c) and (d) concurrent filaments leading to multilevel switching.[16]

between the vacancies and the oxide layer enabled reliable switching between the HRS and the LRS.[18]

2.4. Interfacial resistive switching

IS is also known as non-filamentary switching and is found in MIM structures, which have a semiconducting oxide. This switching mode is gentle and, in most cases, electroforming-free. These types of memristors are often characterized by excellent stability and non-linear current traits with self-rectification properties. Physical or chemical reactions at the oxide/electrode interface govern IS. The two main mechanisms behind IS are non-filamentary ion migration and charge trapping.

Typically, a Schottky contact is needed between one of the electrodes and the semiconductor for the non-filamentary ion migration to occur. Therefore, a Schottky barrier is formed, which increases in height or decreases with the movement of charges or vacancies under the applied electric field.[65,66] The switching takes place when changes in the concentration of oxygen vacancies occur near the Schottky contact. If a negative voltage is applied to the TE, oxygen vacancies are attracted to it, which leads to an increase in the concentration of vacancies at the upper part of the active layer, while the vacancy concentration is decreased across the thickness of the layer. In contrast, if a positive voltage is applied to the TE, the vacancies migrate away from the upper boundary, thus reducing their concentration near the Schottky contact.[57]

p-type semiconductors have oxygen vacancies as their primary charge carriers, and therefore, the LRS signifies their uniform distribution. When the vacancies migrate towards the TE, a depleted region is created near the BE, leading to the HRS. Oxygen vacancies typically act as donor-like defects in n-type semiconductors (*e.g.*, TiO_2, Nb_2O_5, Ta_2O_5, and HfO_2), contributing free electrons as the main charge carriers. In these materials, a uniform distribution of vacancies corresponds to the HRS because it limits the formation of conductive filaments. In contrast, the migration and clustering of vacancies to form localized conductive pathways result in the HRS. Thus, non-filamentary memristors rely on the movement and redistribution of oxygen vacancies or ions across the active interface. The accumulation of oxygen vacancies near the interface reduces the height of the Schottky barrier, resulting in an LRS. Conversely, their depletion increases the barrier height, restoring the HRS. This process is driven by the applied electric field during operation. Initially, electrons become trapped at the TE/oxide interface, creating a negatively charged interfacial layer. The negative charge attracts positively charged oxygen vacancies, causing them to accumulate near the interface. The movement and redistribution of these vacancies modulate the device's resistance by altering the Schottky barrier height, resulting in transitions between the HRS and the LRS.[57]

Interfacial resistive switching in anodic memristors was demonstrated for Nb–Ti alloys during a high throughput combinatorial study. The metallic BEs were prepared by co-sputtering with varying Ti contents (22–64 at% Ti) prior to their anodization for memristor fabrication.[7] The anodic memristors obtained were confirmed to be non-filamentary *via* transmission electron microscopy (TEM), showing a homogenous oxide layer, with no sign of conductive filaments. The memristors were specified as a self-rectifying interfacial type. Based on *I–U* sweeps analysis, a deviation from traditional memristive sweeps is observed, as shown in Fig. 7. Fig. 7(a)

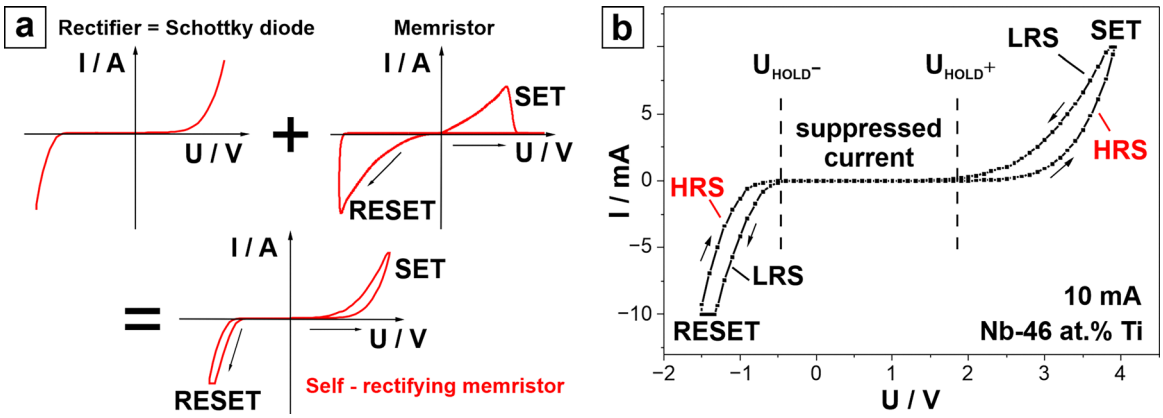

Fig. 7 (a) Typical *I*–*U* sweeps for a rectifier, a memristor and a self-rectifying memristor. (b) *I*–*U* sweep of the Nb – a 46 at% Ti anodic memristor.[7]

illustrates typical *I*–*U* curves from three device types: a rectifier, a memristor, and a self-rectifying memristor for comparison. In Fig. 7(b), the anodic memristor highlights its similarity to self-rectifying memristors. Initially, the device is in the HRS, with the current increasing only after applying a positive hold voltage U_{HOLD} (at approximately 2 V). Beyond this voltage, the current rises sharply until the device reaches a SET voltage – U_{SET} (4 V), where it transitions into the LRS. As the voltage is reduced, the LRS current is suppressed, and a further negative voltage bias leads to current reactivation at U_{HOLD} (0.5 V). The device then returns to the HRS at a reset voltage U_{RESET} (−1.5 V). Current suppression between the holding potentials is a characteristic of self-rectifying behavior and is attributed to the formation of Schottky barriers at the interfaces.[7]

The gradual transition between the HRS and the LRS observed in the *I*–*U* curve corresponds to interfacial switching mechanisms. A complementary study describes anodic TiO_2 memristors as exhibiting forming-free, bipolar resistive switching with self-rectifying behavior. A gradual resistive transition and multilevel states suggest a switching mechanism, potentially influenced by uniform defect structures within the anodic oxide layer.[22]

2.5. Hybrid resistive switching

Hybrid resistive switching mechanisms combine aspects of both, interfacial and filamentary switching. These processes occur simultaneously or sequentially, contributing to the overall resistive behavior of the device. Devices with this mechanism usually display short-lived or partial filaments concurrent with changes in the Schottky barrier height at the electrode–oxide interface, caused by electric field and ion redistribution influences. These hybrid devices combine the gradual resistance changes of interfacial mechanisms alongside the sudden switching associated with filamentary processes.[67]

An example of hybrid resistive switching is anodic Ti memristors. Devices fabricated in phosphate buffer exhibited self-rectifying and volatile behavior, usually attributed to interfacial resistive switching mechanisms. TEM analysis revealed the presence of crystalline protrusions within a semi-crystalline TiO_2 matrix, suggesting the formation of partial filaments as observable in Fig. 8. This structural observation supports a hybrid interfacial memristive switching model, where both interfacial barrier modulation and partial filament formation contribute to the device's resistive switching behavior. Hybrid devices exhibit higher HRS/LRS ratios of 10^4 Ω, ensuring good distinguishability between the two states, for reliable operation. In addition to this advantage, their self-rectifying qualities allow for lower power consumption.[24]

3. Defect engineering for resistive switching

A critical factor for enhancing resistive switching, as well as the lifetime and stability of memristive devices, is intentionally controlling and creating defects within the oxide layer. Intrinsic defects such as oxygen vacancies and stoichiometric or crystallographic irregularities not only are byproducts of oxide formation but also play an active role in defining the type of resistive switching (see Fig. 8). Therefore, the filament formation (or lack of) and the device's reliability are directly influenced. Defect engineering can be carried out by

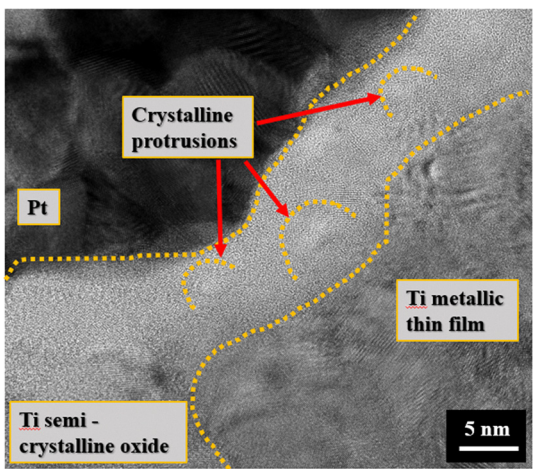

Fig. 8 TEM image of the anodic memristor grown on a Ti thin film with the Pt top electrode (adapted from ref. 24).

introducing dopants to stabilize oxygen vacancies or modify electronic properties. Furthermore, this can be achieved by material type, configuration and post-process heat treatments. An extremely favorable way to create intrinsic defects is by anodization, due to its simplicity and cost-effectiveness as recently demonstrated in combinatorial studies on Hf–Ta alloys.[47,48] By selecting appropriate electrolytes and adjusting process parameters, such as the potential and scan rates, the oxide layer can be tuned for selected applications.[16,68–70] The intrinsic formation of defects through the anodic process of memristive film formation and the control of dopants *via* electrolyte selection represent clear advantages of anodic memristors. In classical memristive device fabrication routes, these aspects need to be addressed separately by appropriate deposition/doping procedures which are time consuming and increase the overall costs.

To further emphasize the influence of defect engineering, Table 2 provides an overview based on fabrication methods for HfO_2, TiO_2, Nb_2O_5, and Ta_2O_5 based devices. This is followed by a subsection presenting anodic alloys, in which the composition is tuned electrochemically, mainly based on electrolyte selection. The most common electrolytes used for anodic oxidation are phosphate buffer (PB), citrate buffer (CB) and borate buffer (BB). For each entry, the most important resistive switching characteristics are reported: HRS/LRS ratio, switching mode, multilevel capability, dominant switching mechanism, endurance type and cycles, and forming behavior. While absolute values depend on device design and testing conditions, the overview aims to indicate that anodic memristors are able to achieve comparable results to other commonly used AL fabrication methods. Several entries listed for the anodic memristors either match or exceed values of the other fabrication techniques, such as the sol–gel method, ALD and sputtering. This shows that anodization, while being a simpler, lower-cost and energy efficient method, is still able to produce reliable memristive devices.

3.1 Electrolyte selection

The choice of electrolyte is vital for the performance of anodic memristors. It governs the formation and properties of the oxide layer.[30,80] The electrolyte composition, pH and ionic species directly influence the defect density, stoichiometry, and structural uniformity.[80] Furthermore, it can govern the anodization kinetics, including the oxide growth rate and thickness.[30] For example, PB solutions can stabilize oxide by complexing with metal ions, leading to uniform and compact oxide layers.[24,30] In addition, the electrolyte species can be incorporated into the oxide layer during anodization, modifying its conductivity and enhancing its qualities, *e.g.* by pinning the atomic path of filament formation and deletion, leading to improved multilevel resistive switching and device lifetime.[30] For instance, in anodic Ti-based memristors, the use of PB as an electrolyte typically results in unipolar switching, whereas citrate buffer CB leads to bipolar switching. The devices fabricated in PB exhibit superior HRS/LRS ratios of 10^4, compared to those in CB with only 10^2. This effect can be attributed to the higher oxide resistance of memristors prepared in PB and the incorporation of phosphate species into the oxide layer.[24]

The incorporation of phosphate species is also reported for Ta,[21] Nb[19] and Hf[61] based anodic memristors. In the case of Ta devices, the anodization in PB results in advantages in the lifetime and stability of the memristors during reading and writing. While CB and BB devices withstand only 10^4 and 10^5 cycles, respectively, the PB device exhibits endurance up to 10^6 cycles without signs of degradation. The reasoning behind the excellent performance of the PB anodized Ta oxide memristor is related to oxyphosphate formation, causing spatial pinning of CF positions during reading and writing operations. This allows the CF's positioning to be predefined *via* anodization and improves its stability. Meanwhile, no incorporation of borate or citrate species was found, resulting in poorer memristive characteristics for these anodic oxides. A similar situation is reported for Nb_2O_5 memristors, where the electrolyte choice leads to drastic differences in device behaviour, comparable to Ti and Ta based devices. Oxides grown in CB show multilevel switching properties, while PB anodized oxides have a prolonged lifetime and stability in the LRS and the HRS. The exact values and mechanisms behind the RS behaviour can be referred to in Table 1.[19]

3.2. Influence of the active layer thickness

Anodic oxidation allows for a fine control of the AL thickness, but reports show that stable memristive behaviour exists only within a certain oxide thickness window. For anodic oxides on Ti, Ta and Nb, with the oxide thickness ranging between roughly 30 and 200 nm, an approximately linear thickness–voltage relationship of 1.6 to 2 nm V^{-1} was reported. This shows that the thickness can be adjusted very reproducibly just by the electrochemical parameters used during the anodic oxidation. Within this range, however, the memristive behaviour was found to depend strongly on the thickness governed by the anodization potentials applied. Thinner oxides grown at 10 V showed no memristive behaviour at all, while optimum anodization parameters were found at 25 V. These devices with an intermediate layer thickness exhibited the most pronounced *I–U* sweeps and therefore highest ON/OFF ratios. Memristive responses were found to degrade with higher applied cell voltage (30–90 V).[81]

A similar trend is observed in an anodic TiO_2 memristor, where devices based on thinner oxides fabricated potentiostatically with very short anodization times of 1 and 3 s (at 30 V) showed degraded ON/OFF ratios and smaller hysteresis openings, while longer anodization times of 60 s (at 30 V) led to asymmetric and unstable *I–U* characteristics. In contrast, memristors with intermediate oxide thicknesses grown for 10 s (at 30 V) allowed for the most symmetric and reproducible memristive *I–U* responses, with the highest ON/OFF ratios.[6]

In reports on anodic TiO_2 nanotube memristors, the nanotube layer thickness was varied between 80, 120, 160 and 200 nm at 10 V for 5, 10, 15 and 20 minutes, respectively. All devices were tested for their HRS/LRS ratios depending on the number of switching cycles. The lowest HRS/LRS ratios (below

Table 2 Representative RS performance of valve metal devices grouped by active layer fabrication methods

Material	AL	AL fabrication	HRS/LRS ratio	Switching type	Multilevel switching	Switching mechanism	Memory	Endurance cycles	Electro-forming	Ref.
Hf	HfO_2	Sol gel	10^3	Bipolar	—	Filamentary	Non-volatile	—	No	32
		ALD	10^2	Bipolar	5 levels	Filamentary	Non-volatile	10^4	Yes	71
		Sputtering	10^2	Bipolar	12 levels	Filamentary	—	—	No	72
		Anodization								
		BB	10^0	Bipolar	2 levels	Filamentary	Non-volatile	10^2	Yes	16
		CB	10^1		4 levels			10^5		
		PB	10^0		1 level			10^5		
Nb	Nb_2O_5	Sol gel	—	Unipolar	—	Filamentary	Non-volatile	—	Yes	73
		Sputtering	$\approx 10^3$	Unipolar	—	Filamentary	—	10^3	Yes	74
		Anodization								
		CB	10^2	Unipolar	8 levels	Filamentary	Threshold and	10^6	Yes	17–19
		PB	10^2	Bipolar depending on CC	4 levels		non-volatile	10^6		
Ta	Ta_2O_5	ALD	—	Bipolar	—	Filamentary	Non-volatile	10^4	Yes	75
		Sputtering	10^3	Bipolar	—	Mixed	Non-volatile	10^3	Yes	76
		Anodization								
		BB	10^1	Bipolar	2 levels	Filamentary	Non-volatile	10^5	Yes	20 and 21
		CB	$\approx 10^2$		2 levels			10^4		
		PB	10^2		4 levels			10^6		

Material	AL	AL fabrication	HRS/LRS ratio	Switching type	Multilevel switching	Switching mechanism	Memory	Endurance cycles	Electro-forming	Ref.
Ti	TiO_2	Sol gel	10^2	Bipolar	3 levels	Interfacial	Non-volatile	10^2	No	77
		ALD	10^3	Bipolar	—	Filamentary	Non-volatile	—	Yes	78
		Sputtering	10^2	Bipolar	—	Filamentary	Non-volatile	10^2	Yes	79
		Anodization								
		CB	10^2	Bipolar	4 levels	Interfacial	Volatile	10^6	No	22–24
		PB	10^4		4 levels			10^6		
Hf-Nb										
Hf-18 at% Nb	HfO_2/Nb_2O_5	CB	10^7	Bipolar	1 level	Filamentary	Threshold and	10^2	No	54
Hf-45 at% Nb			10^6		5 levels		non-volatile	10^7		
Hf-70 at% Nb			10^1		2 levels			10^2		
Ta-Hf										
Ta > 50 at% Hf	Ta_2O_5/HfO_2	CB	10^1	Bipolar	3–4 levels	Filamentary	Threshold and	10^6	Yes	47 and 48
Ta 50–70 at% Hf			10^7	Unipolar	2 levels		non-volatile	10^6	No	
Ta < 70 at% Hf			10^2	Bipolar	1 level			N/A	Yes	
Nb–Ta										
Nb-13–30 at% Ta	Nb_2O_5/Ta_2O_5	PB	10^2–10^4	Unipolar/bipolar	3–4 levels	Filamentary	Threshold and	N/A	Yes	46
Nb-31–40 at% Ta			10^2	depending on	7 levels		non-volatile	10^9	No	
Nb-40–65 at% Ta			10^2–10^6	CC	4–5 levels			10^5	Yes	
Nb-66–80 at% Ta			10^2–10^4		4 levels			N/A	Yes	
Nb–Ti										
Nb- 24–36 at% Ti	Nb_2O_5/TiO_2	PB	10^4–10^5	Bipolar	4 levels	Interfacial	Volatile	10^6	No	7
Nb-37–48 at% Ti			10^6							
Nb 49–52 at% Ti			10^4–10^5							

one order of magnitude) withstanding only 5 cycles were reported for devices with an oxide thickness of 80 nm, while the ratios of approximately 100 were acquired by memristors with 160 and 200 nm thick ALs. The best performing device with an AL thickness of 120 nm exhibited the highest HRS/LRS ratio.[82] Moreover, thicker anodic films have been reported to suffer from poorer mechanical stability and less attractive device characteristics, such as higher electroforming voltages and lower HRS/LRS ratios compared with films of tens up to a few hundred nanometres.[39] All reports taken together emphasize the importance of the AL thickness while tuning devices for optimum performance metrics.

3.3. Alloying of bottom electrodes and combinatorial screening for anodic memristors

The nature of the BE can also lead to defect engineering of anodic oxide memristors.[68] This is mainly related to the competition for oxygen of different cations which a valve metal alloy will contain. By manipulation of the type and concentration of defects in the oxide layer, switching mechanisms can be controlled to enhance device performance and tailor memristors for specific applications, such as non-volatile memory, neuromorphic computing, or high-density crossbar arrays.[15] To efficiently test different alloys as BEs, a combinatorial approach proved to be a very straightforward method for identification of ideal parent metal electrodes. This involves the simultaneous fabrication of the BE *via* co-sputtering, where the deposition geometry is adjusted to achieve a gradient composition of an alloy on a single substrate. After the co-sputtering of the BE from two (or more) metal targets, energy-dispersive X-ray spectroscopy (EDX) mapping is usually carried out to quantify the compositional gradient obtained across the substrate. This step is crucial, as even small variations in the alloy composition can strongly influence the anodization behaviour and the resulting memristive switching characteristics. By determining the local composition at each position on the Si wafer, the subsequent electrical measurements can be correlated with a specific alloy, allowing a composition to property relationship to be established. An example of an EDX composition map of such a gradient is shown in Fig. 9(a) for a combinatorial library created with two valve metals. Here, the colour scale indicates the local metal content across the library. The follow-up anodization results in the formation of mixed oxide layers. Not only it is straightforward and highly scalable, but it also provides a convenient way to quickly evaluate the memristive properties of various valve metal alloys simultaneously, in a high throughput screening manner. The corresponding finished library, after anodization and TE fabrication, is presented in Fig. 9(b), showing how the continuous composition spread is transformed into an array of individual memristor cells ready for high-throughput electrical screening.[46] This approach simplifies the fabrication process and facilitates the rapid evaluation of memristive properties across a range of compositions. By carefully screening alloys, the defect structure within the oxide layer can be compositionally tuned, enabling easier control over oxygen vacancy distribution, conductivity, and switching behavior.

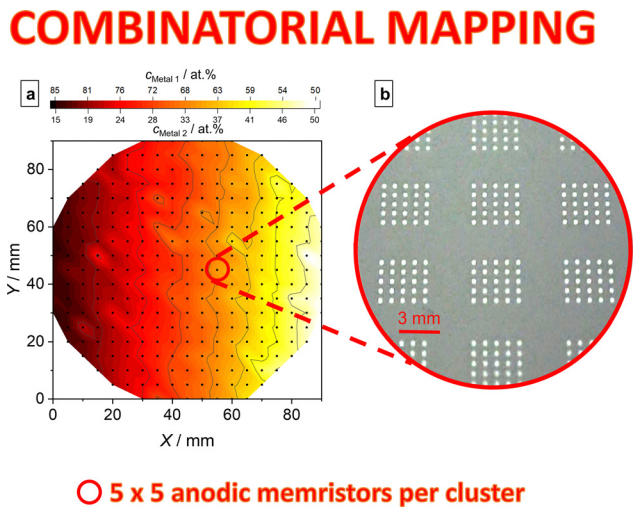

Fig. 9 (a) Example of EDX mapping for a combinatorial library created by alloying 2 valve metals and (b) an image of a finished anodic library.

In this way, alloying serves as a powerful tool for defect engineering in anodic memristors, allowing optimization for memristor performance in specific applications.[7,15,31,46–48,54,83]

In Fig. 10, intrinsic defect engineering by anodization of a Hf-50 at% Ta bottom electrode is presented as obtained from a combinatorial Hf–Ta study. Inside the active memristive mixed oxide, the presence of small pure HfO_2 crystallites is observable, directly impacting the memristive behaviour allowing a change from bipolar to unipolar devices with enhanced properties. Additionally, an enrichment of Hf species close to the top electrode was related to very different ionic transport numbers for Hf and Ta during their competition for O in the anodization process. Unipolar Hf–Ta anodic memristors have an in-depth homogeneous local chemical state of Hf and lower electronic polarizabilities for O and Hf. This is considered as beneficial for the memristive endurance and retention performance.[31]

Studies on Nb–Ta alloys for memristive applications reveal that the concentration of each valve metal significantly impacts the electrical behavior and switching characteristics of the anodic devices. By screening the memristive properties along the parent metal compositional gradient, (ranging from Nb-13 at% Ta to Nb-80 at% Ta), regions were identified where anodic memristors exhibited bipolar, unipolar and coexistence of both switching regimes. Devices grown from bottom electrodes with a higher Ta concentration, above 41 at% Ta, exhibited unstable switching behavior for both unipolar and bipolar cases and lack of multilevel switching capabilities. In contrast, memristors grown from alloys with up to 30 at% Ta are described as bipolar, multilevel and non-volatile. The best performing Nb–Ta alloys were found between 31 and 40 at% Ta, with their anodic oxides having unipolar switching, multilevel capabilities, and forming free behavior, in contrast to all other Nb–Ta alloys. This shows the critical role of the alloy composition in influencing defect structures and their impact on memristive behavior. Alloys exhibiting bipolar and multilevel switching are well-suited for applications such as non-volatile memory and

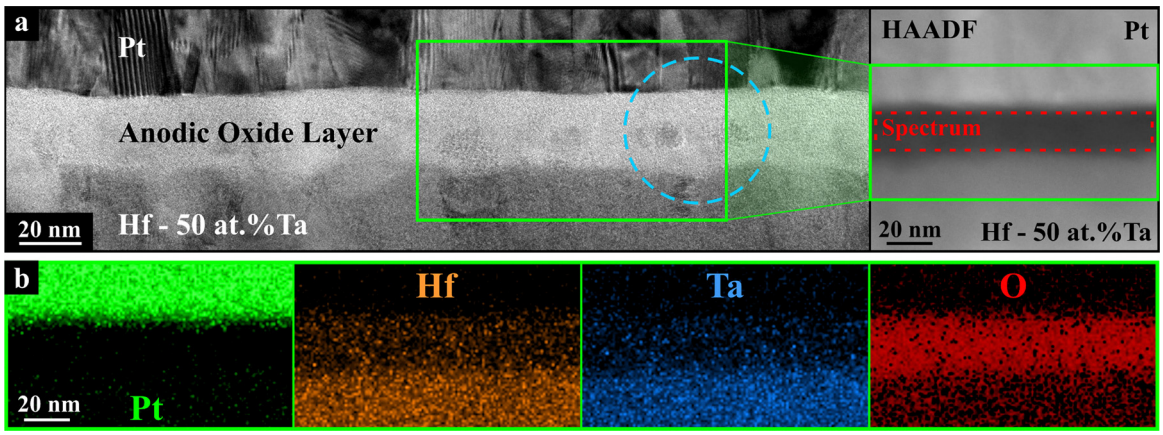

Fig. 10 (a) TEM image of a Hf–Ta anodic memristor showing small HfO_2 crystallites embedded in a mixed Hf–Ta anodic oxide as shown in (b) STEM EDX compositional maps of the region designated with a green frame in (a) (adapted from ref. 31).

neuromorphic computing, where precise and repeatable resistance states are needed. In contrast, alloys demonstrating free-forming, unipolar, multilevel, and threshold switching are ideal for applications in logic circuits, reconfigurable computing, and dynamic memory applications, owing to their versatile and adaptive switching characteristics.[46]

A further alloy example is Hf-45 at% Nb, whose anodic oxide also demonstrates how effective base alloy engineering can be employed to fabricate devices with low costs and low power consumption, but with outstanding memory properties. This memristor has an HRS/LRS ratio of several orders of magnitude, indicating its reliability for data storage and retrieval, along with multiple discrete resistance levels, allowing the storage of more than one bit per cell, thereby increasing data density. The memristors operated efficiently with reduced power requirements, enhancing their suitability for energy-sensitive applications, without electroforming requirements. The anodic oxide of Hf-45 at% Nb consists of a heterogeneous mixture comprising HfO_2 crystallites embedded within quasi-amorphous and stoichiometrically non-uniform Nb oxide regions, in a manner similar to the case of the Hf–Ta alloy presented in Fig. 10. The mixed oxide layer facilitates the formation and dissolution of conductive filaments, underpinning the memristive and threshold-switching behaviours, which is superior to pure HfO_2 memristors.[54] The presence of HfO_2 crystallites is not a coincidence and is related to the crystalline nature of pure HfO_2, which, combined with the amorphization tendencies of both Ta and Nb anodic oxides and their much larger ionic transport numbers, results in such intrinsic effects.[84–86]

An interesting effect of selecting the correct alloys for enhancing atomic-size defects is the influence of mixed oxides on the structural properties of the device. The structural configuration of the oxide layer directly impacts defect dynamics and conduction mechanisms. Apart from the case of anodization of an alloy, such as Hf–Ta alloys shown in Fig. 10, there is another very interesting geometry, which classical memristors cannot achieve, related to the superposition of 2 valve metals in the BE before their anodization. This is fundamentally different from anodization of an alloy, since the parent metal layers are exposed to the anodization front sequentially, rather than simultaneously. As has been known in the electrochemical community for a long time, this anodization of superimposed layers may lead to the formation of oxide "fingers" due to differences in the electrical conductivity of the two growing oxides and the ionic current preferring the lower resistive path, thus overgrowing the more conducting oxide. The anodization outcome is described by elongated, finger-like protrusions of one oxide which extends partly or completely through the entire thickness of the anodic oxide, basically connecting both the TE and the BE.[86]

Recently, this effect was exploited for anodic memristors, which were termed as composite ones, as previously discussed and shown in Fig. 4. The presence of these oxide fingers in superimposed Hf/Ta anodic memristors has a great effect on their electrical properties. Since one influencing factor of the final composite oxide structure is the thickness of each metal, combinatorial studies are possible by deposition of superimposed metallic layers with varying thicknesses.[47] The fingers act as localized regions where oxygen vacancies tend to accumulate, facilitating conductive filament formation. This improves the memristor's switching operation by promoting stable and repeatable transitions between the resistive states. Furthermore, the combination of filamentary conduction along the oxide fingers and interfacial switching mechanisms leads to a hybrid resistive switching mode, allowing versatile applications. Devices with defined oxide finger structures exhibit high HRS/LRS ratios, as the localized field enhancement provided by the fingers increases the difference between the two states. The oxide fingers are more characteristic of alloys with higher Ta concentrations, which also leads to a denser and more defect-rich oxide structure. In conclusion, careful alloy design can be used as a powerful tool for the creation of mixed anodic oxides where the oxide structures are deliberately customized to optimize memristive performance.[47,48] An overview of the memristive properties of valve-metal alloys is provided in

Table 2. As shown, even slight adjustments in the alloy composition can produce systematic differences in device behavior, including endurance, retention, and HRS/LRS ratios.

3.4. Temperature effects

Temperature plays an important role in defect engineering of anodic MIM devices. It influences the formation, mobility, and distribution of defects within the oxide layer. Temperature affects both, the fabrication process and device operation, allowing control over defect characteristics to optimize performance and to customize switching mechanisms. Controlled thermal treatments, such as annealing and elevated-temperature anodization, are commonly employed to engineer the defect structure in oxide layers.[87] For instance, post-fabrication heat treatment facilitates the migration and stabilization of oxygen vacancies.[88] Furthermore, temperature influences defect behaviour during device operation.[87] Elevated temperatures increase the mobility of oxygen vacancies and interstitial ions within the oxide layer. This facilitates redistribution of defects, which, in turn, can modulate and enhance switching characteristics. In unipolar memristors, Joule heating caused by current flow can locally increase the temperature, stabilizing conductive filaments in the LRS. However, excessive heating may lead to filament overgrowth, resulting in permanent short circuits or degradation of switching reliability.[16,89,90]

This is illustrated by Hf-based anodic memristors, using oxide layers grown in a PB electrolyte. These memristors perform better after the application of temperature, which significantly influences the memristive properties of the devices. Studies have shown that these memristors change notably their HRS and LRS values when subjected to temperatures as low as 30 °C. Particularly, the HRS values increase, reaching a peak at approximately 50 °C, before decreasing towards 80 °C, where they approach the LRS levels. This temperature-dependent behavior results in a shift in HRS/LRS ratios, which follows the trend observed in HRS values. Endurance and retention tests carried out at 50 °C display enhanced stability compared to room temperature measurements, with improved uniformity and reproducibility of resistive states up to the failure point. These findings suggest that moderately high operating temperatures can enhance the performance of HfO_2 anodic memristors by optimizing defect structures within the oxide layer, thus improving device reliability and functionality.[16]

4. Applications of anodic memristors

Memristive devices, such those described in the preceding sections, started to gain scientific attention due to their potential for innovative high-tech applications. There are generally three areas in which the application of memristive devices holds great potential. Those primary areas of use are ReRAMs, neuromorphic computing and the sensors with various designs. This section will give a brief overview of the current state of research in these areas and explore exemplary devices that are currently being researched. To provide a better context for the applications of anodic memristors, representative anodic memristor characteristics are summarised in Table 2, in terms of switching type, forming behaviour, endurance, and HRS/LRS ratios, and a comparison to other memristive devices is provided. These are the most critical characteristics relevant for the different application classes discussed in this section. For ReRAM-based applications, the main criteria are stable switching behaviour, low operating voltages, high HRS/LRS ratios and stable endurance over many cycles. In the field of neuromorphic computing, multilevel conductance combined with analog gradual switching is the most critical trait. Regarding sensing applications, the most important parameters are the targeted analyte and resistance response related to the external stimulus. Finally, for logic and logic-in-memory applications, the same basic requirements as for ReRAM apply, with reproducible non-volatile states and sufficiently high HRS/LRS ratios being relevant.

4.1. ReRAMs

ReRAMs are among the most promising applications for memristors, offering potential as scalable and energy-efficient alternatives to most conventional memory devices. Certain criteria must be met for memristors to be viable for this application. They should exhibit non-volatility to retain stored information over extended periods of time. Furthermore, scalability demands are a crucial factor for industrial applications. To achieve this, they are typically fabricated as MIM structures at nanoscale dimensions. Another important property is the switching speed. Devices have to be able to switch between resistive states within nanoseconds, providing writing and reading speeds comparable to current state-of-the-art memories.

Anodically produced memristive devices have shown potential to meet all those criteria. For example, it was shown that Nb_2O_5 films fabricated in this manner show reliable switching with an ON–OFF ratio of 10^3.[17] Furthermore, anodically produced Ta_2O_5 exhibits good performance as well, with switching speeds as fast as 20 ns and a high endurance of up to 10^6 cycles.[20] Despite the progress that is being made in this field, there are still challenges that have to be met. For commercially relevant ReRAMs, switching speed and retention still have to be improved. Furthermore, the operating voltages should ideally be kept below 1 V.[57]

4.2. Neuromorphic computing

Neuromorphic computing aims to mimic the structure and function of the human brain in artificial systems to achieve greater energy efficiency and adaptive computing. Memristors are particularly suitable for this field of research due to their unique properties, such as volatility and non-volatility, as well as their structural resemblance to the functionality of the human brain. The way conductive filaments are formed and how they behave makes them the structures closest to simulating an artificial neuron in modern electronics. This idea is schematically presented in Fig. 11. Two neurons (pre-neuron and post-neuron) form a synapse by linking two of their

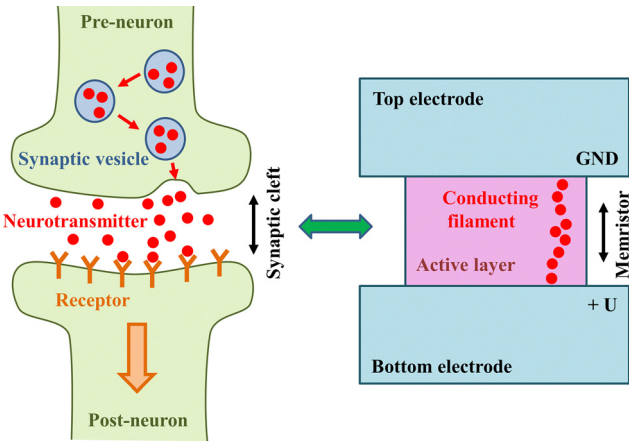

Fig. 11 Analogy between operation principles of synapse and memristors.

terminations *via* neurotransmitters passing electrical impulses from one to the other within the synaptic cleft. According to the Hebbian learning rule, when such synaptic connection repeatedly and successfully transmits electric signals, the coupling between the neurons becomes stronger, or their synaptic weight increases.[91] This behaviour is quite similar to the memristive switching. Furthermore, volatile and non-volatile memristors can be seen as analog to basic brain functions. Volatile memristors are compatible to "forgetting" since data cannot be retained without the application of an electric field, while non-volatile memristors provide support for "remembering" by long-term storage of data, thus simulating short- and long-term memory, respectively.[92] As examples from the valve metal family, TiO_2 based memristor-neuromorphic arrays have already been demonstrated as suitable candidates for applications such as convolutional neural networks with successful fast-converging *in situ* training without the need for additional circuitry.[26,93] Furthermore, the arrangement of memristive devices in crossbar arrays allows for their application in vector–matrix multiplications. It has been shown that they provide the possibility to perform multiple operations in parallel with local analog computing, opening up less energy demanding possibilities for the design of artificial neural networks.[94]

4.3. Sensors

Memristors are attractive for sensor applications due to their ability to integrate sensing, data storage, and *in situ* computation in a single device. The general mechanism behind their sensing capabilities is dynamic resistance modulation. These can be influenced by changes in pH, temperature or even more complex chemical interactions such as the oxidation of biomolecules. It has been demonstrated that anodically grown Nb–Ti oxide memristors exhibit potential for pH sensing applications. These memristors arranged in a crossbar array exhibited a linear response and high sensitivity for pH changes in bio-inspired electrolytes.[15] A schematic drawing of such a crossbar array and the detection mechanism can be seen in Fig. 12. Furthermore, HfO_2 and TiO_2 based memristors have been effectively used to sense biomolecules *via* changes in the

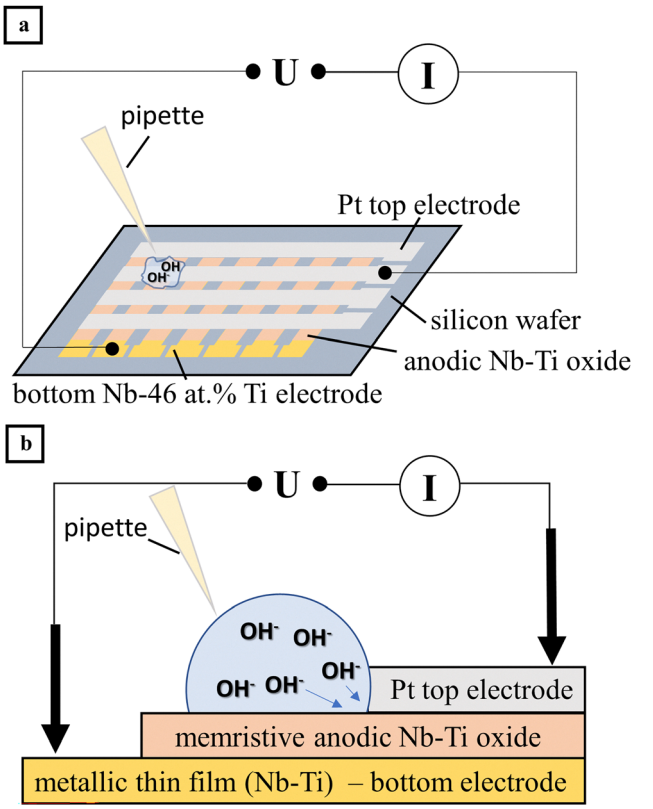

Fig. 12 (a) Schematic view of the crossbar array of anodic memristors on an oxidized Si wafer and (b) schematic view of a single memristive pH sensor defined by the crossing of bottom and top electrodes.[15]

hydroxyl ion concentration, highlighting their suitability for diagnostic applications.[14,95]

Additionally, promising efforts are being made in developing gas sensors based on memristive devices. These devices have been shown to reliably measure O_2 concentrations and NO contents in continuous and discontinuous gas flows.[89,90,96] Research is ongoing to develop advanced sensing units aimed at creating artificial auditory, visual, and tactile sensors with integrated *in situ* processing capabilities. Developments in this area are promising and could lead to highly advanced perception systems, in particular, combined with the neuromorphic computing capabilities provided by memristive devices.[96]

4.4. Logic and logic-in-memory

Beyond non-volatile memory and neuromorphic computing, resistive switching devices can also be implemented for stateful logic and logic-in-memory architectures. In stateful logic, the memristor resistance itself encodes the logic variable, with the HRS = 0 and LRS = 1.[97] At the same time, the same devices are used to retain and process information. This is carried out by applying voltage pulse sequences to a memristor array, enabling them to implement logic primitives, such as material implication (IMP) and FALSE, from which any Boolean function can be established.[98] Such concepts have been created for oxide-based memristors, including IMP-based logic, hybrid

memristor-CMOS gates, and compact analog or mixed-signal logic.[99] Anodic memristors fulfil the same basic device requirements required for logic operations. They are two-terminal elements, which have reproducible, non-volatile resistance states with appropriate HRS/LRS ratios and, in many cases, multilevel switching characteristics. Anodically formed Ta_2O_5 and mixed anodic oxides of Hf–Ta, for example, exhibit stable bipolar or unipolar switching, forming-free operation and sufficient HRS/LRS ratios.[21,47,48] These characteristics are precisely those exploited in existing memristor-based logic-in-memory demonstrations, suggesting that anodic devices could, in principle, be integrated into the same logic frameworks. However, Boolean logic gates implemented with anodic devices have not yet been described in the literature, as reports on anodic memristors, in general, are scarce.

5. Future outlook

Anodic memristors are a well-evolving area from a materials and device-physics standpoint into a more application-driven direction. Electrochemical anodization already offers a low-cost, low-temperature and scalable route to uniform oxide formation, with good thickness and composition control. The next step in the exploration of anodic materials for their memristive properties lies in the systematic screening of mixed and doped anodic oxides using combinatorial approaches. Recent work on anodic thin-film combinatorial libraries based on valve metal alloy systems has shown that composition spreads and defect engineering can be used to identify forming-free anodic memristors, tune the coexistence of volatile and non-volatile behaviour, and optimise endurance and variability across entire libraries. At the same time, anodic oxides are taking the first steps towards integration into crossbar arrays for sensing and neuromorphic functions. As a result, anodic oxides are found in Nb–Ti-based alloys for pH-sensing crossbars, nanoscale TiO_2 for neuromorphic devices, and volatile WO_3 for short-term plasticity. This indicates that more complex circuits and in-sensor/neuromorphic systems are within reach.[15,24,100]

Simultaneously, some bottlenecks and roadmap items can be identified. From a materials point of view, the strong connection between the alloy composition, electrolyte chemistry, anodization conditions and the oxide morphology indicates that the switching mechanism and device performance can vary continuously across a library, rather than having a single dominant mechanism. Furthermore, a stronger link between the local structure and conduction mechanisms remains an open challenge. From a technological position, the main obstacles are scaling anodic devices into dense, CMOS-compatible arrays while keeping variability under control. Addressing these challenges will require a closer integration of electrochemical process design with combinatorial screening, as well as the opportunity to place anodic memristors as a low-cost, sustainable alternative to vacuum-processed oxides in future memory, neuromorphic and sensing hardware.

6. Conclusions

Valve metals and their alloys are excellent materials for MIM memristive devices due to their ability to form stable, semiconducting or insulating oxide layers through anodization. These anodic oxides exhibit high dielectric constants, chemical stability, and tuneable electrical properties, making them ideal for the engineering of high-performance memristors. Anodization enables precise control over the oxide film thickness and composition, contributing to device stability and reliability. It is a cost-effective, straightforward method that can also allow for an intrinsic incorporation of nanoscale structures in order to create conductive pathways and optimize the resistive switching behaviour.

The choice of electrolyte during anodization significantly impacts the structure and functionality of the oxide layer, influencing properties such as the composition, defect density, and long-term stability. Optimizing these parameters is critical for reproducible performance and enhanced reliability. Furthermore, anodic memristors can exhibit a diverse range of resistive switching mechanisms, including filamentary (VCM or ECM), interfacial, and hybrid switching, enabling flexibility for specific applications. The resistive switching mechanisms allow for threshold and multilevel memory behavior, characterized by high HRS/LRS ratios, low operating voltages, and forming-free operation.

Defect engineering strategies, such as electrolyte incorporation (by appropriate electrolyte selection), alloying, and thermal treatments, further enhance the performance of anodic memristors. These devices demonstrate significant potential for neuromorphic computing, where their ability to mimic synaptic functions supports efficient and adaptive information processing. Features like multilevel resistance states, forming-free switching, self-rectifying behavior, and high endurance make them well-suited for scalable crossbar arrays and energy-efficient computing architectures.

Beyond neuromorphic applications, anodic memristors are suitable for fields such as reconfigurable circuits, secure hardware, and high-density memory storage. Their scalability, adaptability in switching behavior, and non-volatile nature address the growing demand for compact, high-speed, and energy-efficient electronic systems. As a result, anodic memristors serve as adaptable components, linking traditional electronics with emerging multifunctional technologies.

Despite their attractive features, in some cases, superior to their classical memristor counterparts, anodic memristors remain somewhat marginalized. Their scientific attention remains inferior compared to the focus on classical memristors, which, in the last few years, have increased exponentially, despite reports containing more and more complex fabrication procedures involving multi-layer thin film deposition combined with doping and various additional treatments. There are still many features of the anodic memristor yet to be studied and their industrial implementation still needs to be appropriately developed. However, its most attractive feature, provided by its inherently native nanoscale modifications

during anodization, will eventually appeal more scientists, once the design simplicity of this particular type of device is better communicated and advertised.

Conflicts of interest

There are no conflicts to declare.

Data availability

This is a review article. All data are available at locations described in the cited papers.

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References

1 L. Chua, *IEEE Trans. Circuit Theory*, 1971, **18**, 507–519.
2 L. Chua, *Appl. Phys. A: Mater. Sci. Process.*, 2011, **102**, 765–783.
3 Y. Xiao, C. Gao, J. Jin, W. Sun, B. Wang, Y. Bao, C. Liu, W. Huang, H. Zeng and Y. Yu, *Adv. Dev. Instrum.*, 2024, **5**, 0044.
4 Z. Cao, B. Sun, G. Zhou, S. Mao, S. Zhu, J. Zhang, C. Ke, Y. Zhao and J. Shao, *Nanoscale Horiz.*, 2023, **8**, 716–745.
5 J. Domaradzki, D. Wojcieszak, T. Kotwica and E. Mańkowska, *Int. J. Electron. Telecommun.*, 2020, **66**, 373–381.
6 K. Miller, K. S. Nalwa, A. Bergerud, N. M. Neihart and S. Chaudhary, *IEEE Electron Device Lett.*, 2010, **31**, 737–739.
7 D. Knapic, A. Minenkov, E. Atanasova, I. Zrinski, A. W. Hassel and A. I. Mardare, *Nanomaterials*, 2024, **14**, 381.
8 Y. Xiao, B. Jiang, Z. Zhang, S. Ke, Y. Jin, X. Wen and C. Ye, *Sci. Technol. Adv. Mater.*, 2023, **24**, 2162323.
9 B. Mohammad, M. A. Jaoude, V. Kumar, D. M. Al Homouz, H. A. Nahla, M. Al-Qutayri and N. Christoforou, *Nanotechnol. Rev.*, 2016, **5**, 311–329.
10 A. Wedig, M. Luebben, D.-Y. Cho, M. Moors, K. Skaja, V. Rana, T. Hasegawa, K. K. Adepalli, B. Yildiz, R. Waser and I. Valov, *Nat. Nanotechnol.*, 2016, **11**, 67–74.
11 D. Kuzum, S. Yu and H.-S. Philip Wong, *Nanotechnology*, 2013, **24**, 382001.
12 M. Müller, I. Efe, M. F. Sarott, E. Gradauskaite and M. Trassin, *ACS Appl. Electron. Mater.*, 2023, **5**, 1314–1334.
13 P. Basnet, D. G. Pahinkar, M. P. West, C. J. Perini, S. Graham and E. M. Vogel, *J. Mater. Chem. C*, 2020, **8**, 5092–5101.
14 I. Zrinski, D. Knapic, A. W. Hassel and A. I. Mardare, *J. Electrochem. Sci. Eng.*, 2023, **13**, 805–815.
15 D. Knapic, E. Anatasova, I. Zrinski, A. W. Hassel and A. I. Mardare, *Phys. Status Solidi A*, 2024, **221**, 2300878.
16 I. Zrinski, C. C. Mardare, L.-I. Jinga, J. P. Kollender, G. Socol, A. Minenkov, A. W. Hassel and A. I. Mardare, *Nanomaterials*, 2021, **11**, 666.
17 T. V. Kundozerova, A. M. Grishin, G. B. Stefanovich and A. A. Velichko, *IEEE Trans. Electron Devices*, 2012, **59**, 1144–1148.
18 G. Leonetti, M. Fretto, K. Bejtka, E. S. Olivetti, F. C. Pirri, N. De Leo, I. Valov and G. Milano, *Phys. Chem. Chem. Phys.*, 2023, **25**, 14766–14777.
19 I. Zrinski, M. Löfler, J. Zavašnik, C. Cancellieri, L. Jeurgens, A. Hassel and A. Mardare, *Nanomaterials*, 2022, **12**, 813.
20 A. Zaffora, D. Cho, K. Lee, F. Di Quarto, R. Waser, M. Santamaria and I. Valov, *Adv. Mater.*, 2017, **29**, 1703357.
21 I. Zrinski, A. Minenkov, C. C. Mardare, J. P. Kollender, S. A. Lone, A. W. Hassel and A. I. Mardare, *Appl. Surf. Sci.*, 2021, **565**, 150608.
22 V. Aglieri, G. Lullo, M. Mosca, R. Macaluso, A. Zaffora, F. Di Franco, M. Santamaria, U. Lo Cicero and L. Razzari, *in 2018 IEEE 4th International Forum on Research and Technology for Society and Industry (RTSI)*, *IEEE*, 2018, 1–4.
23 V. Aglieri, A. Zaffora, G. Lullo, M. Santamaria, F. Di Franco, U. Lo Cicero, M. Mosca and R. Macaluso, *Superlattices Microstruct.*, 2018, **113**, 135–142.
24 D. Knapic, E. Atanasova, I. Zrinski, A. W. Hassel and A. I. Mardare, *Coatings*, 2024, **14**, 446.
25 D. Sanjay Khone, S. Bera and A. Singh Rana, *Mater. Today Proc.*, 2023, DOI: 10.1016/j.matpr.2023.03.238.
26 S.-B. Hua, T. Jin and X. Guo, *Int. J. Extrem. Manuf.*, 2024, **6**, 032008.
27 Q. Xia and J. J. Yang, *Nat. Mater.*, 2019, **18**, 309–323.
28 F. Zahoor, F. A. Hussin, U. B. Isyaku, S. Gupta, F. A. Khanday, A. Chattopadhyay and H. Abbas, *Discover Nano*, 2023, **18**, 36.
29 A. Yesil, F. Gül and Y. Babacan, *Memristor and Memristive Neural Networks*, InTech, 2018.
30 M. M. Lohrengel, *Mater. Sci. Eng., R*, 1993, **11**, 243–294.
31 I. Zrinski, A. Minenkov, C. Cancellieri, R. Hauert, C. C. Mardare, J. P. Kollender, L. P. H. Jeurgens, H. Groiss, A. W. Hassel and A. I. Mardare, *Appl. Mater. Today*, 2022, **26**, 101270.
32 S. Abdul Hadi, K. M. Humood, M. Abi Jaoude, H. Abunahla, H. F. Al Shehhi and B. Mohammad, *Sci. Rep.*, 2019, **9**, 9983.
33 C. Hao, J. Peng, R. Zierold and R. H. Blick, *Adv. Mater. Technol.*, 2024, **9**, 2301762.
34 H. B. Profijt, S. E. Potts, M. C. M. van de Sanden and W. M. M. Kessels, *J. Vac. Sci. Technol., A*, 2011, **29**, DOI: 10.1116/1.3609974.
35 K. Islam, R. Sultana and R. Mroczyński, *Materials*, 2025, **18**, 3454.
36 C. Chen, Y. Cheng, Q. Dai and H. Song, *Sci. Rep.*, 2015, **5**, 17684.
37 P. Borowski and J. Myśliwiec, *Coatings*, 2025, **15**, 922.
38 D. G. Coronell, E. W. Egan, G. Hamilton, A. Jain, R. Venkatraman and B. Weitzman, *Thin Solid Films*, 1998, **333**, 77–81.

39 A. Brenna, F. Corinto, S. Noori, M. Ormellese, M. Pedeferri and M. V. Diamanti, *Advances in Memristor Neural Networks – Modeling and Applications*, InTech, 2018.
40 M. Loizos, K. Rogdakis, A. P. Parambil, M. Lira-Cantu and E. Kymakis, *APL Energy*, 2024, **2**, 040901.
41 C. Lee, I. Kim, W. Choi, H. Shin and J. Cho, *Langmuir*, 2009, **25**, 4274–4278.
42 X. Zhao, S. Menzel, I. Polian, H. Schmidt and N. Du, *Nanomaterials*, 2023, **13**, 1325.
43 R. Khan, N. Ilyas, M. Z. M. Shamim, M. I. Khan, M. Sohail, N. Rahman, A. A. Khan, S. N. Khan and A. Khan, *J. Mater. Chem. C*, 2021, **9**, 15755–15788.
44 X. Liao, Y. Jiang, L. Wang, J. Li, Z. Hou, K. L. Choy and Z. Li, *Nanomaterials*, 2025, **15**, 1674.
45 E. Amrani, A. Drori and S. Kvatinsky, *2016 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), IEEE*, 2016, 1–5.
46 I. Zrinski, A. Minenkov, C. Cancellieri, C. Cela Mardare, H. Groiss, A. Walter Hassel and A. Ionut Mardare, *Appl. Surf. Sci.*, 2023, **613**, 155917.
47 I. Zrinski, A. Minenkov, C. C. Mardare, A. W. Hassel and A. I. Mardare, *J. Phys. Chem. Lett.*, 2021, **12**, 8917–8923.
48 I. Zrinski, A. Minenkov, J. Duchoslav, C. C. Mardare, H. Groiss, A. W. Hassel and A. I. Mardare, *Phys. Status Solidi A*, 2022, 2100751.
49 A. R. Patil, T. D. Dongale, R. K. Kamat and K. Y. Rajpure, *Mater. Today Commun.*, 2023, **34**, 105356.
50 N. S. Sterin, T. Nivedya, S. S. Mal and P. P. Das, *J. Mater. Sci.: Mater. Electron.*, 2022, **33**, 2101–2115.
51 M. Lanza, H.-S. P. Wong, E. Pop, D. Ielmini, D. Strukov, B. C. Regan, L. Larcher, M. A. Villena, J. J. Yang, L. Goux, A. Belmonte, Y. Yang, F. M. Puglisi, J. Kang, B. Magyari-Köpe, E. Yalon, A. Kenyon, M. Buckwell, A. Mehonic, A. Shluger, H. Li, T. Hou, B. Hudec, D. Akinwande, R. Ge, S. Ambrogio, J. B. Roldan, E. Miranda, J. Suñe, K. L. Pey, X. Wu, N. Raghavan, E. Wu, W. D. Lu, G. Navarro, W. Zhang, H. Wu, R. Li, A. Holleitner, U. Wurstbauer, M. C. Lemme, M. Liu, S. Long, Q. Liu, H. Lv, A. Padovani, P. Pavan, I. Valov, X. Jing, T. Han, K. Zhu, S. Chen, F. Hui and Y. Shi, *Adv. Electron. Mater.*, 2019, **5**, 1800143.
52 R. Wang, J.-Q. Yang, J.-Y. Mao, Z.-P. Wang, S. Wu, M. Zhou, T. Chen, Y. Zhou and S.-T. Han, *Adv. Intell. Syst.*, 2020, **2**, 2000055.
53 Y.-H. Wang, T.-C. Gong, Y.-X. Ding, Y. Li, W. Wang, Z.-A. Chen, N. Du, E. Covi, M. Farronato, D. Ielmini, X.-M. Zhang and Q. Luo, *J. Electron. Sci. Technol.*, 2022, **20**, 100177.
54 I. Zrinski, J. Zavašnik, J. Duchoslav, A. W. Hassel and A. I. Mardare, *Nanomaterials*, 2022, **12**, 3944.
55 N. Ghenzi and P. Levy, *Microelectron. Eng.*, 2018, **193**, 13–17.
56 W. Zuo, Q. Zhu, Y. Fu, Y. Zhang, T. Wan, Y. Li, M. Xu and X. Miao, *J. Semicond.*, 2023, **44**, 053102.
57 A. G. Isaev, O. O. Permyakova and A. E. Rogozhin, *Russ. Microelectron.*, 2023, **52**, 74–98.
58 Z. Zhang, Y. Wang, Y. Luo, Y. He, M. Ma, R. Yang and H. Li, *Sci. Rep.*, 2018, **8**, 12617.
59 I. Valov, R. Waser, J. R. Jameson and M. N. Kozicki, *Nanotechnology*, 2011, **22**, 254003.
60 X. Guo, Q. Wang, X. Lv, H. Yang, K. Sun, D. Yang, H. Zhang, T. Hasegawa and D. He, *Nanoscale*, 2020, **12**, 4320–4327.
61 I. Zrinski, C. C. Mardare, L.-I. Jinga, J. P. Kollender, G. Socol, A. W. Hassel and A. I. Mardare, *Appl. Surf. Sci.*, 2021, **548**, 149093.
62 A. Zaffora, R. Macaluso, H. Habazaki, I. Valov and M. Santamaria, *Electrochim. Acta*, 2018, **274**, 103–111.
63 J. Chen, C. Huang, C. Chiu, Y. Huang and W. Wu, *Adv. Mater.*, 2015, **27**, 5028–5033.
64 T. Tsuruoka, I. Valov, S. Tappertzhofen, J. van den Hurk, T. Hasegawa, R. Waser and M. Aono, *Adv. Funct. Mater.*, 2015, **25**, 6374–6381.
65 F.-C. Chiu, *Adv. Mater. Sci. Eng.*, 2014, **2014**, 1–18.
66 E. Lim and R. Ismail, *Electronics*, 2015, **4**, 586–613.
67 G. U. Kamble, N. P. Shetake, S. D. Yadav, A. M. Teli, D. S. Patil, S. A. Pawar, M. M. Karanjkar, P. S. Patil, J. C. Shin, M. K. Orlowski, R. K. Kamat and T. D. Dongale, *Int. Nano Lett.*, 2018, **8**, 263–275.
68 W. Banerjee, Q. Liu and H. Hwang, *J. Appl. Phys.*, 2020, **127**, 051101.
69 F. Di Franco, A. Zaffora, M. Santamaria and F. Di Quarto, *Encyclopedia of Interfacial Chemistry*, Elsevier, 2018, pp. 26–40.
70 G. D. Sulka, *Nanostructured Anodic Metal Oxides*, Elsevier, 2020, pp. 1–34.
71 P. Jančovič, B. Hudec, E. Dobročka, J. Dérer, J. Fedor and K. Fröhlich, *Appl. Surf. Sci.*, 2014, **312**, 112–116.
72 W. He, H. Sun, Y. Zhou, K. Lu, K. Xue and X. Miao, *Sci. Rep.*, 2017, **7**, 10070.
73 H. Baek, C. Lee, J. Choi and J. Cho, *Langmuir*, 2013, **29**, 380–386.
74 K. Lee, J. Kim, I.-S. Mok, H. Na, D.-H. Ko, H. Sohn, S. Lee and R. Sinclair, *Thin Solid Films*, 2014, **558**, 423–429.
75 T. H. Park, S. J. Song, H. J. Kim, S. G. Kim, S. Chung, B. Y. Kim, K. J. Lee, K. M. Kim, B. J. Choi and C. S. Hwang, *Sci. Rep.*, 2015, **5**, 15965.
76 J.-H. Ryu, F. Hussain, C. Mahata, M. Ismail, Y. Abbas, M.-H. Kim, C. Choi, B.-G. Park and S. Kim, *Appl. Surf. Sci.*, 2020, **529**, 147167.
77 L. Hu, W. Han and H. Wang, *Nanotechnology*, 2020, **31**, 155202.
78 B. J. Choi, D. S. Jeong, S. K. Kim, C. Rohde, S. Choi, J. H. Oh, H. J. Kim, C. S. Hwang, K. Szot, R. Waser, B. Reichenberg and S. Tiedke, *J. Appl. Phys.*, 2005, **98**, 033715.
79 Y. Rong, Y. Yang, M. Lv, Y. Liu, C. Wang, D. Cui, Y. Liu, C.-F. Yu and G. Wei, *J. Vac. Sci. Technol., B*, 2025, **43**, 022208.
80 M. Zych, K. Syrek, L. Zaraska and G. D. Sulka, *Molecules*, 2020, **25**, DOI: 10.3390/molecules25122916.
81 M. V. Diamanti, R. Pisoni, A. Cologni, A. Brenna, F. Corinto and M. Pedeferri, *J. Appl. Biomater. Funct. Mater.*, 2016, **14**, e290–e295.
82 I. B. Dorosheva, A. S. Vokhmintsev, R. V. Kamalov, A. O. Gryaznov and I. A. Weinstein, *2018 Ural Symposium*

on Biomedical Engineering, Radioelectronics and Information Technology (USBEREIT), IEEE, 2018, 279–282.
83 A. Zaffora, F. Di Quarto, H. Habazaki, I. Valov and M. Santamaria, *Faraday Discuss.*, 2019, **213**, 165–181.
84 D. A. Vermilyea, *J. Electrochem. Soc.*, 1957, **104**, 427.
85 N. Khalil and J. S. L. Leach, *Electrochim. Acta*, 1986, **31**, 1279–1285.
86 J. P. S. Pringle, *Electrochim. Acta*, 1980, **25**, 1423–1437.
87 P. Roy, S. Kunwar, D. Zhang, D. Chen, Z. Corey, B. X. Rutherford, H. Wang, J. L. MacManus-Driscoll, Q. Jia and A. Chen, *Adv. Electron. Mater.*, 2022, **8**, 2101392.
88 H. J. Lee, J.-H. Kim, H.-J. Kim and S.-N. Lee, *Materials*, 2024, **17**, 2727.
89 C. Nyenke and L. Dong, *Microelectron. Eng.*, 2016, **164**, 48–52.
90 D. Lee, M. Chae and H.-D. Kim, *Sens. Actuators, B*, 2024, **401**, 135063.
91 N. Caporale and Y. Dan, *Annu. Rev. Neurosci.*, 2008, **31**, 25–46.
92 L. Chen, W. Zhou, C. Li and J. Huang, *Neurocomputing*, 2021, **456**, 126–135.
93 J. Jang, S. Gi, I. Yeo, S. Choi, S. Jang, S. Ham, B. Lee and G. Wang, *Adv. Sci.*, 2022, **9**, 2201117.
94 X. Zhang, A. Huang, Q. Hu, Z. Xiao and P. K. Chu, *Phys. Status Solidi A*, 2018, **215**, 1700875.
95 N. S. M. Hadis, A. Abd Manaf, S. H. Herman and S. H. Ngalim, *2015 IEEE SENSORS, IEEE*, 2015, 1–4.
96 X. Ji, X. Zhao, M. C. Tan and R. Zhao, *Adv. Intell. Syst.*, 2020, **2**, 1900118.
97 Q. Chen, L. Lu, J. Meng, M. Xu and T. Wang, *Research*, 2025, **8**, 0916.
98 J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart and R. S. Williams, *Nature*, 2010, **464**, 873–876.
99 S. Kvatinsky, G. Satat, N. Wald, E. G. Friedman, A. Kolodny and U. C. Weiser, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, 2014, **22**, 2054–2066.
100 E. Atanasova, A. Greul, A. Udovicic, A. W. Hassel and A. I. Mardare, *Phys. Status Solidi A*, 2025, **222**, 2500236.
101 N. Natarajan and P. Kuppusamy, *Mater. Sci. Pol.*, 2025, **43**, 196–209.
102 A. V. Saenko, R. V. Tominov, I. L. Jityaev, Z. E. Vakulov, V. I. Avilov, N. V. Polupanov and V. A. Smirnov, *Nanomaterials*, 2024, **14**, 1901.