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# Low-frequency noise in nanowires

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40 years of research on low-frequency (LF) noise and random-telegraph noise (RTN) in metallic and semiconducting nanowires (NWs) demonstrate the importance of defects and impurities to each system. The fluctuating interference of electrons in the local environment of a mobile bulk defect or impurity can lead to LF noise, RTN, and device-to-device variations in metallic and semiconducting NWs. Scattering centers leading to mobility fluctuations in semiconducting NWs include random dopant atoms and bulk defect clusters. Effective energy distributions for the relevant defects and impurities can be obtained from noise *versus* temperature measurements in conjunction with the Dutta–Horn model of LF noise for both metallic and semiconducting NWs. In semiconducting NWs configured as metal-oxide-semiconductor field-effect transistors, fluctuations in carrier number due to charge exchange with border traps, such as oxygen vacancies and/or their complexes with hydrogen in adjacent or surrounding dielectrics, often dominate or add to bulk noise sources.

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## I. Introduction

Size and scale matter. The transitions from classical to quantum regimes and bulk to surface-dominated responses have been intense areas of study over the last century. In recent decades, metallic and semiconducting nanowires (NWs) have enabled investigations of a wide range of phenomena including Anderson localization, electron–electron interactions, and quantum-mechanical decoherence;[1–23] magnetism, including Aharonov–Bohm oscillations and the Kondo effect;[11,18,23–39] superconductivity, macroscopic quantum tunnelling, and Majorana bound states;[39–50] and low-frequency noise, random-telegraph noise, and universal conductance fluctuations.[51–77]

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When pioneering experimental studies of localization and electron–electron interactions were performed on metallic NWs fabricated *via* substrate step methods in 1979–1982,[5–9] the semiconductor industry was transitioning from the micron to the submicron scale.[78–81] For several decades, typical metal-oxide-semiconductor field-effect transistor (MOSFET) channel dimensions were several orders of magnitude larger than mesoscale and nanoscale NWs.[5–9,12,20] As microelectronic fabrication techniques advanced, NW fabrication techniques evolved from substrate step and templating methods to state-of-the-art lithography capable of producing nanostructures in volume and integrating semiconductor NWs into architectures that facilitate fabrication and measurement.[5–9,12,20,71–77,81,82]

This paper reviews the evolution of low-frequency (LF) and random-telegraph noise (RTN) in metallic and semiconducting NWs over the last ~40 years. Defects and impurities are critical to the noise of each system. Metal NWs are passive devices; semiconducting NWs typically are built as active devices. The noise of semiconducting NWs is especially important to future analog integrated circuits (ICs), since LF noise and RTN often limit their accuracy and precision.[55,60,66,81]

This review is organized as follows. Section II presents an overview of LF noise and RTN in metals and semiconductor devices. The Dutta–Horn model of thermally-activated $1/f$

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noise, where $f$ is the frequency, and the number fluctuation model of LF noise in MOSFETs are emphasized.[55,66,73,76] LF noise and RTN of metallic NWs are discussed in Section III; representative results for semiconducting NWs with Si and III–V semiconductor channels are shown in Section IV. Bulk noise persists over large volumes in metallic NWs.[51,71,83] Fluctuations due to single defects become increasingly common in highly scaled devices of each type.[15,53–58,66,74–77,84–90] These results illustrate the diversity of mechanisms that can lead to conductivity fluctuations in metallic and semiconducting NWs.

## II. Overview of low-frequency noise

**II.A. Metals.** Metallic nanowires are resistors; any resistive system exhibits noise. Thermal noise in a resistor of any size, shape, material, or composition results from the Brownian motion of charge and has voltage-noise power spectral density $S_{V_t}$ (in units of $V^2\ Hz^{-1}$) of

$$S_{V_t} = 4kTR. \tag{1}$$

Here $T$ is the absolute temperature, $k$ is Boltzmann's constant, and $R$ is the resistance.[55,66,91,92] When current $I$ is passed through a resistor, there is often "excess noise," after thermal noise $S_{V_t}$ is subtracted, with power-spectral density $S_V$ approximately proportional to $1/f$. For an ohmic system, $S_V/V^2 = S_I/I^2 = S_R/R^2$; $V$ is the voltage and $S_I$ and $S_R$ are the respective current-noise and resistance-noise power spectral densities.[55,66] Low-frequency noise in metals is often parameterized by Hooge's empirical formula,[55,66,93–95]

$$\frac{S_V}{V^2} = \frac{\gamma_H}{N_C f}. \tag{2}$$

Here $\gamma_H$ is a dimensionless figure of merit proportional to noise magnitude and $N_C$ is the number of channel carriers. For a metal, it is usually assumed that $N_C \approx N_A$, where $N_A$ is the number of atoms.[51,55,95]

Fig. 1 shows a room-temperature LF noise spectrum for a first-generation sputtered-platinum NW fabricated using substrate step lithography *via* the process sequence shown schematically in Fig. 2.[5,7,8,51] NWs fabricated *via* substrate step lithography are poly-crystalline, with grain sizes less than wire diameters.[5,7–9,16,20,51–54] The noise magnitude of the NW in Fig. 1 increases as $1/f^{1.15}$ over nearly five decades in frequency. The Hooge parameter at $f$ = 1 Hz is $\gamma_H \cong 3 \times 10^{-4}$, a typical value for sputtered Pt wires and thin films.[51,71,96,97] The $1/N \approx 1/N_A$ dependence of the noise magnitude in eqn (2) presumes a bulk origin for the fluctuations.

Several key experiments in the late 1970s through mid-1980s demonstrate the crucial roles of defects and impurities in LF noise in metals.[52,55,66,83,95,98–103] One defect with a single characteristic scattering or transition time $\tau$ leads to RTN with a Lorentzian spectrum that falls off as $1/f^2$ at frequencies above $1/\tau$ and is constant at frequencies below $1/\tau$.[55,62,66,95,104–106] An example is shown for a ZnO NW in Section II.B. If instead the noise results from multiple defects having a distribution of

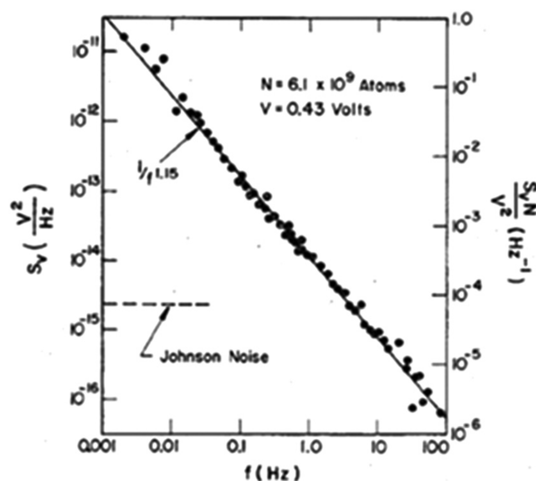


Fig. 1 Excess voltage-noise power spectral density $S_V$ as a function of frequency $f$ for a Pt nanowire (NW) fabricated *via* substrate step lithography. The Johnson (thermal) noise background has been subtracted. The size and voltage normalized noise, $S_V N/V_r^2$ is shown on the right-h and $y$-axis, with $N = N_A$. Reproduced from ref. 51 with permission. Copyright 1983 The American Physical Society.

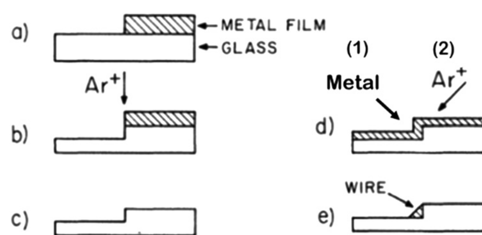


Fig. 2 Schematic illustration of substrate step lithography. (a) Metal is deposited onto the unmasked portion of a glass slide. (b) The masking metal is removed *via* argon ion milling, leaving behind (c) a step in the substrate. (d) Step 1: metal is deposited at an angle favoring step filling. Step 2: without breaking vacuum, argon ion milling removes all metal except that shadowed by the step, leaving (e) a nanowire. Adapted from ref. 5 with permission. Copyright 1979 The American Physical Society.

characteristic times $D(\tau)$, and if $D(\tau) \sim 1/\tau$ for times $\tau_1 < \tau < \tau_2$, then the integrated noise,

$$S_V = C\int [D(\tau)/(1+\omega^2\tau^2)]\mathrm{d}\tau \tag{3}$$

is proportional to $\sim 1/f$ for $1/\tau_2 < f < 1/\tau_1$.[55,66,95,104,105] Here $\omega = 2\pi f$ and $C$ is a frequency-independent parameter that is proportional to the noise magnitude. If the noise results from a random, thermally activated process, as is often the case,[52,66,95,104,107] then

$$\tau = \tau_0 e^{E/kT}, \tag{4}$$

where $\tau_0$ is the characteristic time and $E$ is the activation energy. When $D(E)$ is nearly constant in the range $kT\ln(\tau_2/\tau_0) \leq E \leq kT\ln(\tau_1/\tau_0)$, the condition that $D(\tau)$ is proportional to $\sim 1/\tau$ is satisfied, and $1/f$ noise is observed.[55,95,104,105] This follows directly from the solution of eqn (3), with an exchange of variables ($\tau$, $E$).[104,105]

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Dutta and Horn extended this approach to show that, if the noise is caused by a random thermally activated process that is not approximately constant in energy, but changes in the distribution occur slowly with respect to $kT$, the frequency and temperature dependences of the noise are correlated *via*:[52,55,66,95]

$$\alpha(\omega, T) = 1 - \frac{1}{\ln(\omega\tau_0)}\left(\frac{\partial \ln S_V(T)}{\partial \ln T} - 1\right), \tag{5}$$

where $\alpha = -\partial \ln S_V / \partial \ln f$. When the measured frequency and temperature dependences of the noise follow eqn (5), the effective defect-energy distribution $D(E_0)$ can be estimated *via*:[52,55,66,73,95]

$$D(E_0) \propto \frac{\omega}{kT} S_V(\omega, T). \tag{6}$$

The energy that corresponds to a given temperature in a plot of $S_V$ *vs.* $T$ can be estimated to first order *via*:[55,66,95,107]

$$E_0 \approx -kT \ln(\omega\tau_0). \tag{7}$$

Fig. 3 shows normalized noise as a function of temperature for Pt NWs similar to those in Fig. 1.[96] The energy scale inferred from eqn (7) is shown on the upper $x$-axis, assuming $\tau_0 \approx 10^{-14}$ s, a typical value for metals.[55,66,95] The noise of the two wires differs by less than a factor of 2 up to ~300 K, with more significant differences at higher temperatures and energies.[96] Additional studies of the temperature dependence of the noise of metallic NWs are shown in Section III.

For thin metal films and NWs, variations in scattering rates caused by defect and/or impurity motion and/or the reconfiguration of bulk defect complexes often are dominant sources of $1/f$ noise.[52,55,66,86,95] In most cases, the noise is due to the fluctuating interference of electrons in the local environment of a moving defect or impurity.[55,86] At low temperatures, the noise may also be due to universal conductance fluctuations (UCF), in which the motion of one strong scattering center leads to conductance fluctuations of order $q^2/h$, where $q$ is the magnitude of the electron charge and $h$ is Planck's constant.[15,85] Examples are shown in Section III.

**II.B. Semiconductor devices.** Semiconducting nanowires are often fabricated in a MOSFET configuration.[59–74] This passivates the NW surface and facilitates charge control. The MOSFET structure typically includes significant densities of charge traps in adjacent or surrounding dielectrics (Fig. 4). The LF noise of semiconductor NWs in a MOSFET configuration usually is caused by similar processes that lead to noise in planar MOSFETs or FinFETs. These are fluctuations in carrier number due to carrier trapping and emission, and/or trap activation and passivation, and fluctuations in carrier mobility due to time-dependent variations in carrier scattering rates.[55,66,93–95,107–115] The inherently small volumes and large surface-to-volume ratios of NWs can lead to enhanced $1/f$ noise magnitudes and RTN, compared with devices of larger dimension, as illustrated in Section IV.[59–74]

When contact noise is controlled effectively during device fabrication, near-interfacial oxide traps (border traps) can lead to LF noise and RTN in MOSFETs.[56,66,73,74,76,77,90,107–124] In the Si MOS literature, particularly before the early 1990s, these defects are often erroneously called interface traps (or states).[113,116] This term should be applied only to defects at the interface that are in rapid communication with the channel, typically on ~μs time scales for Si MOS devices.[66,73,90,107,113,116–119,125,126] In contrast, charge exchange times for border traps of relevance to LF noise measurements typically are ms to s (or longer) in Si MOS devices.[113,116,118,119,125] Note that, for wide band-gap (WBG) semiconductors, *e.g.*, SiC and GaN, separating effects of interface and border traps on device response and/or LF noise is more challenging than for Si, Ge, GaAs, and other narrow gap semiconductors, due to the significant overlap between time constants for deep interface traps and border traps in WBG devices.[55,66,113,116,118,123,126,127]

Fig. 4 schematically illustrates an nMOS transistor biased in inversion. For constant drain current $I_{DS}$ and gate bias $V_{GS}$

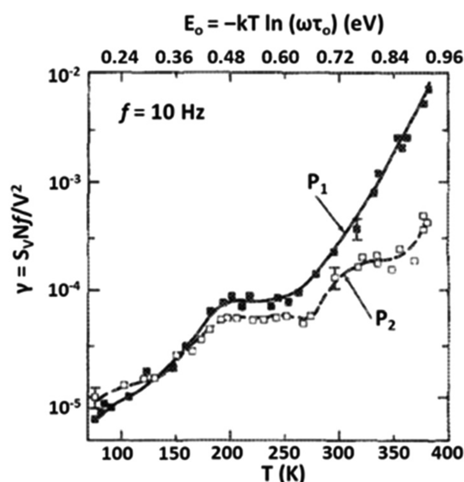


**Fig. 3** Normalized noise magnitude *vs.* temperature for two Pt NWs. The energy $E_0$ that corresponds to the temperature $T$ *via* eqn (7) is shown on the upper $x$-axis, assuming $\tau_0 \approx 10^{-14}$ Hz. Adapted from ref. 96 with permission. Copyright 1987 American Institute of Physics.

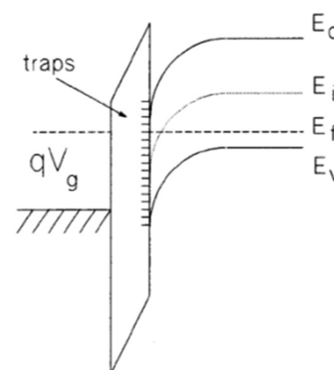


**Fig. 4** Schematic band diagram for an nMOS transistor biased in inversion. Reproduced from ref. 112 with permission. Copyright 1991 Institute of Electrical and Electronics Engineers.

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in the linear region of MOS operation, fluctuations in trapped charge density and occupancy $\delta Q_t$ have an effect that is equivalent to fluctuations in gate voltage $\delta V_{GS}$:[73,108,112]

$$\delta V_{GS} = \frac{\delta Q_t}{C_{ox}} = q\frac{\delta N_t}{C_{ox}}. \quad (8)$$

$C_{ox} = \varepsilon_{ox}/t_{ox}$ is the oxide capacitance per unit area, $\varepsilon_{ox}$ is the insulator dielectric constant, $t_{ox}$ is the gate insulator thickness, and $N_t$ is the areal trap density. Fluctuations in $\delta V_{GS}$ lead to fluctuations in drain voltage $\delta V_{DS}$:[73,108,112]

$$\delta V_{DS} = \frac{\partial V_{DS}}{\partial I_{DS}}\frac{\partial I_{DS}}{\partial V_{GS}}\delta V_{GS}. \quad (9)$$

$\partial I_{DS}/\partial V_{GS} = g_m$ is the transconductance and $(\partial V_{DS}/\partial I_{DS})^{-1} \approx \partial I_{DS}/\partial V_{DS}$ is the output conductance. In terms of $\delta N_t$, this becomes:[73,108,112]

$$\partial V_{DS} = \frac{qV_{DS}}{C_{ox}(V_{GS} - V_{TH})}\delta N_t. \quad (10)$$

$V_{TH}$, $V_{GS}$, and $V_{DS}$ are the threshold, gate, and drain voltages, respectively. In the linear mode of transistor operation, where the device can be treated as a gated resistor, the areal density of carriers in the channel $n_c$ is approximately[76,93,94,110,111]

$$n_c \approx \frac{C_{ox}(V_{GS} - V_{TH})}{q}. \quad (11)$$

Again, when individual defects dominate device response, RTN and Lorentzian power spectra are observed,[55,56,59,62,66,88,95,104–106] as shown for a ZnO NW in Fig. 5. RTN is shown in the inset; the resulting power spectrum has a $1/f^2$ corner frequency of ~18 Hz for a NW measured in vacuum at a temperature of 4.2 K.[62]

For RTN due to one or a few prominent border traps, the expected change in drain current $I_{DS}$ in the linear mode of device operation in a simple number-fluctuation model (neglecting mobility fluctuations) is:[76,110,111]

$$\left|\frac{\Delta I_{DS}}{I_{DS}}\right| = \frac{1}{N_C} \approx \frac{q}{AC_{ox}(V_{GS} - V_{TH})}. \quad (12)$$

Here $A$ is the cross-sectional area of the channel. For cases in which RTN magnitudes exceed the level of eqn (12) by a significant amount, mobility fluctuations also must be considered, as discussed below.[76,110,111,115]

When more than a few defects are active on the time scales of the measurements, $1/f$ noise is observed.[55,66,73,84,112] The excess drain-voltage noise power spectral density $S_{V_d}$ can be related *via* eqn (10) to fluctuations in the trapped charge density in the near-interfacial dielectric:[73,108,112]

$$S_{V_d}(f,T) = \frac{q^2 V_{DS}^2}{C_{OX}^2(V_{GS} - V_{TH})^2} S_{N_t}(f,T). \quad (13)$$

Thus, in the number fluctuation model of low frequency noise, $S_{V_d}$ is proportional to $1/N_{C2}$. This contrasts with eqn (2), in which $S_{V_d}$ is proportional to $1/N_C$.[76,93,94,110,111] The ability to modify $N_C$ within a given device for MOS transistors provides information on the nature of the fluctuations not often available for metals.[51,55,76,93–95,110,111] Indeed, measurements of LF noise *vs.* current and/or voltage, and thus $N_C$, are often performed on MOS devices to attempt to differentiate bulk noise due to fluctuations in carrier scattering rates from surface noise due to fluctuations in occupancy of border traps.[93,94,111,115] However, these tests are open to multiple interpretations, as discussed below, so additional information typically is required to determine whether bulk or surface noise dominates the response of a particular device.[66,73,128]

For simplicity in calculation, it is commonly assumed that the exchange of charge between the device channel and border traps occurs *via* tunneling, and that defects are distributed approximately uniformly in space within the gate insulator and in energy within the Si band gap.[73,108–115] With these simplifying assumptions, fluctuations in the density of traps $N_t$ lead to a power-spectral density $S_{N_t}$:[73,108,112]

$$S_{N_t}(f,T) = \frac{kTD_{BT}(E_f)}{A\ln(\tau_2/\tau_1)f}. \quad (14)$$

In this case $N_t = D_{BT}(E_f)$ is the effective number of border traps per unit energy and area at the Fermi level $E_f$, and $\tau_1$ and $\tau_2$ are minimum and maximum tunneling times. Combining eqn (13) and (14) yields a first-order expression that relates $S_{V_d}$ to $D_{BT}(E_f)$ in the linear mode of transistor response:[73,108,112]

$$S_{V_d} = \frac{q^2 V_{DS}^2 kTD_{BT}(E_f)}{C_{OX}^2(V_{GS} - V_{TH})^2 A\ln(\tau_2/\tau_1)f}. \quad (15)$$

Hence, when MOS $1/f$ noise is due primarily to border traps, $D_{BT}$ is an effective measure of relative noise magnitude.[66,93,113–115,117,118]

In a first-order number fluctuation model, $S_{I_d}/I_d^2$ is proportional to $(g_m/I_d)^2$ in both linear and saturation modes of transistor operation.[111,115,129] Electric fields are stronger and

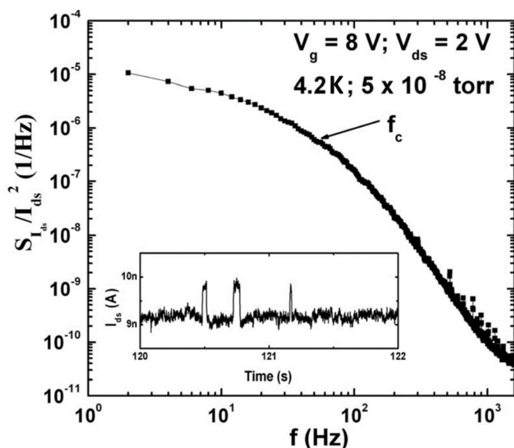


Fig. 5 Lorentzian noise power spectrum for a ZnO NW exhibiting random telegraph noise, RTN, at a temperature of 4.2 K. The corner frequency $f_c$ is ~18 Hz. The inset plots current *vs.* time. Reproduced from ref. 62 with permission. Copyright 2007 American Institute of Physics.



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less uniform in saturation than in the linear mode. Thus, deviations from nominal response often are observed as voltage and current increase in a MOS transistor, particularly when surface roughness scattering, mobility fluctuations, spatial variations in trap density, and/or areal variations in trap density are significant.[66,73,111,115]

Although good agreement between eqn (15) and complementary methods to estimate border-trap densities in MOSFETs is often observed,[66,90,113,117,118] caution must be used when interpreting results because (1) thermally activated charge exchange is much more common in MOS devices than purely quantum-mechanical tunneling exchange,[66,76,90,130] (2) border-trap energy distributions are often non-uniform in space and/or energy,[66,90,107,128,131–134] and (3) bulk defects and impurities in the device channel also contribute to 1/*f* noise and/or RTN in some MOS devices.[73,74,76,77,110,111,130,135,136]

The Hooge model is often applied to semiconductor devices in an effort to analyze noise due to mobility fluctuations.[55,66,93–95,111,114,137] However, the Hooge model as formulated in 1969 and updated in 1978 attributes the noise to lattice scattering.[93,94,137] The lack of a theoretical foundation, internal inconsistencies, and crucial roles for defects and impurities in the 1/*f* noise of microelectronic devices and materials argue persuasively against Hooge mobility fluctuations as the origin of noise in metals or semiconductor devices.[55,66,76,86,95,128] As a result, the Hooge parameter as defined in eqn (2) is not as useful in comparisons of the relative noise levels of semiconducting devices as it is for metals.[55,66,93–95,114]

Correlated mobility fluctuation (CMF) models are often used to analyze LF noise in semiconductor devices.[76,110,111,115,135,136] In the CMF model, simultaneous changes in charge state and strength of scattering of channel carriers by border traps are inferred to lead to enhanced LF noise over simple number fluctuation predictions *via* eqn (15). In the CMF model of Hung, *et al.*, for example, the input-referred noise power spectral density, $S_{V_g}$, is given by:[110,111,115,135,136]

$$S_{V_g}(f) = \frac{kTq^2}{\gamma f A C_{OX}{}^2}(1 + \alpha\mu N_C)^2 D_{BT}(E_{fn}). \qquad (16)$$

Here $\gamma$ is a tunneling parameter that characterizes attenuation of the electron wave function in the oxide, $\alpha$ is a carrier-defect scattering coefficient, $\mu$ is the effective carrier mobility, $N_C$ is the channel carrier density per unit area, and $E_{fn}$ is the quasi-Fermi level.

It can be challenging to interpret eqn (16) physically. As noted above, charge exchange between the channel and border traps is rarely due to pure tunneling. Moreover, when this charge exchange occurs at capture and emission rates accessible to typical LF noise measurements, the Coulomb interaction between channel carriers and border traps is often too weak to lead to the enhanced scattering in eqn (16), compared with eqn (15), and/or increased RTN, compared with eqn (12), as discussed in Section IV.[76,110,111,115,130,135] It is more likely that the enhanced 1/*f* noise or RTN in these cases is caused by (1) fluctuations in scattering rates caused by random dopants, (2) changes in charge state or configuration of bulk defect clusters in the device channel, and/or (3) fluctuating concentrations of interface traps caused by hydrogen-mediated interface-trap activation and passivation.[76,77,138–144] These are fruitful areas for future study.

Values of $D_{BT}$ often depend strongly on temperature, consistent with the critical role that thermally activated processes play in the LF noise of MOS and other semiconductor devices. Much work over the last ~40 years has demonstrated that the temperature dependence of the noise of semiconductor devices is often described well by the Dutta–Horn model of 1/*f* noise.[66,73,90,95,107,132–134,145–150] Fig. 6 shows an example of the degree of agreement that is often observed, in this case for a SiGe pMOSFET.[133]

Comparative studies of LF noise, radiation response, and bias-temperature instabilities (*e.g.*, Fig. 7 and 8), often supported by first principles calculations, show that O vacancies and/or complexes with hydrogen can lead to LF noise and RTN in MOSFETs with $SiO_2$ or high-K gate dielectrics in a variety of semiconductor technologies and transistor architectures.[66,73,74,90,107,109,112–114,120,122,123,132–134,145,150–153] For nMOSFETs, O vacancies in the strained region of the MOS gate oxide near the channel interface are close enough in energy to the Fermi level to contribute to 1/*f* noise, as illustrated in Fig. 7(a).[66,73,107,133,134] Inferred defect-energy distributions for FinFETs with high-K gate dielectrics are shown in Fig. 7(b) before and after devices were subjected to bias-temperature stress and then irradiated to 2 Mrad($SiO_2$).[154] The increase in LF noise for these and similar devices correlates strongly with O vacancy densities.[109,112,114,131,154–156] For pMOS transistors, density-functional calculations suggest that LF noise and RTN are due to O vacancies complexed with

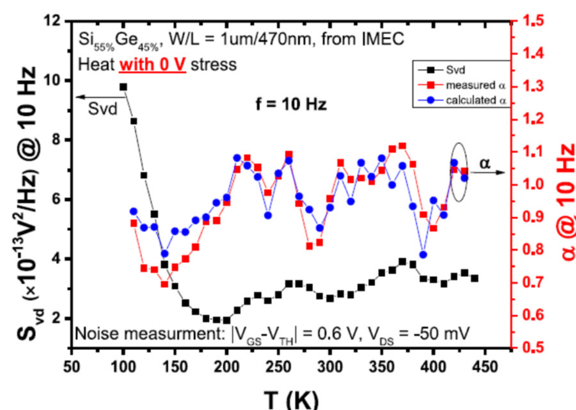


**Fig. 6** Noise magnitude (left *y*-axis) and measured and predicted values of $\alpha = -\partial \ln S_V/\partial \ln f$ *vs.* temperature (right *y*-axis) for a SiGe pMOSFET with $SiO_2/HfO_2$ gate dielectric. Predicted $\alpha$ values are derived from the $S_{V_d}$ *vs.* *T* curve measured before bias-temperature stress, using eqn (5) of the text. Reproduced from ref. 133 with permission. Copyright 2016 Institute of Electrical and Electronics Engineers.

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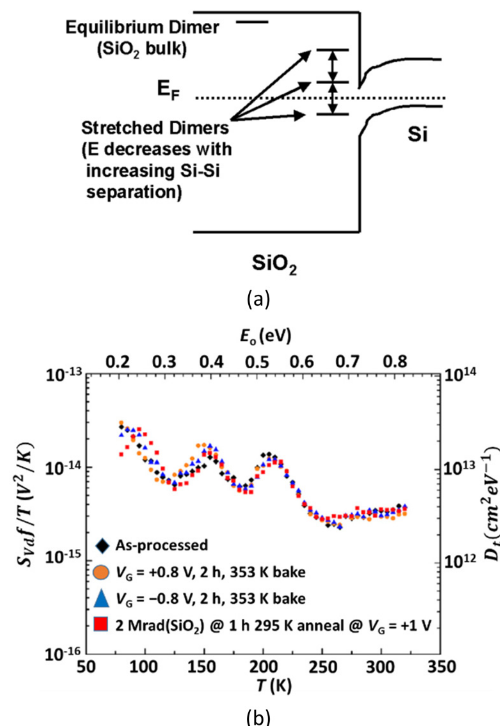


**Fig. 7** (a) Schematic diagram of dimer (unrelaxed) O vacancy energy levels in bulk and near-interfacial $SiO_2$. Band narrowing and near-interfacial strain reduce O vacancy energies, facilitating electron capture. Electron capture relieves strain, increasing the energy, and favoring emission. Reproduced from ref. 107 with permission. Copyright 107 Institute of Electrical and Electronics Engineers. (b) Normalized 1/*f* noise (left *y*-axis) and effective border-trap density from eqn (15) (right *y*-axis) *vs.* temperature for nMOS transistors with $SiO_2/HfO_2$ gate dielectrics before and after bias-temperature stress at 353 K and 10 keV X-ray irradiation to 2 Mrad($SiO_2$). The energy scale on the upper *x*-axis is from eqn (7). Reproduced from ref. 154 with permission. Copyright 2023 Institute of Electrical and Electronics Engineers.

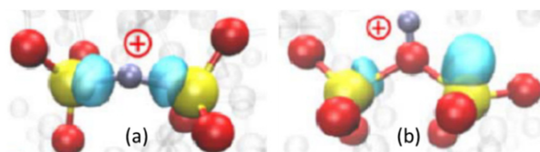


**Fig. 8** Oxygen vacancy complexes with hydrogen that are hole traps during negative-bias-temperature stress, and border traps leading to LF noise and RTN in pMOS transistors: (a) hydrogen bridge – when charged, the central hydrogen atom (small silver ball) is bonded to both Si atoms (large yellow balls), and (b) hydroxyl E′ center – when charged, a bridging O atom (medium red ball) attaches to a H atom. Reproduced from ref. 157 with permission. Copyright 2014 Institute of Electrical and Electronics Engineers.

hydrogen, *e.g.*, in a hydrogen bridge configuration, as in Fig. 8(a), or hydroxyl *E*′ configuration, as in Fig. 8(b).[73,90,157,158]

The LF noise of MOS devices with 2D materials (*e.g.*, graphene, $MoS_2$, BP) as channels typically is dominated by border traps with defect energy distributions similar to those in Fig. 7(b). However, traps at the 2D material surface can introduce sources of scattering-induced noise, RTN, instability, and/or part-to-part variations that can be much larger than observed in Si MOS transistors.[73,121,134,158–165] Finally, carbon nanotube transistors (CNTs) can show a wide range of responses, including giant LF noise if surfaces are unpassivated or if mesh percolation significantly affects transport, border-trap related noise due to charge exchange between the CNT and adjacent oxides, and/or bulk LF noise.[166–173]

Knowing the microstructures of the defects that lead to LF noise and RTN enables process improvements to device response. In older technologies, limiting post-gate-oxidation annealing temperature to ∼875 °C to avoid oxygen out-diffusion from $SiO_2$ and minimizing hydrogen to reduce interface-trap formation can lead to reduced LF noise and enhanced radiation tolerance.[66,73,76,107,109,112,114,132,174,175] In newer, highly scaled technologies, defect-passivation treatments such as high-pressure annealing in hydrogen or deuterium have been effective in reducing LF noise and RTN.[176–179]

## III. Metallic nanowires

As thin-film and NW dimensions shrink, volume *vs.* surface scaling becomes an increasingly significant issue. However, Fig. 9 shows that, for more than six orders of magnitude in volume, an approximate $\sim 1/N_A$ dependence is observed for the noise of Pt thin films and NWs.[51,71] Hence, bulk fluctuations dominate the LF noise.[51] This result was confirmed and extended by Zimmerman, *et al.*,[83] for Cr films with thicknesses from 8–260 nm.

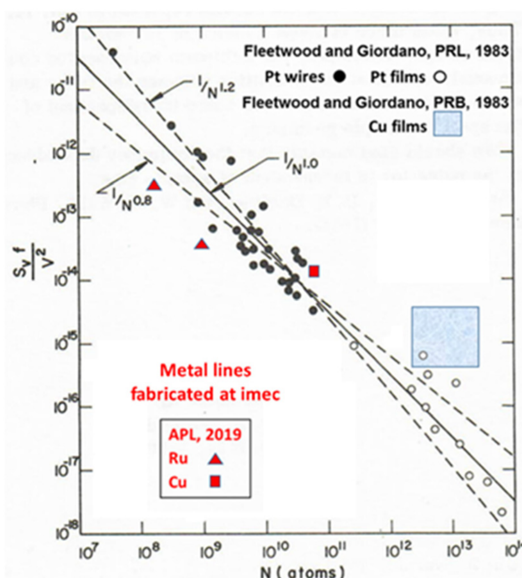


**Fig. 9** $S_V N/V^2$ at 295 K and *f* = 10 Hz for Pt NWs fabricated by substrate step lithography (solid black circles); mechanically scribed, sputtered Pt films (open circles); and mechanically scribed, thermally evaporated Cu films (large, blue box). Lines are proportional to $1/N^{(1.0\pm0.2)}$. Results are compared with Ru (length *L* = 10 μm and 50 μm; red triangles) and Cu resistors fabricated at imec (small red box). Adapted from ref. 71 with permission. Copyright 2019 American Institute of Physics.



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One naturally may wonder how the noise of structures prepared by substrate step lithography and mechanical scribing in Fig. 1, 3, and 7 compares with that of devices prepared *via* state-of-the-art lithography. To address this point, Fig. 9 also includes results for Ru (a Pt group metal) and Cu metal lines fabricated by imec in a modern CMOS fabrication facility[71] and early 1980s results for mechanically scribed Cu metal films.[97] Noise magnitudes are remarkably similar for Pt NWs and Ru resistors of similar dimensions, and for scribed and patterned Cu resistors when scaled for differences in volume. The relatively modest decreases in normalized noise for imec-fabricated Ru and Cu resistors are due simply to the reduced concentrations of defects and impurities in metal lines fabricated *via* modern lithography than in the sputtered Pt NWs and Pt and Cu films fabricated *via* the first-generation techniques of Fig. 1–3.[71]

Giordano discovered in 1980 that as-processed, highly disordered AuPd films showed larger increases in resistance at low temperatures as a result of enhanced carrier localization and/or electron–electron interactions than films of lower resistivity and reduced disorder; these results are shown in Fig. 10.[7] This finding inspired a later experiment in which a series of systematic annealing treatments on disordered AuPd NWs were performed to test the degree to which eqn (5) is satisfied.[52] The results of this study are summarized in Fig. 11. Remarkably close agreement is observed between the experimental results and the predictions of eqn (5) through three measurement and annealing cycles. In Fig. 11(a) the slope of the $S_V$ *vs.* $T$ curve is maximum between ~200 K and ~300 K in an as-processed AuPd NW. This corresponds to the maximum value of $\alpha = -\partial \ln S_V/\partial \ln f$ in Fig. 11(b), consistent with eqn (5). When the resistivity of the NW and the noise magnitude are reduced in Fig. 11(a) as a result of *in situ* heating (curves A and B) or baking in an external oven (between curves B and C), changes in the frequency dependence of the noise again closely follow predictions based on eqn (5). These results clearly show the validity and utility of the Dutta–Horn model of $1/f$ noise.[52,55,66,73,95]

Fig. 12 illustrates the significant differences often observed among temperature-dependent noise magnitudes and inferred

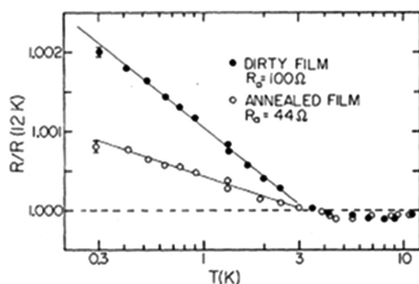


**Fig. 10** Relative resistance *vs.* temperature for an as-processed, sputtered AuPd thin film ("dirty") with sheet resistance of 100 Ω □$^{-1}$ and an otherwise identical film annealed for 24 h in Ar at 300 °C with sheet resistance of 44 Ω □$^{-1}$. Lines are best fits to the data. Reproduced from ref. 7 with permission. Copyright 1980 The American Physical Society.

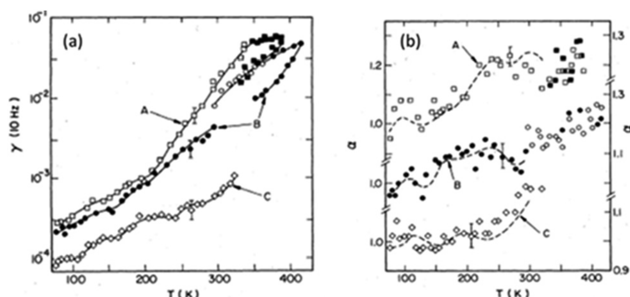


**Fig. 11** (a) $\gamma = \gamma_H \equiv S_V N f/V^2$ at $f$ = 10 Hz and (b) $\alpha = -\partial \ln S_V/\partial \ln f$ as functions of temperature and sequential annealing for sputtered AuPd NWs. (a) Open squares (curve A) show the noise of an as-processed sample with resistivity $\rho$(295 K) = 180 ± 20 μΩ cm. Solid squares show noise measurements while the sample is annealing *in situ*. Open and solid circles [curve B, $\rho$(295 K) = 145 ± 16 μΩ cm] show the noise during the second series of measurements. Diamonds [curve C, $\rho$(295 K) = 124 ± 14 μΩ cm] show the noise after the sample was heated to $T$ = 473 K in an oven outside the cryostat assembly for about an hour. (b) Dashed curves are predictions of Dutta–Horn model, eqn (5) of the text. Reproduced from ref. 52 with permission. Copyright 1985 The American Physical Society.

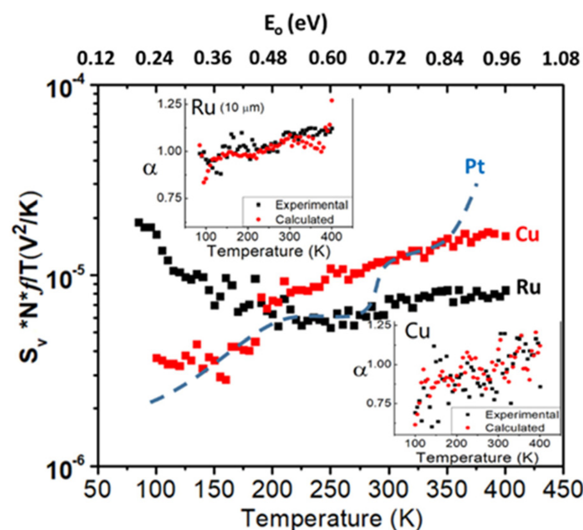


**Fig. 12** Temperature dependence of the normalized noise of a Pt NW (blue dashed curve) fabricated by substrate step lithography and Ru (black squares) and Cu (red squares) metal-line resistors fabricated at imec. Also shown are comparisons of values of the frequency dependence, $\alpha$, that were measured (black squares) or predicted by the Dutta–Horn model of $1/f$ noise (red circles) for Ru (upper inset) and Cu (lower inset), showing good agreement. Adapted from ref. 71 with permission. Copyright 2019 American Institute of Physics.

defect-energy distributions among metallic NWs.[51,71,96] The fully normalized noise of the sputtered Pt NW fabricated *via* substrate step lithography in the early 1980s increases monotonically with increasing temperature in Fig. 12, as does the normalized noise of the lithographically defined Cu metal line fabricated by imec in 2019.[71] Although the shapes of the curves vary, the normalized noise magnitudes differ by less than a factor of 2 over the full range of measurements. In con-

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trast to the results for Pt and Cu, the normalized noise of the lithographically defined Ru metal line is approximately constant above 200 K and increases monotonically with *decreasing* temperature below 200 K.[71] These results illustrate the kinds of variations that can be observed among the noise magnitudes and temperature dependences for metal lines and NWs due to differences in defect and/or impurity types, concentrations, and/or energy distributions.[52,55,66,71,73,95,96]

When NWs are cooled to low temperature, enhanced fluctuations can be observed. Fig. 13(a) shows resistance *vs.* temperature measurements from ~5 K to ~70 mK for a Bi NW fabricated *via* substrate step lithography.[53] An increase in resistance is observed with decreasing temperature due to localization and electron–electron interactions. As the temperature decreases, the spread in measurements increases. Fig. 13(b) shows that this resistance spread is due to random jumps in resistance that are similar to RTN in semiconductor devices (*e.g.*, Fig. 5).[53,54,56,62,90,106] Charge trapping does not occur in metallic NWs owing to the high density of free carriers in the conduction band, so fluctuations in scattering rates due to carrier-defect interactions are the most likely origin of the RTN. Similar resistance fluctuations are shown in Fig. 14(a) for a Bi film at 70 mK and in Fig. 14(b) for a Pt film at 250 mK.[54]

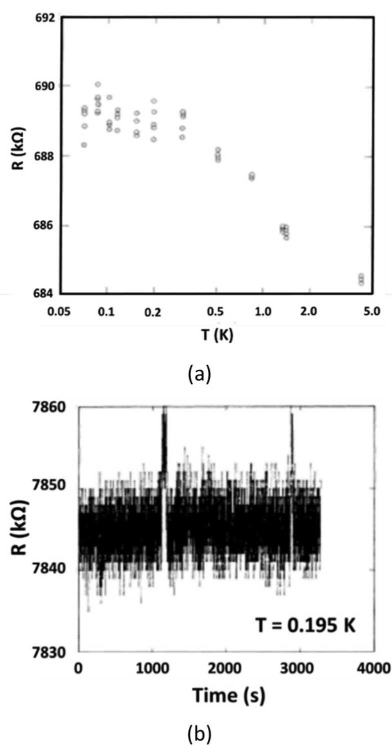


**Fig. 13** (a) Resistance *vs.* temperature for a Bi wire with $L$ = 60 μm and diameter $d$ = 46 nm fabricated *via* substrate step lithography. (b) Resistance at $T$ = 0.195 K as a function of time for a Bi film with $L$ = 16 μm, width $W$ = 8 μm, and thickness $t$ = 7 nm, fabricated in the same batch as the wires of (a). The rapid fluctuations with an envelope of about ±10 Ω are due to system noise. Large switching events at times of ~1200 s and ~2900 s are characteristic of RTN. Adapted from ref. 53 with permission. Copyright 1987 The American Physical Society.

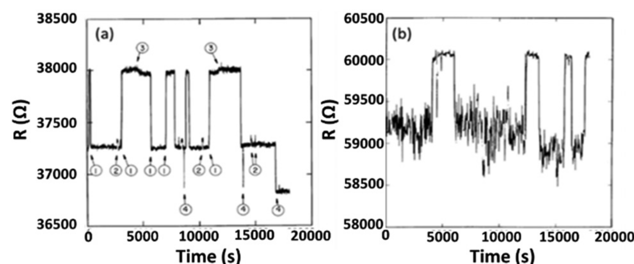


**Fig. 14** (a) Resistance *vs.* time at $T$ = 70 mK for an ~8 nm thick Bi film with $L$ = 10 μm and $W$ = 4 μm. Numbers denote different fluctuators. (b) Resistance *vs.* time at 250 mK for a 1 nm thick Pt film with $L$ = 7 μm and $W$ = 5 μm. Adapted from ref. 54 with permission. Copyright 1987 Institute of Physics.

In 1987 Beutler, Meisenheimer, and Giordano compared the fluctuations in Fig. 13 and 14 with those predicted by the theory of universal conductance fluctuations (UCF) by Feng, Lee, and Stone.[15,53,54,85] UCF theory predicts that the motion of one strong scattering center leads to conductance fluctuations of order $q^2/h$, where $h$ is Planck's constant.[15,85] They find that fluctuations in Fig. 13 and 14 are ~10× larger than predicted by UCF.

Also in 1987, following the approach of Martin, Pelz and Clarke showed that the fluctuating interference of electrons in the local environment of a moving defect or impurity ("local-interference") can lead to conductance fluctuations that are smaller than UCF predictions, and more consistent with the 1/*f* noise observed in metals.[86,180,181] In 1989 Birge *et al.* then measured low-temperature conductance fluctuations in thin Bi films that are much smaller than those in Fig. 13 and 14.[182] Fluctuation magnitudes in these films agree well with predictions of the local-interference model of Pelz and Clarke.[86,182] Taken together, it is likely that the "giant" conductivity fluctuations in Fig. 13 and 14 are most likely due to the stochastic motions and/or reconfiguration of larger defect and/or impurity complexes in the bulk of the Bi NWs and films.[15,53,54,85,86,108]

When a magnetic field is applied to a metal wire that exhibits UCF, the theory of Feng, Lee, and Stone predicts a 2× decrease in 1/*f* noise magnitude from the zero-field value.[15,18,183] This 2× reduction is due to a corresponding decrease in noise-producing transmission channels caused by magnetization-induced dephasing.[15,85,183–186] Spin-orbit coupling is a key consideration in both electron localization and UCF.[3,15,85,183–186] Clear evidence of time-dependent UCF (TDUCF) is shown in Fig. 15(a) for Li, Fig. 15(b) for Ag, and Fig. 15(c) for AuPd NWs, which vary from low to high spin–orbit coupling.[184–186] In all three cases in Fig. 15, TDUCF is observed at temperatures low enough to suppress scattering due to local interference and/or magnetic impurities (if present). At higher temperatures, a mixture of noise due to TDUCF, local interference, and/or magnetic impurities is found, leading to increases in relative noise magnitudes. These results confirm the significance of TDUCF in nanowires with lower (Li) or higher (Ag and AuPd) spin–orbit coupling.[184–186]

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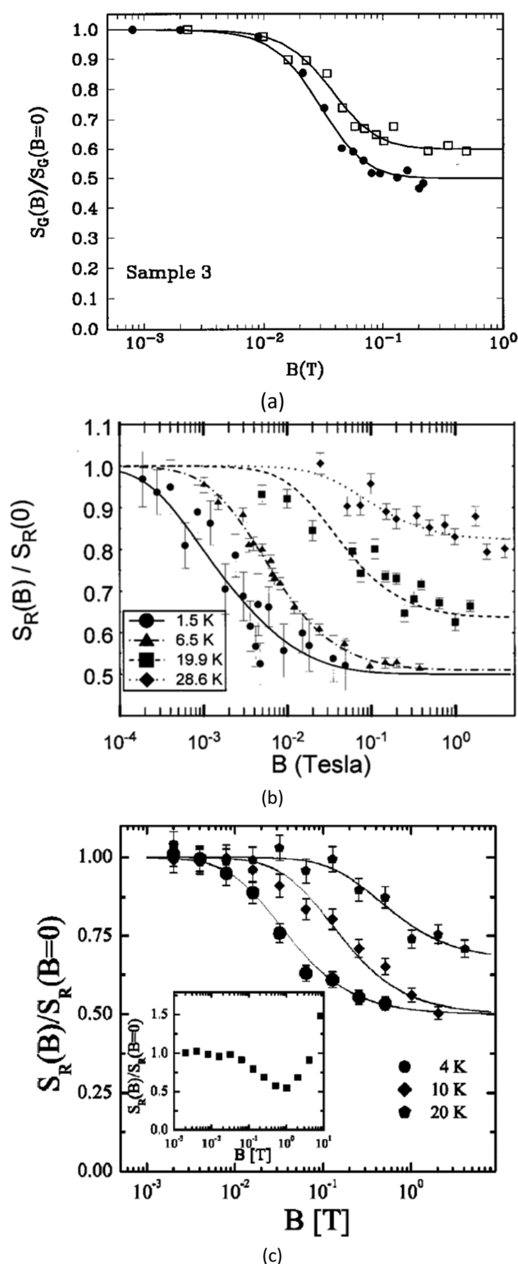


**Fig. 15** Ratios of 1/*f* noise magnitudes with, $S_R$(B), and without, $S_R$(0), magnetic fields applied to (a) Li (reproduced from ref. 184 with permission; copyright 1997 The American Physical Society), (b) Ag (reproduced from ref. 185 with permission; copyright 1999 The American Physical Society), and (c) AuPd NWs (reproduced from ref. 186 with permission; copyright 2004 The American Physical Society). The 2× reduction in $S_R(B)/S_R(0)$ at low temperatures is due to universal conductance fluctuations. At higher temperatures, fluctuations due to local interference increase values of $S_R(B)/S_R(0)$. The upturn in $S_R(B)/S_R(0)$ in the inset of (c) is due to process-introduced magnetic impurities.

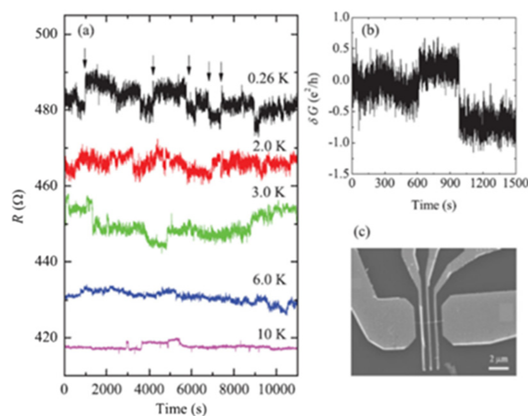


**Fig. 16** (a) Resistance at five temperatures for a $RuO_2$ NW with length $L$ = 1.5 μm and diameter $d$ = 67 nm. Data at 6.0 K, 3.0 K, 2.0 K, and 0.26 K are offset by 10 Ω, 20 Ω, 30 Ω, and 40 Ω, respectively, for clarity. (b) Conductance variation $\delta G = G - \langle G \rangle$ *vs.* time at 0.26 K. (c) Scanning electron microscope (SEM) image of lithographically defined NW. Reproduced from ref. 65 with permission. Copyright 2011 American Institute of Physics.

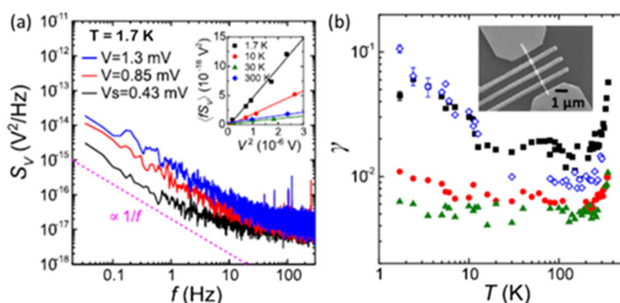


**Fig. 17** (a) $S_V$ *vs.* *f* and *T* for an $IrO_2$ NW with $L$ = 0.9 μm and $d$ = 147 nm; $\langle fS_V \rangle$ *vs.* $V^2$ is shown in the inset. (b) $\gamma = S_V N_c f/V^2$ *vs.* *T* for $IrO_2$ NWs from 1.7 K to 350 K. The inset is a SEM image of a NW. Dimensions are $L$ = 1.9 μm, $d$ = 143 nm (solid black squares); $L$ = 1.0 μm, $d$ = 123 nm (solid red circles); $L$ = 0.75 μm, $d$ = 125 nm (solid green triangles); and $L$ = 0.9 μm, $d$ = 147 nm (open blue diamonds). Reproduced from ref. 75 with permission. Copyright 2023 American Institute of Physics.

While defects and impurities are critical to the LF noise and RTN of metallic NWs, it is usually not possible to identify their microstructures.[55,66,86,95] As an exception, mobile hydrogen has been identified as a scattering impurity in Pd films by Zimmerman and Webb.[98] Also, Fig. 16 and 17 show conductivity fluctuations and LF noise in lithographically defined $RuO_2$ and $IrO_2$ NWs, respectively. In each case, the LF noise and RTN are attributed to TDUCF caused by mobile defects and/or impurities in the NWs, with oxygen vacancies a likely source in each case.[65,75] The normalized noise magnitudes for the $IrO_2$ NWs in Fig. 17 are 1–2 orders of magnitude higher than those of the Pt, Ru, and Cu NWs in Fig. 1, 3, 9, and 12. This suggests a higher defect density, mobility, and/or scattering cross-section for the $IrO_2$ NWs in Fig. 17 than for Pt, Ru, and Cu NWs.

As illustrated in Fig. 18, significant RTN can also be found in metallic nanobridges, which are essentially short, tapered NWs.[57,58,87,89] The conductivity fluctuations are dominated by the restriction at the base of the lithographically defined nanobridge in Fig. 18(a). Ralls *et al.* verified the crystallinity of these Cu nanobridges,[57] but still find significant RTN at room

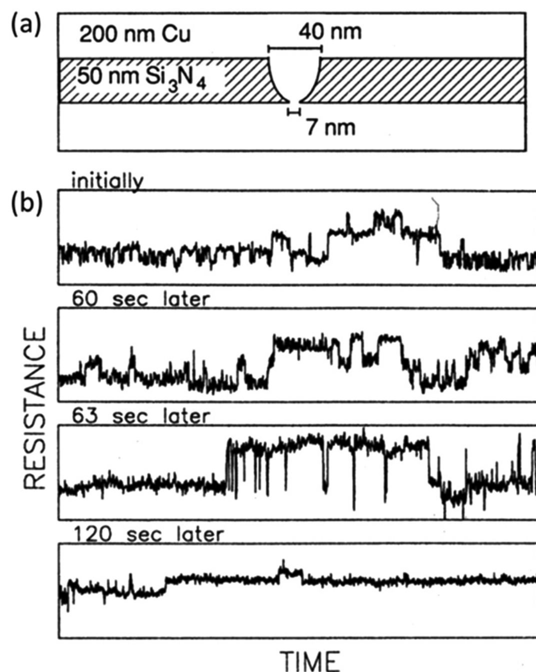


Fig. 18 (a) Schematic diagram of Cu nanobridge and (b) resistance *vs.* time snapshots (0.2 s each) at 300 K, illustrating the time evolution of defect-induced scattering in these structures at room temperature. Reproduced from ref. 57 with permission. Copyright 1989 The American Physical Society.

temperature, as shown in Fig. 18(b). These results demonstrate that, even in the absence of grain boundaries, large conductivity fluctuations can be found in metallic NWs and other nanoscale structures.[57,58,87,89] Ralls and Buhrman discuss the resulting fluctuations in terms of a "defect glass," in which the two-level fluctuations observed in Fig. 18(b) result from slow, stochastic transitions of the system from one configurational state to another.[58] These results show that, while defects and impurities can enhance 1/*f* noise and RTN in metallic NWs, significant noise due to fluctuations in scattering rates can occur even in clean, highly ordered nano-systems at room temperature.[57,58] The universality of these scattering processes helps explain why LF noise is observed in so many different types of materials and devices.[55,57,58,66,95]

## IV. Semiconducting nanowires

Ralls, *et al.*, showed in 1984 that MOS transistors at the ∼1 μm scale exhibit RTN at cryogenic temperatures due to the alternating capture and emission of electrons at a single, prominent oxide trap. Heating the device and decreasing the gate voltage closer to $V_{th}$ increased the number of active defects, leading to 1/*f* noise.[84] Kirton and Uren provide a thorough review of the intense activity that followed this initial report in the late 1980s.[56] It is therefore no surprise that, with continuing Moore's Law scaling of MOS structures, semiconducting NWs with much smaller dimensions exhibit LF noise and RTN in proportions that vary with device geometry, channel and insulator materials, defect concentrations, bias, temperature, *etc.*[59–74]

Fig. 19 shows LF noise measurements for a GaAs NW with AlGaAs insulating layer and PtPd Schottky wrap gate.[64] For many of the NWs, LF noise spectra are similar to the red curve for the *L* = 60 nm device in Fig. 19(a). An inverse-area dependence is observed for the noise magnitude, consistent with number-fluctuation noise *via* eqn (15).[64] This result shows that contact noise is not significant in these devices.[60,64,187,188] In some cases, *e.g.*, the blue and green curves for larger devices in Fig. 19(a), generation–recombination (G–R) noise is observed. The G–R noise correlates with gate leakage, suggesting that individual defects in AlGaAs are contributing Lorentzian noise at frequencies above 100–300 Hz.[64] A likely candidate for the responsible defect is the DX center, a well-known electron trap in AlGaAs, which is most often an isolated Si donor.[64,189–191]

RTN and LF noise are observed in InGaAs NW MOSFETs with gate dielectrics of 0.5 nm $Al_2O_3$/4.0 nm $LaAlO_3$ in Fig. 20(a) and (b) and with a 3.5 nm $Al_2O_3$ gate oxide in Fig. 20(c).[67] The RTN in Fig. 20(a) and the higher-noise device in Fig. 20(c) are attributed to number fluctuations due to discrete charge trapping in the gate oxide; the 1/*f* noise in the lower-noise device in Fig. 20(c) is attributed to mobility fluctuations.[67] The device is operating in the subthreshold regime of device operation in Fig. 20(a), in which small perturbations in surface potential due to charge capture and emission can lead

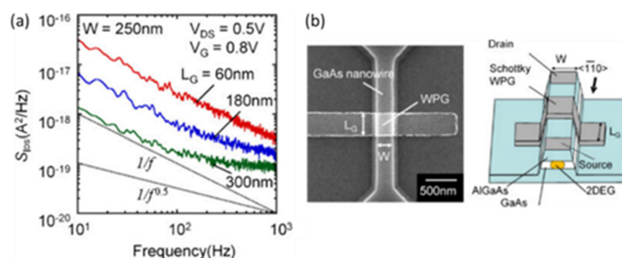


Fig. 19 (a) Current noise power-spectral densities of Schottky wrap-gate (WPG) GaAs/AlGaAs NW transistors with *W* = 250 nm and varying *L*. (b) Top view and schematic cross-section. Adapted from ref. 64 with permission. Copyright 2011 Institute of Physics.

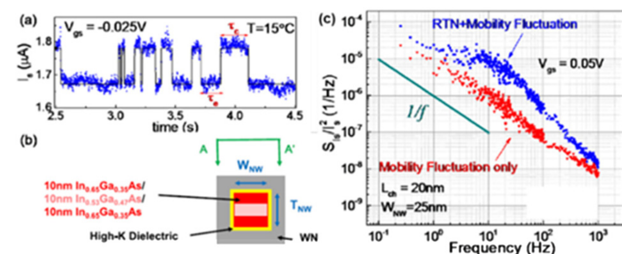


Fig. 20 (a) RTN at $V_{DS}$ = 50 mV for InGaAs NW MOSFET with geometry illustrated schematically in (b). The gate dielectric of the device in (a) is 0.5 nm $Al_2O_3$/4 nm $LaAlO_3$. (c) Normalized noise power spectral density *vs.* frequency for two InGaAs NW MOSFETs with 3.5 nm $Al_2O_3$ dielectrics: one showing RTN and the other showing LF noise. Adapted from ref. 67 with permission. Copyright 2015 Institute of Electrical and Electronics Engineers.

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to significant changes in current. About a 7% change in current is observed for each discrete trapping or emission event in Fig. 20(a). The mobility-fluctuation noise of the devices of Fig. 20 is analyzed by the authors within the framework of the Hooge mobility fluctuation model.[67] However, as noted in Section II, the Hooge model does not correctly characterize or parameterize the noise of semiconductor devices.[55,66,76,95,128,132,192] It is therefore more likely that the noise of these NWs is due to a mixture of number fluctuations (eqn (8)–(16))[73,108,112] and mobility fluctuations due to carrier scattering by defects and/or impurity atoms within NW channels, *e.g.*, as described by the local interference model of Pelz and Clarke.[86,180,181]

The Hooge mobility model is similarly used to interpret the LF noise observed in the Si NW MOSFETs of Fig. 21, primarily because the gate-voltage dependence of the noise follows eqn (2) instead of eqn (15) in the subthreshold region of device operation in Fig. 20(a).[63] As noted above, deviations from an inverse $(V_{GS} - V_{TH})^2$ dependence can occur for a several reasons in MOS devices, *e.g.*, strongly varying spatial or energy distributions of defects, as often found.[66,73,90,107,117–124,128,154,192] Noise *vs.* temperature measurements usually are required to determine if this is the case.[55,66,73,90,95] In the absence of such variation in defect spatial or energy distribution, carrier scattering by defects and/or impurity atoms within the NW channels is the most likely origin for the "excess" LF noise above that expected from number fluctuations in the subthreshold region of device operation in Fig. 21(a).[55,66,86,95,180,181]

Fig. 22 shows RTN for a vertical InAs/InGaAsSb/GaSb NW tunnel FET with a 20 nm InAs channel diameter[69] and $Al_2O_3$/$HfO_2$ gate dielectric, and Fig. 23 shows RTN for a silicon NW on a silicon-on-insulator (SOI) wafer with a $SiO_2$ gate dielectric.[59] The "giant" RTN observed in each case is far too large to be caused by simple charge exchange between the NW channel and traps in the gate dielectric.[59,69,76] Moreover, the scattering effectiveness of charged border traps decreases strongly with

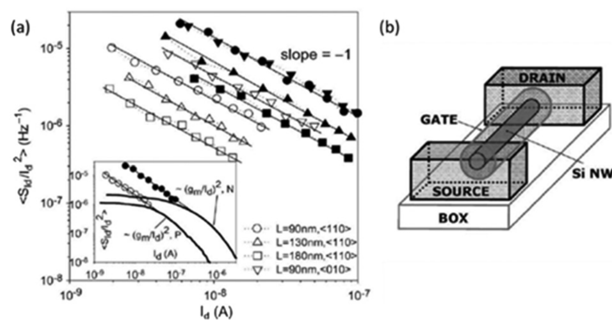


Fig. 21 (a) Average normalized drain–current spectral density at $|V_{DS}|$ = 50 mV and $f$ = 10 Hz *vs.* drain current $I_{DS}$ for *n*-type (solid symbols) and *p*-type (open symbols) Si NW transistors with $SiO_2$ gate dielectric thickness of 4 nm and effective radius of ~40 nm, as shown schematically in (b). The noise data of 90 nm n- and p-type SNWTs in the ⟨110⟩ direction are compared with lines of (constant × $(g_M/I_{DS})^2$) in the inset. Adapted from ref. 63 with permission. Copyright 2009 Institute of Electrical and Electronics Engineers.

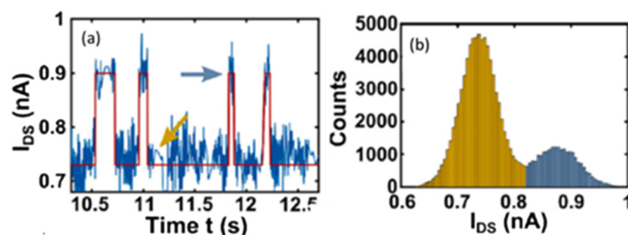


Fig. 22 (a) RTN at a temperature of 150 K in a vertical InAs/InGaAsSb/GaSb NW tunnel FET with a 20 nm InAs channel diameter and $Al_2O_3$/$HfO_2$ gate dielectric with effective oxide thickness of 1.4 nm. (b) Histograms of current values measured in the higher conductivity (gold) and lower conductivity (blue) states of the device, corresponding to the respective arrows in (a). Adapted from ref. 69 with permission. Copyright 2017 American Chemical Society.

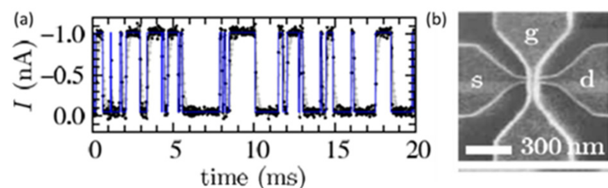


Fig. 23 (a) RTN for a silicon NW on a silicon-on-insulator (SOI) wafer with length of 200 nm and width of 30 nm with $SiO_2$ gate oxide thickness of 24 nm. $V_{GS}$ = 0.5 V, $V_{DS}$ = −6 mV. (b) Top view of NW. Adapted from ref. 59 with permission. Copyright 2006 Springer.

distance between the channel and the trap.[59,69,76,138] Thus, fluctuations in scattering rates caused by random dopant atoms in the NW channel and/or changes in charge state or configuration of bulk defect clusters in the NW channel are much more likely causes of the giant RTN observed in the NWs of Fig. 22 and 23.[59,69,76,139–144] The fluctuating activation and passivation of interface traps may also play a role in the LF noise of devices in Si MOS devices in which there are simultaneously high densities of dangling Si bonds and high concentrations of hydrogen at the $SiO_2$ interface.[76,132,193] This is an area of active current investigation.[76]

Nanosheets are essentially flattened and stacked versions of NWs being considered for next-generation Si MOS technologies.[72,81] The noise of gate-all-around devices with Si nanosheet channels and high-K gate dielectrics is shown in Fig. 24. LF noise due to number fluctuations is observed,[72] most likely because each measured device consists of 22 fins in parallel with two stacked nanosheets per fin. Hence, multiple defects and/or impurities are contributing to the noise. The normalized noise of the devices of Fig. 24 is comparable to or less than that of other advanced MOS technologies, indicating relatively low concentrations of border traps in the gate dielectrics and/or bulk defects in the nanosheets.[72,194–196] In studies by Hellenbrand, *et al.*, border traps also are found to be primarily responsible for the LF noise of III–V NWs, tunnel FETs, and planar MOSFETs.[197,198]

Fig. 25 summarizes results from detailed evaluations of RTN before total-ionizing-dose irradiation of gate-all-around

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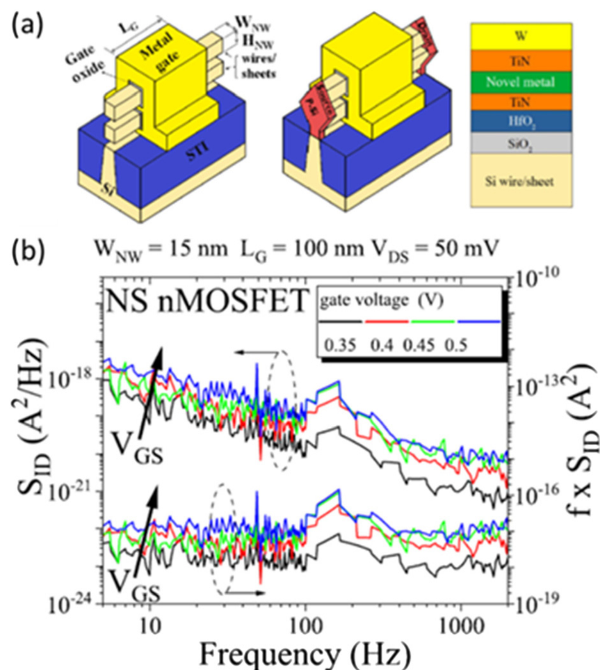


Fig. 24 (a) Schematic diagrams of gate-all-around GAA nFETs with two vertically stacked Si nanosheets. (b) Drain current noise power spectral density (left $y$-axis) and normalized power spectral density (right $y$-axis) as a function of frequency for a 15 nm nanosheet width device at different gate voltages. Adapted from ref. 72 with permission. Copyright 2020 Institute of Electrical and Electronics Engineers.

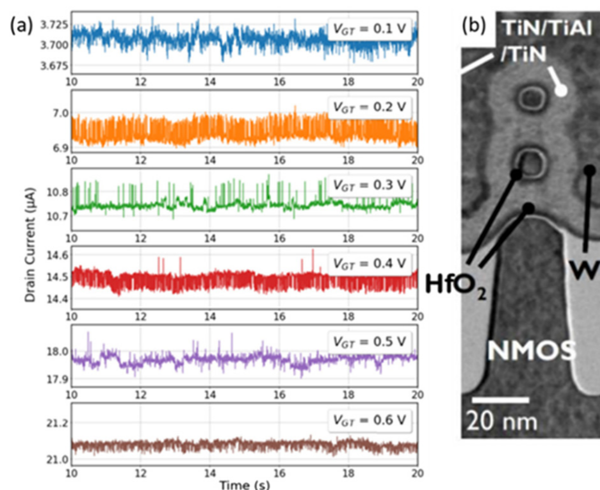


Fig. 25 Gate-to-threshold voltage dependence of $I_{DS}$ at 295 K for a GAA NW nFET with $L \approx 25$ nm, 8 nm diameter, and 1.8 nm $HfO_2$/1 nm gate dielectric; a transmission-electron-microscope image of the structure is shown in (b). $V_{DS}$ = 50 mV; $V_{GT} \equiv V_{GS} - V_{TH}$. Note that each value of $V_{GT}$ has a different $y$-axis scale. Adapted from ref. 74 with permission. Copyright 2021 Institute of Electrical and Electronics Engineers.

(GAA) Si MOS NW transistors with high-K dielectrics. Each device contains four fins and two NWs.[74] As the gate voltage and/or device temperature is varied, LF noise with or without RTN is observed, depending on the gate voltage. Fig. 25 shows significant RTN at room temperature, especially for $V_{GT} \equiv V_{GS} - V_{TH}$ at 0.2 V and 0.3 V. Primarily $1/f$ noise is observed for $V_{GT}$ = 0.1 V and $V_{GT}$ = 0.6 V. Using a hidden Markov model and measured ratios of capture and emission times, it is inferred that only a few prominent defects lead to the observed RTN in Fig. 25.[74,199–201] Under the conventional assumption that these RTN are due to charge exchange with border traps in a standard number fluctuation model, estimates of trap locations were inferred, with defects identified in both the near-interfacial $SiO_2$ and the $HfO_2$ layer of the dielectric stack.[74] However, in at least some cases, this typical interpretation[74,199–201] may not be complete or correct,[76,77] as we now discuss.

Table 1 summarizes predicted and observed RTN magnitudes for the data of Fig. 25; predictions use the simple number fluctuation model of eqn (12) without mobility fluctuations.[76,110,111] At $V_{GT}$ = 0.2–0.3 V, where RTN are most active, Table 1 shows that ratios of observed magnitudes of current fluctuations are up to ∼2.5× larger than expectations based on the number fluctuation model of eqn (12). This demonstrates the importance of mobility fluctuations in the RTN of these devices.[76,77,110,111] At these voltages, the strength of scattering needed to account for the RTN magnitudes is much greater than likely from remote Coulomb scattering from border traps.[59,69,76,77,138]

These results suggest that the RTN of the Si NW MOSFETs of Fig. 25 are caused by a mixture of border traps in the high-K dielectric, bulk defects in the NW channels, and interface traps.[74,76,77] The responsible bulk defects may be random dopant atoms and/or defect clusters.[74,76,77,139–144] For interface traps to contribute to LF noise and/or RTN, the rate-limiting step is more likely to be hydrogen-mediated defect activation and passivation, which can occur on ms to s time scales, than charge capture and emission, which typically occur on μs time scales for interface traps.[76]

Fig. 26 and 27 show the evolution of the LF noise *vs.* frequency and temperature for as-processed and irradiated devices. Consistent with the results in Fig. 25, spectral slopes range from $\sim 1/f$ (no RTN) to $\sim 1/f^2$ (significant RTN).[74] Inferred defect-energy distributions from the Dutta–Horn model of LF noise[66,95] are shown in Fig. 26(b) and 27(b). Some active defects in as-processed devices are passivated during irradiation, some defects are newly activated *via* irradiation, and other defects are remarkably stable through the full irradiation and measurement sequence.[74,77]

Table 1 Predicted and Observed Current Fluctuation Magnitudes for the Silicon NWs of Fig. 25. Data are from Gorchichko, *et al.*[74] Predictions are from the Number Fluctuation Model (NMF) using eqn (12) of the text

| $n_c$ ($10^{12}$ cm$^{-2}$) | $V_{GT}$ (V) | $1/N_C$ ($10^{-3}$) NMF prediction | $\Delta I_{DS}/I_{DS}$ ($10^{-3}$) measured | $\frac{(\Delta I_{DS}/I_{DS})}{1/N_C}$ |
|---|---|---|---|---|
| 2.2 ± 0.1 | 0.10 | 9.0 ± 0.5 | 8.0 ± 1.0 | 0.90 ± 0.15 |
| 4.3 ± 0.2 | 0.20 | 4.5 ± 0.25 | 8.5 ± 1.0 | 1.9 ± 0.3 |
| 6.5 ± 0.4 | 0.30 | 3.0 ± 0.2 | 7.5 ± 1.0 | 2.5 ± 0.3 |
| 8.6 ± 0.4 | 0.40 | 2.3 ± 0.1 | 2.8 ± 0.3 | 1.2 ± 0.2 |
| 11 ± 0.5 | 0.50 | 1.8 ± 0.1 | 2.8 ± 0.3 | 1.6 ± 0.3 |
| 13 ± 0.5 | 0.60 | 1.5 ± 0.1 | 1.9 ± 0.3 | 1.25 ± 0.25 |

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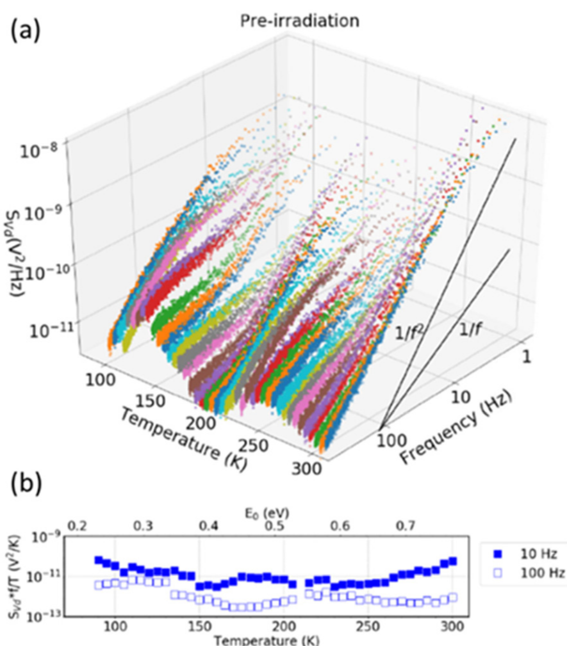


Fig. 26 (a) Frequency and temperature dependences of $S_{V_d}$ at $f$ = 1–400 Hz and $T$ = 90–300 K and (b) temperature dependence of the normalized noise at $f$ = 10 and 100 Hz for the as-processed GAA NW nFETs of Fig. 25. Noise measurements were performed at $V_{GT}$ = 0.4 V and $V_d$ = 50 mV. When significant RTN is observed, the normalized noise at 10 Hz significantly exceeds that at 100 Hz. Adapted from ref. 74 with permission. Copyright 2021 Institute of Electrical and Electronics Engineers.

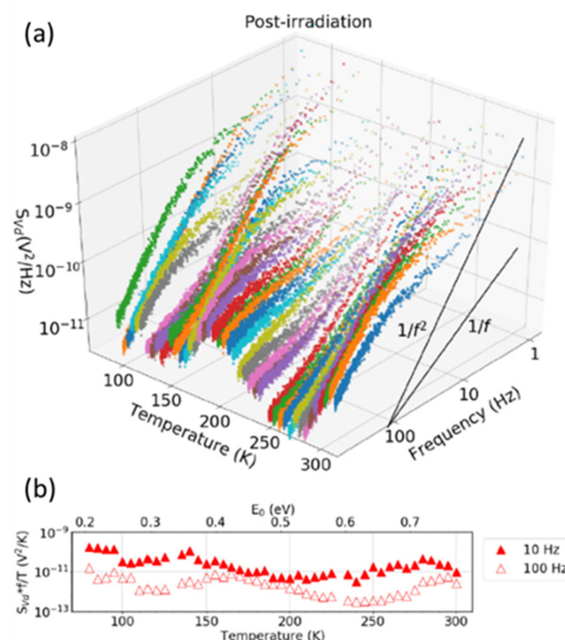


Fig. 27 (a) Frequency and temperature dependences of $S_{V_d}$ at $f$ = 1–400 Hz and $T$ = 90–300 K and (b) temperature dependence of normalized $S_{V_d}$ at $f$ = 10 and 100 Hz for GAA NW nFETs of Fig. 25 and 26 irradiated to 2 Mrad($SiO_2$) and annealed for 1 h at $V_{GS}$ = 0.5 V. Noise measurements were performed at $V_{GT}$ = 0.4 V and $V_d$ = 50 mV. When significant RTN is observed, the normalized noise at 10 Hz significantly exceeds that at 100 Hz. Adapted from ref. 74 with permission. Copyright 2021 Institute of Electrical and Electronics Engineers.

That border traps primarily lead to 1/*f* noise and bulk defects evidently lead to large RTN in the Si MOS NWs of Fig. 25–27 is the reverse of the trend inferred for early-generation InGaAs NWs in Fig. 20. There RTN was attributed to border traps and LF noise was attributed to fluctuations in carrier scattering rates due to bulk defects.[67] This trend reversal may result from improvements in NW fabrication over the last ~10 years.

Finally, Fig. 28 shows that, when the NWs of Fig. 25–27 are operated under conditions for which large RTN is *not* observed, the slope of the gate-voltage dependence, $\beta = -\frac{\partial \ln S_{V_d}}{\partial \ln V_{GT}}$, is generally close to 2, as expected from eqn (15) for noise caused primarily by border traps with approximately uniform energy and spatial distributions.[55,66,95] Hence, neither quantum confinement, series resistance, nor trap-trap interaction effects appear to be significantly affecting the LF noise of these NWs.[202,203] Instead, the results of Fig. 26 and 27 are consistent with previous studies on planar MOSFETs and FinFETs with $SiO_2$ and/or high-K gate dielectrics (*e.g.*, Fig. 7 and 8) for which O vacancies and complexes with hydrogen most likely lead to the observed 1/*f* noise.[66,73,74,90,107,109,112–114,120–123,131–134,145–147,204–210]

The wide range of noise magnitudes and frequency dependences observed in Fig. 25–28 strongly suggest that the noise of analog ICs built using semiconducting NWs may be quite challenging to model with confidence as a function of operating voltage and temperature.[211–217] Until these issues are resolved, users will have difficulty in assessing and assuring the accuracy and precision of systems relying on NWs or similarly scaled MOS devices.[81] These manufacturability and reliability issues must be addressed before high-volume application of NW-based ICs is possible in critical commercial, defense, space, and scientific applications.[214–217]

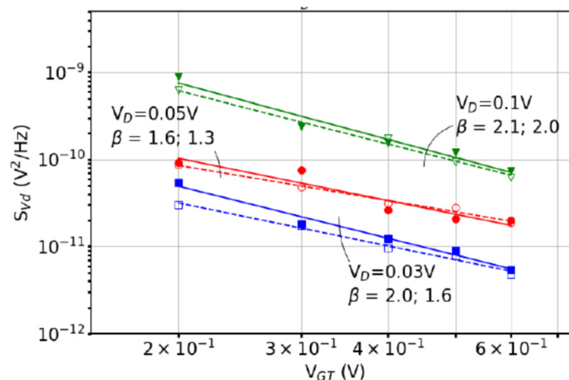


Fig. 28 Gate-voltage dependence of $S_{V_d}$ at $V_{DS}$ = 30 mV, 50 mV, and 100 mV for as-processed (closed symbols, solid lines) and irradiated (open symbols, dashed lines) GAA NW *n*FETs. The device was irradiated to 1 Mrad($SiO_2$) with 10 keV X-rays at $V_{GS}$ = 0.5 V. Reproduced from ref. 74 with permission. Copyright 2021 Institute of Electrical and Electronics Engineers.

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## V. Conclusions

Defects and impurities play critical roles in the LF noise of metallic and semiconducting NWs. Effective defect-energy distributions can be obtained from noise *versus* temperature measurements in conjunction with the Dutta–Horn model of $1/f$ noise. For metallic NWs, fluctuations in scattering rates caused by defect and/or impurity motion and/or reconfiguration of a bulk defect complex are often the dominant sources of LF noise and RTN. With few exceptions, the nature of these defects and impurities are unknown.

The capture and emission of carriers by border traps in adjacent or surrounding dielectrics often dominate LF noise and RTN for NWs in MOSFET configurations. Comparative studies of device performance, reliability, and radiation response, often supported by first principles calculations, enable identification of border traps leading to LF noise in semiconductor NWs and other MOS devices passivated with $SiO_2$ and/or high-K dielectric layers. In particular, oxygen vacancies and/or their complexes with hydrogen can lead to LF noise and/or RTN. Defect-passivation treatments such as high-pressure annealing in hydrogen or deuterium have been effective in reducing LF noise and RTN in semiconductor devices. Bulk defects and/or impurities also can contribute significantly to the LF noise, RTN, and device-to-device variations of semiconducting NWs. Reducing defect densities and variability in response are therefore crucial steps to enable high-volume manufacturing of ICs relying on NWs for critical terrestrial and space applications.

## Conflicts of interest

There are no conflicts to declare.

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