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REVIEW ARTICLE

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Charge traps revisited: from unwanted defects to functional synapses in photosynaptic devices

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Charge trap sites have often been considered defects that induce bias stress, reduce stability, and compromise device reliability. In an out-of-the-box perspective, recent work shows that these sites can also act as useful elements that store charge, tune responses, and mimic biological learning. While past research focused on suppressing or eliminating traps, a growing body of studies now takes the opposite view and explores their deliberate use for synaptic functions. This new direction shifts charge traps from unwanted sites to functional components in memory, synaptic, and optoelectronic devices. Studies now demonstrate trap-based weight storage, light-driven plasticity, and hybrid electro-photonic learning. This review summarizes progress in using interface traps for adaptive and multifunctional electronics. We compare device designs that exploit trap dynamics and highlight their impact on neuromorphic and optoelectronic systems. Key challenges include reproducibility, stability, and integration at large scale. This review offers a timely perspective on exploiting charge traps, with an emphasis on their emerging roles in next-generation neuromorphic and optoelectronic technologies.

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Introduction

Since the early development of semiconductor devices, charge traps have been primarily viewed as parasitic defects that limit charge transport performance and operational stability.^{1,2} Trapping and de-trapping of charge carriers have been widely

associated with threshold voltage shifts, hysteresis, bias stress effects, and long-term reliability degradation in a broad range of electronic^{3,4} and optoelectronic devices.^{5,6} Accordingly, extensive efforts have been devoted to suppressing or eliminating charge traps through annealing,^{7–12} defect passivation,^{13–20} interface engineering,^{21–28} and dielectric optimization.^{29–36} In



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metal-oxide-semiconductor field-effect transistors,^{37–39} thin-film transistors,^{40–46} and photodetectors alike,^{47–52} reducing trap density has been regarded as a prerequisite for achieving high mobility,^{53–58} fast response,^{59–63} and stable operation.^{64–68} As a result, charge traps have long been treated as obstacles to be minimized rather than as elements with potential functional value.

In parallel with these traditional efforts to suppress defects, neuromorphic electronics has recently emerged as a promising study for overcoming the fundamental limitations of conventional von Neumann computing.^{69,70} In conventional von Neumann systems, memory and computation units are physically separated, requiring repeated data transfer between the processor and memory during operation. Such architectural separation has become a major source of inefficiency in modern information processing, especially in terms of energy consumption and latency. Neuromorphic systems aim to address this limitation by integrating sensing, storage, and computation, enabling adaptive and energy-efficient operation.⁷¹ Inspired by biological neural systems, neuromorphic devices aim to emulate key brain functions such as learning, adaptation, and energy-efficient information processing, leading to rapidly growing interest and intensive research efforts across materials,^{72–76} devices,^{77–79} and system architectures.^{80–84} A central requirement for neuromorphic hardware is the ability to achieve gradual, analog, and history-dependent modulation of conductance, which serves as the physical basis for synaptic weight storage and learning.^{85,86} Different from digital memory elements that rely on abrupt switching, synaptic devices demand continuous and multilevel memory operation with tunable retention times.^{87–89} From this perspective, charge trapping phenomena, including incremental charge accumulation and time-dependent release, naturally provide the physical mechanisms required to realize such analog synapse memory behaviors.^{90–92}

In photosynaptic devices, the interaction between photogenerated carriers and localized electronic states is a crucial factor in governing synaptic behavior. Charge traps, which capture and gradually release photogenerated carriers, directly give rise to key synaptic characteristics such as persistent photoconductivity^{93–95} and tunable memory retention.^{96–98} Importantly, these trap-mediated dynamics closely resemble biological synaptic processes, where learning and forgetting are governed by the accumulation and decay of internal states rather than abrupt switching events. As a result, phenomena that were once considered detrimental, including carrier trapping, delayed recombination, and hysteresis, can be reinterpreted as essential physical mechanisms for implementing light-driven synaptic plasticity. Here, we revisit charge traps as functional building blocks for optoelectronic synapses, rather than as defects to be suppressed, and systematically categorize recent strategies that use trap-mediated charge dynamics for neuromorphic applications.

1. Principles of charge traps in photosynaptic devices

Charge traps are localized electronic states within the bandgap that can temporarily capture electrons or holes, thereby

influencing carrier transport and recombination dynamics.⁹⁹ Trap states are generally classified as shallow or deep trap depending on their depth relative to the band edges. Shallow traps, located closer to the band edges, release carriers more efficiently because of their smaller energy barrier for de-trapping and are therefore often associated with volatile conductance modulation. In contrast, deep traps can retain carriers for extended periods and are more closely related to persistent photoconductivity and non-volatile memory behavior. In semiconducting electronic materials, such trap states may arise from intrinsic defects,¹⁰⁰ impurities,¹⁰¹ grain boundaries,¹⁰² dielectric/semiconductor interfaces,¹⁰³ or heterojunction interface,¹⁰⁴ and have a significant influence on device operation.

In conventional electronic and optoelectronic devices, charge traps are typically regarded as undesirable because they can reduce carrier mobility,¹⁰⁵ induce threshold-voltage instability,¹⁰⁶ and degrade operating reproducibility.¹⁰⁷ Accordingly, extensive efforts have been devoted to suppressing trap states through defect passivation,¹⁰⁸ interface optimization,¹⁰³ impurity control,¹⁰¹ and thermal annealing.³⁸ These approaches aim to reduce trap density, thereby enabling more stable and predictable device operation.

In contrast, the trapping and de-trapping of photogenerated carriers constitute one of the key physical mechanisms underlying optical synaptic operation.¹⁰⁹ Upon optical excitation, photogenerated carriers in the active layer can be captured by defect states or interfacial trap sites, causing recombination delays. This process induces a photogating effect, in which trapped charges act as an additional local gate bias and modulate the channel conductivity.¹¹⁰ Therefore, the temporal characteristics of synaptic responses are closely governed by de-trapping dynamics. Fast de-trapping leads to transient conductance modulation similar to short-term plasticity (STP), whereas slower de-trapping from deeper trap states maintains the postsynaptic current after stimulus remove, thereby enabling long-term plasticity (LTP) and memory retention.

To provide a comprehensive roadmap for using charge trapping phenomena, Fig. 1 schematically illustrates the classification of recent optoelectronic synaptic devices based on two distinct axes: the wavelength region and the trap dynamics methodology. First, the wavelength region represents a input dimension that governs the generation of charge carriers. The most fundamental physical prerequisite for the operation of optoelectronic synaptic devices is that the incident photon energy should exceed the intrinsic bandgap of the channel or light-absorbing layers. Accordingly, this review classifies devices into the ultraviolet (UV), visible, and Infrared (IR) regimes to analyze the technological advancements within each spectral range. This spectral classification not only establishes criteria for selecting materials optimized for specific wavelength regions but also provides strategic insights into engineering trap sites to overcome wavelength-dependent challenges. Complementing the wavelength region, the dynamics methodology is categorized by the trap generation strategies into five distinct methods: (i) interface traps, (ii)



i) Synapses according to wavelength region

Ultra-violet detection Visible-light detection Infra-red detection

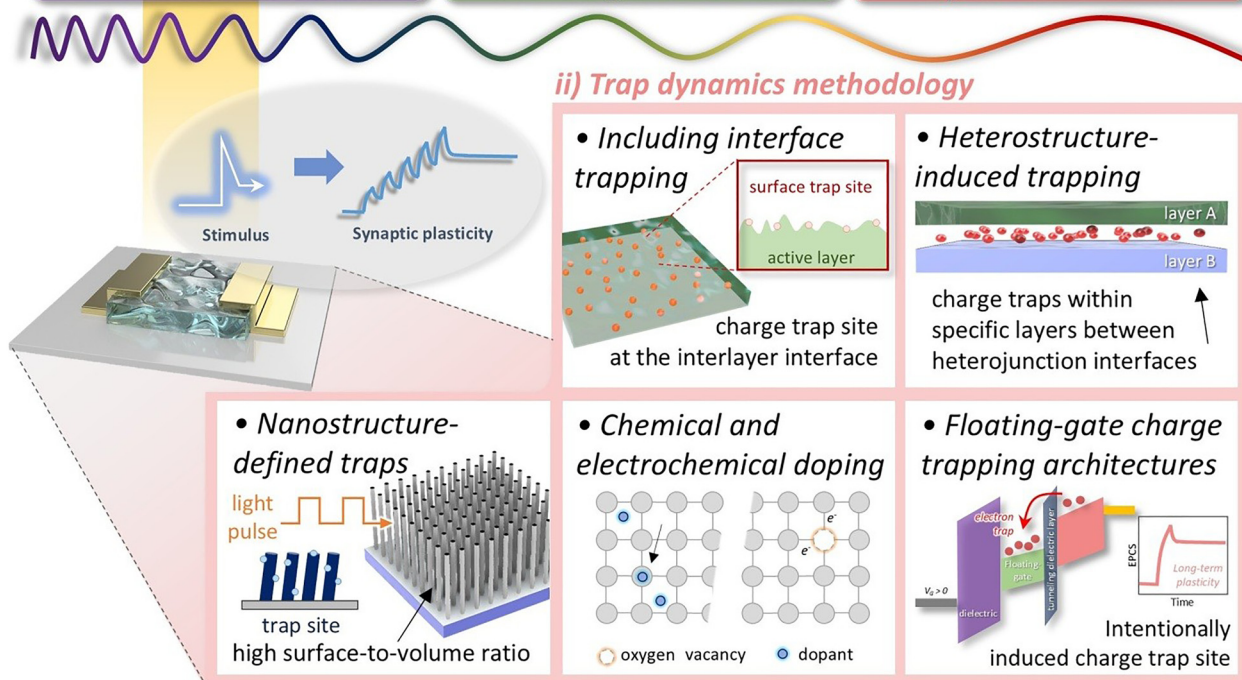


Fig. 1 Schematic illustration of the classification framework for optoelectronic synapses, organized along two orthogonal axes: (i) wavelength-dependent operation (UV, visible, and IR) and (ii) trap-engineering methodologies, including interface trapping, heterostructure-induced trapping, nanostructure-defined traps, chemical/electrochemical doping, and floating-gate architectures.

heterostructure-induced trapping, (iii) nanostructure-defined traps, (iv) chemical and electrochemical doping, and (v) floating-gate charge trapping architectures. This classification offers a better understanding of where the trap sites are located, whether at the dielectric interface, within the bulk film, or in isolated floating nodes, and how the trapping/de-trapping mechanism operates within the optoelectronic devices. By correlating these structural methodologies with their operational wavelengths, this review explains the diverse design rules for optimizing trap based neuromorphic systems.

2. Utilization of optoelectronic synapse devices depending on wavelength region

In this section, we examine efficient photodetection and synaptic emulation across the UV, visible, and IR spectra, covering strategies based on the intrinsic bandgap of the material in the device. Since the wavelength of incident light determines both photon energy¹¹¹ and optical penetration depth,¹¹² the generation and spatial distribution of photocarriers vary accordingly.¹¹³ This subsequently influences charge trapping and de-trapping dynamics, resulting in different synaptic behaviors such as plasticity, weight modulation, and retention.¹¹⁴ We categorize recent advances by target wavelength, highlighting how trap states are engineered to improve synaptic

properties, thereby optimizing responsivity, persistent photoconductivity, and energy efficiency within each spectral region.

2.1. UV light-induced optoelectronic synapses

Optoelectronic devices operating in the UV spectrum possess profound technological significance by extending visual perception beyond the biological limitations of human cone cells, which are restricted to detecting only visible light. This capability to perceive invisible wavelengths is critical for diverse environmental, industrial, and biological applications. UV optoelectronic synapses are becoming promising in advanced optical detection fields, including biometric recognition, fire monitoring, and information safety systems.^{49–51} However, the practical realization of these devices has traditionally been challenged by inherent performance trade-offs between dark current, synaptic plasticity, responsivity, and memory retention.^{115,116} To address these issues, recent research has focused on manipulating carrier dynamics through advanced material engineering strategies, ranging from elemental doping to the construction of heterostructures with intended charge trapping layers.

To achieve reduced dark current and developed synaptic behavior, Lee *et al.* proposed a photosynaptic device based on doping method.¹¹⁷ While undoped SnO₂ exhibits a strong persistent photoconductivity effect due to its intrinsic defects, it suffers high dark current. Zn doping can suppress dark current but degrade persistent photoconductivity effect and



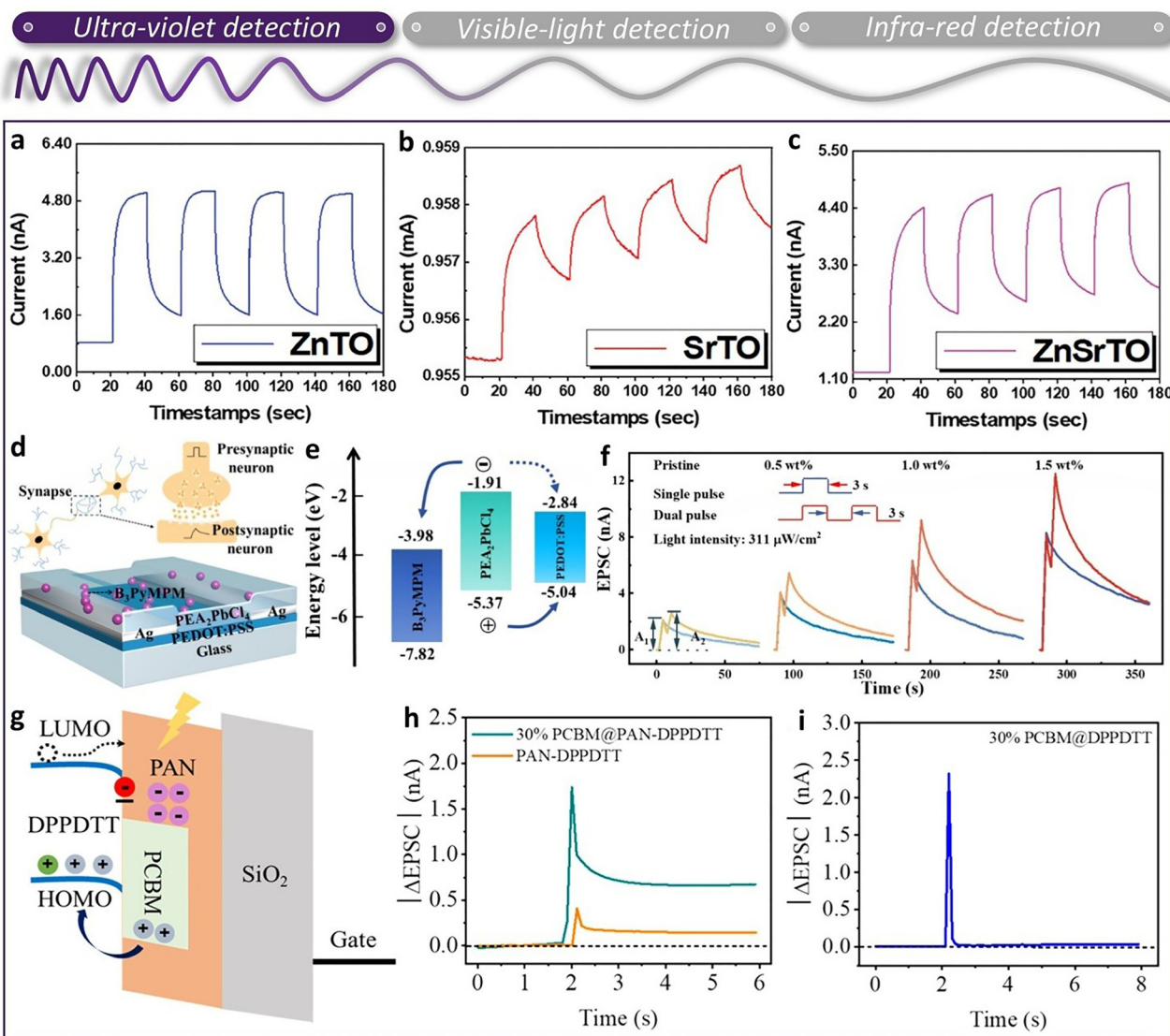


Fig. 2 (a) Current–time curve of Zn doped SnO₂ under DUV illumination. (b) Current–time curve of Sr doped SnO₂ under DUV illumination. (c) Current–time curve of both Zn and Sr doped SnO₂ under UV illumination. (a)–(c) Reproduced with permission.¹¹⁷ Copyright 2025 Wiley-VCH GmbH. (d) Device structure of DUV OSP. (e) Energy band diagram of deep-UV optoelectronic synapses inserting B₃PyMPM trapping layer under deep-UV illumination (f) EPSC–time curve based on different B₃PyMPM concentrations under deep-UV illumination. (d)–(f) Reproduced with permission.¹¹⁸ Copyright 2025 American Chemical Society. (g) Operation mechanism under UV illumination (h) EPSC–time curve comparison depending on the presence of PCBM layer under UV illumination (i) EPSC–time curve for PAN layer functionality under UV illumination. (g)–(i) Reproduced with permission.¹¹⁹ Copyright 2024 American Chemical Society.

synaptic behavior (Fig. 2a). To overcome this trade off problem, Sr doping is introduced to facilitate the formation of oxygen vacancies (Fig. 2b). SnO₂ doped with both Zn and Sr balances reduced dark current with enhanced persistent photoconductivity effect, realizing energy efficient photosynaptic devices (Fig. 2c).

Beyond modulating intrinsic defects *via* elemental doping, constructing heterostructures with incorporated trapping species offers an alternative strategy to manipulate carrier recombination and enhance synaptic plasticity. To enhance photocurrent and paired pulse facilitation (PPF) ratio, Xie *et al.* proposed an optoelectronic synaptic device inserting electron trapping layer within a heterostructure (Fig. 2d).¹¹⁸

The strategy involves incorporating B₃PyMPM into the perovskite layer to generate internal trap sites. Both B₃PyMPM and PEDOT:PSS hinder recombination of electron–hole pairs (EHPs), by separating electrons and holes, respectively (Fig. 2e), increasing the photocurrent. The synaptic plasticity is governed by the dopant concentration. Increasing the B₃PyMPM concentration augments the density of trap sites, thereby further inhibiting recombination and resulting in a significant increase in the photocurrent and PPF ratio (Fig. 2f).

Extending the charge trapping strategy to organic electronics, recent research has focused on integrating dedicated insulating trapping layers within p–n heterojunctions to simultaneously optimize spectral responsivity and memory



retention. To suppress carrier recombination and enhance the retention, Liang *et al.* proposed a p–n heterojunction optoelectronic synaptic transistor incorporating a charge trapping layer.¹¹⁹ The device utilizes a PCBM@PAN layer as an electron trapping layer, facilitating the spatial separation of photogenerated carriers (Fig. 2g). Comparative analysis reveals the distinct contributions of each component. [6,6]-Phenyl-C71-butyric acid methyl ester (PCBM) improves responsivity to UV light, thereby driving higher excitatory photo-synaptic current (EPSC) (Fig. 2h), whereas polymer polyacrylonitrile (PAN) functions as an electron trapping layer to suppress recombination and extending the retention time (Fig. 2i). The integrated PCBM@PAN-DPPDTT device demonstrates enhanced optoelectronic performance under UV illumination by combining the high responsivity of PCBM with the strong retention capability of PAN.

2.2. Visible light-induced optoelectronic synapses

Optoelectronic synaptic devices operating in the visible spectrum hold profound significance as the hardware foundation for artificial vision systems that emulate human perception. Different from UV or IR devices designed to extend capabilities beyond biological limits, visible light synapses aim to replicate the complicated processing functions of the human retina and visual cortex. Conventional image sensors merely capture optical intensity, creating a bottleneck where massive data processing is relegated to external processors. However, recent advancements demonstrate that synaptic devices can transcend passive sensing to perform sophisticated in-sensor computing.^{120–122} Such capabilities are critical for realizing intelligent neuromorphic vision systems that can efficiently process complex real word environments with human-like cognitive accuracy.

By engineering intrinsic defects within the channel layer, Chen *et al.* proposed an optical synaptic device featuring enhanced photoconductivity and non-volatile behavior.¹²³ The study demonstrates that increasing the *in situ* thermal treatment temperature leads to the enlargement of voids between nanoplates (Fig. 3a). These structural modifications facilitate the formation of defect sites that induce band bending, effectively functioning as a mechanism to separate the channel into a conductive active layer (surface) and a trap layer (interior). This potential gradient drives photogenerated electrons toward the surface while trapping holes within the interior defect states. Even after removing illumination, the potential barrier formed by defect states impedes carrier recombination, resulting in long-term potentiation behavior (Fig. 3b). This spatial separation effectively suppresses carrier recombination, thereby enabling the realization of robust non-volatile characteristics (Fig. 3c).

While creating robust memory *via* defect engineering is a significant step, reproducing complex biological functions like visual attention requires more than just optical retention. It demands the integration of electrical modulation to process signals dynamically. Visual perception tasks require synaptic devices capable of integrating multimodal plasticity. In this

context, Chen *et al.* reported a 2D integration of optoelectronic synapse devices operating in the visible region, which mimics the human visual attention mechanism.¹²⁴ The device operates through dual mechanisms depending on the type of stimulation pulse. Under optical pulse, intrinsic defects within the channel act as trap sites to induce persistent photoconductivity, enabling perceptual learning for the contrast enhancement of weak signals (Fig. 3d). Under an electrical pulse modulated by gate bias polarity, electrons tunnel between the channel and the floating-gate, thereby exhibiting inhibitory post synaptic current (IPSC) (Fig. 3e) and EPSC properties, respectively. This electrical plasticity allows the device to implement top-down attention modulation independent of optical stimuli. As a result, by utilizing optical long-term potentiation for saliency detection and electrical long-term depression for attention shift, the system successfully executes a sequential multi-target recognition strategy, overcoming the limitations of conventional sensing (Fig. 3f).

In addition to the modulation of attention mechanisms, the next frontier in neuromorphic vision is to selectively process diverse optical information such as color and polarization, which requires bidirectional photoresponses implemented in advanced heterostructures. Kim *et al.* proposed a heterostructure synaptic phototransistor that selectively implements positive photocurrent (PPC) and negative photoconductance (NPC), depending on the gate bias and incident light wavelength.¹²⁵ Under low gate voltage, the PPC effect is induced by the increased channel conductance, driven by the abundant electrons generated within the channel under blue light and the tunneling of electrons formed in the trap layer to the channel under red light (Fig. 3g). Conversely, under high gate voltage, the NPC effect is formed by the gate screening effect. Under blue light, electrons in the channel tunnel into the trap layer, while under red light, electrons are generated in the trap layer (Fig. 3h). This bidirectional photoresponse characteristic, which selectively controls potentiation and depression *via* two variables enables the realization of a high-level neuromorphic vision system capable of simultaneously recognizing and memorizing color and polarization information (Fig. 3i).

2.3. IR light-induced optoelectronic synapses

Optoelectronic synaptic devices operating in the IR spectrum are pivotal for expanding the frontiers of machine vision beyond human capabilities. Their ability to perform visual identification tasks in low wavelength light conditions and ensure accurate image transmission through obscurants like smoke and dust makes them indispensable for next-generation technologies, including autopilot systems, telecommunications, and light detection and ranging (LiDAR).^{126,127} Furthermore, implementing these capabilities within in-sensor and edge computing architectures enables the real-time processing of invisible information with high energy efficiency and low latency.^{128,129} To realize such robust all weather vision systems, recent research has focused on overcoming the material limitations of IR detection through advanced heterostructure engineering. These advancements collectively highlight the



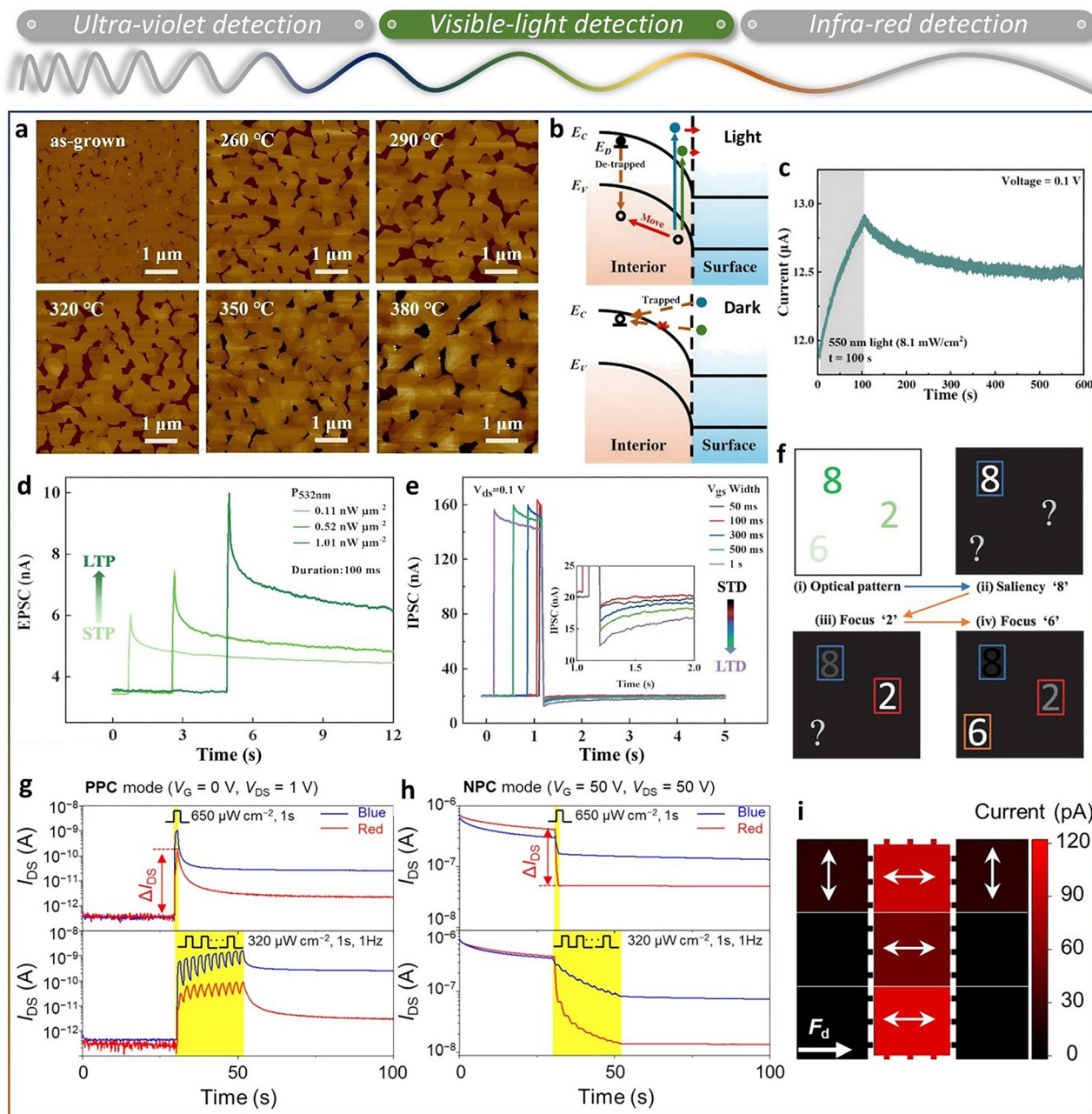


Fig. 3 (a) Atomic force microscope images based on various temperature of *in situ* thermal treatment. (b) Operation mechanism under visible illumination and dark. (c) Current–time curve under green illumination. (a)–(c) Reproduced with permission.¹²³ Copyright 2025 Elsevier. (d) EPSC–time curve from STP to LTP depending on light pulse intensity. (e) IPSC–time curve depending on voltage pulse width. (f) Simulation mechanism of neuromorphic vision system. (d)–(f) Reproduced with permission.¹²⁴ Copyright 2023 Wiley-VCH GmbH. Current–time curve when (g) PPC and (h) NPC mode operates. (i) 3 × 3 pixel device array for polarization imaging. (g)–(i) Reproduced with permission.¹²⁵ Copyright 2022 American Chemical Society.

potential of IR synaptic devices to serve as the fundamental hardware for autonomous and secure communication systems.

Shim *et al.* proposed a synapse electronic device based on a 0D/2D heterostructure designed to achieve efficient short-wavelength infrared (SWIR) detection alongside outstanding memorizing behaviors (Fig. 4a).¹³⁰ Driven by the quantum confinement effect of indium arsenide (InAs) quantum dots (QDs), the device exhibits significantly higher responsivity to SWIR (1060 nm) compared to the pristine tungsten diselenide

(WSe₂) device (Fig. 4b). Furthermore, the type-II band alignment established between the InAs QDs and WSe₂ facilitates the efficient spatial separation of photogenerated EHPs. This mechanism, coupled with charge trapping effects induced by QD ligands, effectively suppresses carrier recombination, thereby synergistically enhancing the photodetector performance and synaptic plasticity (Fig. 4c).

While such QD based heterostructures effectively target the SWIR region, extending detection capabilities into the broader



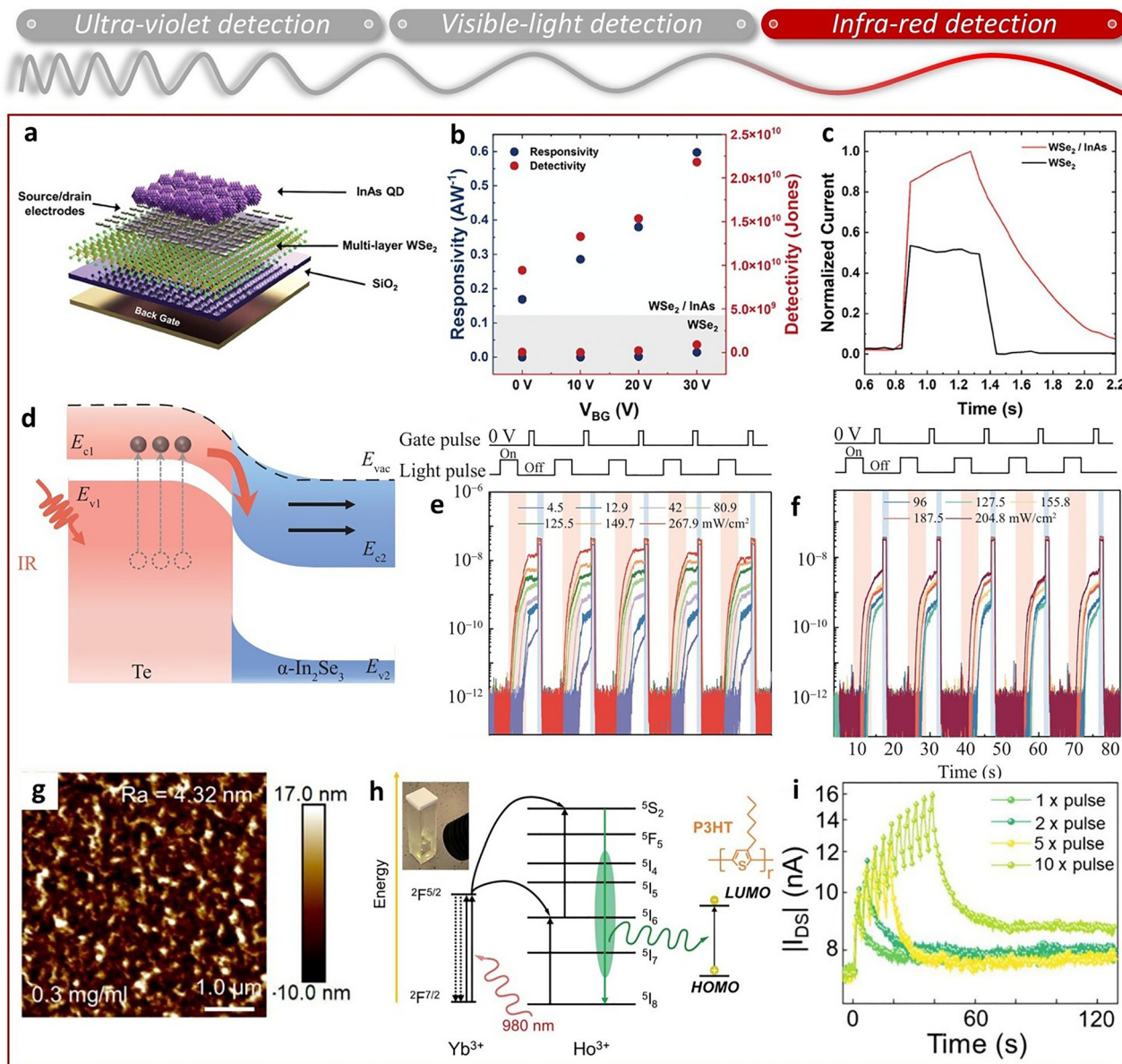


Fig. 4 (a) Device structure of 0D/2D heterostructure. (b) Responsivity and detectivity under SWIR illumination to compare WSe₂ and WSe₂/InAs. (c) Current–time curve under SWIR illumination to compare WSe₂ and WSe₂/InAs. (a)–(c) Reproduced with permission.¹⁵⁰ Copyright 2025 Wiley-VCH GmbH. (d) Energy band diagram of type-II heterostructure device under NIR illumination. (e) Current–time curve depending on light pulse intensity with 1.2 V gate pulse. (f) Current–time curve depending on light pulse intensity with 1.8 V gate pulse. (d)–(f) Reproduced with permission.¹⁵¹ Copyright 2023 Springer Nature. (g) Atomic force microscope image of LaF₃:Yb/Ho UCQDs doped P3FT film with high doping concentration. (h) Energy band diagram about upconversion luminescence under NIR illumination. (i) Current–time curve based on pulse counts. (g)–(i) Reproduced with permission.¹⁵² Copyright 2024 American Chemical Society.

telecommunication and sensing bands require materials with even narrower bandgaps and mechanism for active carrier regulation, such as ferroelectric modulation. Yan *et al.* proposed a near-Infrared (NIR) responsive optoelectronic synaptic transistor utilizing a type-II heterostructure composed of a tellurium (Te) NIR absorbing layer and ferroelectric α -In₂Se₃.¹⁵¹ Upon NIR illumination, EHPs are generated in the Te layer and subsequently undergo spatial separation due to the type-II heterostructure. The separation and recombination of these photogenerated carriers are regulated by the band

bending, which is controlled by the dipole alignment direction of the α -In₂Se₃ (Fig. 4d). Based on these features, the device successfully extends the operational range of 2D ferroelectric synaptic devices to the telecommunication (1550 nm) and sensing (1940 nm) NIR bands (Fig. 4e and f).

Apart from utilizing narrow bandgap inorganic semiconductors, another innovative strategy to enable NIR response (particularly in organic systems that lack intrinsic IR absorption) is the integration of upconversion materials that convert low energy photons into detectable visible light. Luan *et al.*



proposed a NIR responsive organic synaptic transistor by doping upconversion quantum dots (UCQDs) that serve as charge trapping sites.¹³² In the proposed device, increasing the doping concentration of UCQDs induces electrical degradation due to increased surface roughness, whereas it enhances the optical response owing to the increased density of trap sites. Accordingly, a film with a concentration of 0.3 mg mL^{-1} was utilized to optimize the optical properties (Fig. 4g). Upon NIR illumination, the incident light is absorbed by Yb^{3+} ions within the UCQDs, and the energy is transferred to Ho^{3+} ions. The excited Ho^{3+} ions then emit green light, which is reabsorbed by the channel. The UCQDs act as trap sites during this process, suppressing charge recombination (Fig. 4h). Based on these mechanisms, the device exhibits synaptic plasticity under NIR illumination (Fig. 4i).

These wavelength selective optoelectronic devices are of significant value due to their high responsivity within specific spectral ranges. However, they simultaneously face distinct challenges inherent to each spectrum. UV detection requires superior device stability to withstand high energy photons. Visible detection often suffers from noise interference. And IR detection is plagued by high dark currents. Overcoming these inherent limitations associated with each spectral region can lead to high-performance architectures. Furthermore, the next generation of optoelectronics should evolve beyond narrow band detection. By integrating advanced materials, structures, and defect engineering strategies, research should aim to realize broadband multimodal devices capable of covering the entire spectrum from UV to IR.

3. Identification of the methodology of trap or de-trap mechanism

The emulation of complex synaptic behaviors requires precise control over the trapping and de-trapping rates of photogenerated carriers. We categorize these methodologies into five primary approaches: interface engineering, heterostructure design, nanostructure defined trapping, chemical or electrochemical doping, and floating-gate architectures. To provide a consolidated perspective on how these diverse strategies impact actual device performance, Table 1 summarizes the key metrics of optoelectronic synapses categorized by their operational wavelength and trap engineering methodology. The representative metrics summarized in Table 1 include light intensity, readout voltage, recognition rate, and paired-pulse facilitation/depression (PPF/PPD). Light intensity represents the level of light stimulation used to generate photocarriers, affecting the amount of trapped carriers and the photogating behavior. Readout voltage refers to the electrical bias used to probe the synaptic current or conductance state, and low-voltage operation is generally preferred for energy-efficient device performance. Recognition rate represents the inference accuracy obtained when a device or device array is applied to a neuromorphic task, reflecting the practical applicability of the synaptic response. PPF/PPD describes the relative

enhancement or suppression of the second postsynaptic response induced by two successive stimuli and is widely used as a method to express the efficiency of plasticity. Collectively, these metrics provide a practical basis for comparing the performance of photosynaptic devices, and this comprehensive comparison clarifies the trade-offs inherent in various architectures, including interface engineering, heterostructures, and floating-gate.

3.1. Interface traps: charge trap site at the interlayer interface

Interface engineering allows for regulating the charge dynamics of optoelectronic devices. The interface between heterogeneous materials or grain boundaries often hosts a high density of trap states, which modulates channel conductance.

By controlling interfacial roughness,^{133,134} and energy band, these trap sites can be utilized to induce photogating effects and tunable synaptic plasticity. This section explores strategies that – utilize interface traps to enhance device performance, enabling functions such as photomultiplication and dual mode synaptic operations beyond the capabilities of bulk materials.

Islam *et al.* demonstrated a monolayer MoS_2 optoelectronic synaptic transistor utilizing a simple FET architecture consisting of source/drain electrodes, channel, and dielectric layer.¹³⁵ The device operation is governed by the gate voltage bias, which modulates the charge trapping dynamics. Under negative gate bias, photogenerated holes are effectively trapped at the interface of channel and dielectric, preventing recombination and inducing the persistence photoconductivity effect that mimics synaptic potentiation. Under positive gate bias, trapped carriers are released or recombined rapidly, acting as a photodetector. Furthermore, to elucidate the specific origin of the trap sites, the authors compared polycrystalline chemical vapor deposition (CVD) grown MoS_2 (Fig. 5a) with single crystal exfoliated MoS_2 (Fig. 5b). Despite the significant difference in grain boundary density, both devices exhibited substantial synaptic behaviors driven by the persistence photoconductivity effect. This observation confirms that the dominant trapping mechanism originates from the interface of channel and dielectric rather than grain boundaries although the presence of grain boundaries can influence the retention time. With comparison of ambient and vacuum conditions, O_2 and H_2O absorption in the ambient condition causes much more retention than in the vacuum condition (Fig. 5c).

While the aforementioned MoS_2 device effectively utilized interface traps, it still relied on electrical gate bias to modulate the trapping dynamics. To achieve fully autonomous optical modulation without external voltage gating, recent strategies have shifted towards spatially engineering defect distributions within the channel structure. Hu *et al.* proposed an all optically controlled memristor utilizing a bilayer indium gallium zinc oxide (IGZO) structure with distinct oxygen concentrations, enabling SET/RESET operations solely through light induced charge trapping at interface of homojunction (Fig. 5d).¹³⁶ Due to the oxygen concentration gradient, a potential barrier forms at the oxygen deficient (O_D) IGZO side, while a potential well forms at the oxygen rich (O_R) IGZO side. High energy blue light



Table 1 Comparison of the different optoelectronic devices based on wavelength region, trap dynamics methodology, and device performance properties in this review

Wavelength [nm]	Stimulation	Trap source	Simulation recognition rate [%]	Intensity [mW cm ⁻²]	Readout voltage [V]	PPF/PPD index [%]	Simulation	Ref.
276, 365	Light	Active layer trap site	N/A	1–9	0.01	142	N/A	117
254–365	Light	Doping	96.7	0.115–0.602	0.1	180	Fingerprint data	118
365	Light, voltage	Interface	95	0.4–15.98	0.5	≈166	MNIST	119
450, 550	Light	Active layer trap site	N/A	5.2	N/A	173	N/A	123
450, 532, 650	Light, voltage	Interface	99.12	7–101	N/A	≈143/≈143	MNIST	124
405, 645	Light	Interface	N/A	0.032–0.65	0, 50	N/A	N/A	125
450, 1060	Light	Interface	96.55 (digit MNIST), 86.13 (fashion MNIST)	12.99	20, –20	≈99.8/≈122	Digit MNIST, fashion MNIST	130
1550, 1940	Light, voltage	Interface, heterostructure	82.7	4.5–293	0	N/A	Fashion MNIST	131
980	Light	Active layer trap site	N/A	3.5–650	0.5	≈138	N/A	132
450	Light	Interface	N/A	6–13.5	–3 to 3	203.5	N/A	135
420–1000	Light	Interface	N/A	0.0144–0.024	0.01	N/A	N/A	136
530	Light	Interface	91.7	0.1–0.85	10, 20	≈119.8	MNIST	137
450–808	Light	Heterostructure	N/A	0.002–0.5	40, –40	160 (red)	N/A	141
365, 680	Light	Heterostructure	N/A	≈5–12	0	≈116	N/A	142
375–1310	Light, voltage	Heterostructure	N/A	N/A	0	158	N/A	143
455	Light, voltage	Nanostructure	92.6	0.18–0.45	–1, –2, –10, –20	N/A	MNIST	148
455, 530, 660	Light, voltage	Nanostructure	97.4 (MNIST), 89 (ECG), 93.4 (EMG), 83.8 (CIFAR-10)	0.26–1.42	7	N/A	MNIST, ECG, EMG, CIFAR-10	149
255	Light	Nanostructure	N/A	0.0057–0.0167	N/A	0	N/A	150
532	Light	Doping	N/A	0.6	0	153	N/A	168
450, 500, 550	Light, voltage	Doping	91 (activation rate)	2–7	–0.6	≈185	Facial recognition	169
254, 365	Light, voltage	Doping	95.4 (n-type), 94.2 (p-type)	0.03–13.64	0	111 (n-type)	MNIST	170
450, 532, 635	Light, voltage	Floating-gate	90.77	N/A	0.1	170.5 (p-type) ≈242 (optoelectronic), ≈144 (electronic)	N-MNIST	174
455, 530, 660	Light + voltage	Floating-gate	91.37	0.53, 0.54, 0.55	0	N/A	Fashion MNIST	175
400, 514	Light, voltage	Floating-gate	N/A	0.0254–0.127	0	N/A	N/A	176

functions as a SET pulse by ionizing oxygen vacancies to narrow the barrier width, promoting electron tunneling. Conversely, low energy NIR light serves as a RESET pulse by activating trapped electrons to recombine with ionized vacancies (Fig. 5e). By using these pulses as pre and post synaptic spikes, the device demonstrated synaptic plasticity, including potentiation by blue pulses and depression by NIR pulses (Fig. 5f).

Recent strategies have turned to engineer the physical morphology of interfaces to integrate distinct functionalities, such as memory and synaptic plasticity, into a single device architecture. Kim *et al.* proposed dual function optical synaptic and memory transistors within a single device by controlling interface roughness and trap density.¹³⁷ In this architecture, the buried layer serves distinct roles depending on the operation mode (Fig. 5g). In memory mode, it functions as a floating-gate where programming and erasing are achieved by charge trap and de-trap at substrate and floating-gate interface through parylene dielectric under bias and illumination

(Fig. 5h). In synapse mode, it acts as a roughness inducing layer. Thickness optimization of lower *N,N'*-ditridecyl-3,4,9,10-perylene-tetracarboxylic diimide (PTCDI-C₁₃) plays a critical role, depending on the property of its high crystallinity and strong π - π stacking. Therefore, PTCDI-C₁₃ exhibits a significant increase in grain size and surface roughness as film thickness increases. While a thin layer lacks sufficient trap sites at the interface of parylene and upper PTCDI-C₁₃, an excessively thick layer hinders carrier transport of upper PTCDI-C₁₃ due to severe roughness. The optimized device successfully modulates synaptic weight *via* the photogating effect induced by electron trapping at the interface under light illumination (Fig. 5i).

Adopting interface traps allows for sophisticated control over carrier dynamics, facilitating the development of high quality, multifunctional optoelectronic devices. Nevertheless, improvements are needed to address the following limitations: uncontrolled defect densities can induce degradation in device performance and impede efficient carrier transport. To fully



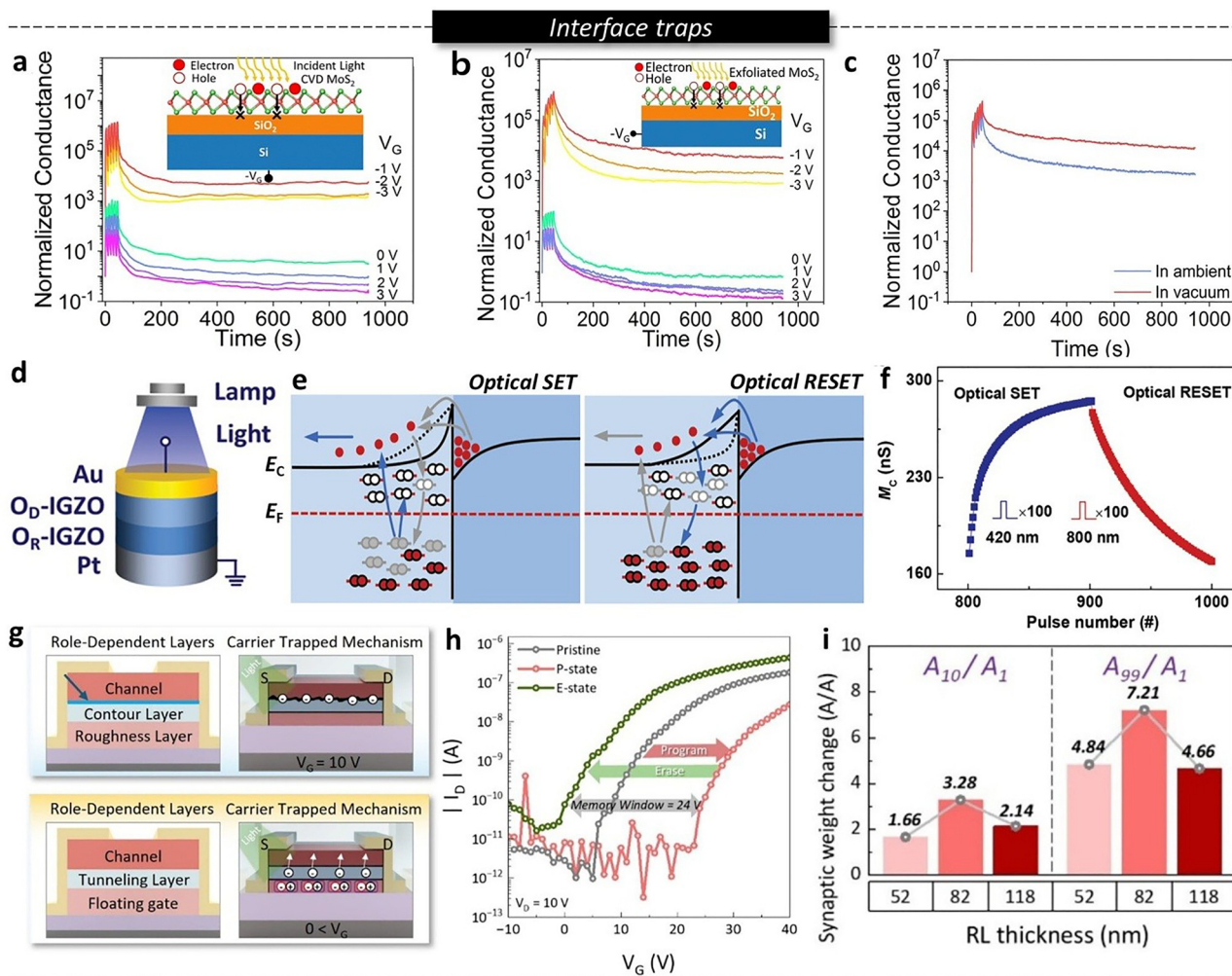


Fig. 5 (a) Current–time curve of CVD grown monolayer MoS₂ transistor. (b) Current–time curve of exfoliated monolayer MoS₂ transistor. (c) Current–time curve to compare circumstance under ambient and vacuum condition. (a)–(c) Reproduced with permission.¹³⁵ Copyright 2020 Springer Nature. (d) Device structure of bilayer IGZO structure. (e) Energy band diagram to explain the device mechanism. (f) Optical SET and RESET operation based on illumination wavelength. (d)–(f) Reproduced with permission.¹³⁶ Copyright 2021 Wiley-VCH GmbH. (g) Concept of study: contouring and tunneling layer. (h) Transfer curve that exhibits programming and erasing operations. (i) Synaptic weight based on roughness layer thickness. (g)–(i) Reproduced with permission.¹³⁷ Copyright 2025 American Chemical Society.

take advantage of interface traps, precise optimization of interfacial states and the development of robust defect engineering are indispensable.

3.2. Heterostructure-induced trapping: charge trap site within a specific layer

Constructing a heterostructure is a strategy to spatially separate photogenerated carriers and extend their lifetime by reducing recombination. Through band alignment, built in potential effectively segregates electrons and holes into distinct regions. This spatial separation not only suppresses immediate recombination but also directs carriers toward trap sites, located at internal defects and heterostructure interfaces as well as additional trap sites induced by environmental interactions. The recent studies demonstrate how such engineered trapping mechanisms maximize persistent photoconductivity and

enable robust nonvolatile memory and synaptic emulation by effectively managing carrier dynamics.^{138–140}

Huang *et al.* proposed a dual mode learning ambipolar synaptic phototransistor capable of broadband operation from the visible to NIR regions by employing a heterojunction channel layer with different spectral response layers.¹⁴¹ This device is integrated with visible sensitive PEA₂SnI₄ and NIR sensitive Y6, allowing for full spectrum responsivity. The device realizes both EPSC and IPSC within a single device, depending on the gate bias and excitation wavelength. EPSC is achieved by NIR light, where EHPs are generated in Y6, and the holes flow into the PEA₂SnI₄ and are bound at the heterostructure interface (Fig. 6a). In contrast, IPSC is activated by visible light under positive bias, where both layers generate carriers, and electrons are trapped by Sn vacancies within PEA₂SnI₄. This capture induces hole accumulation that recombines with electrons in the channel to suppress current (Fig. 6b).



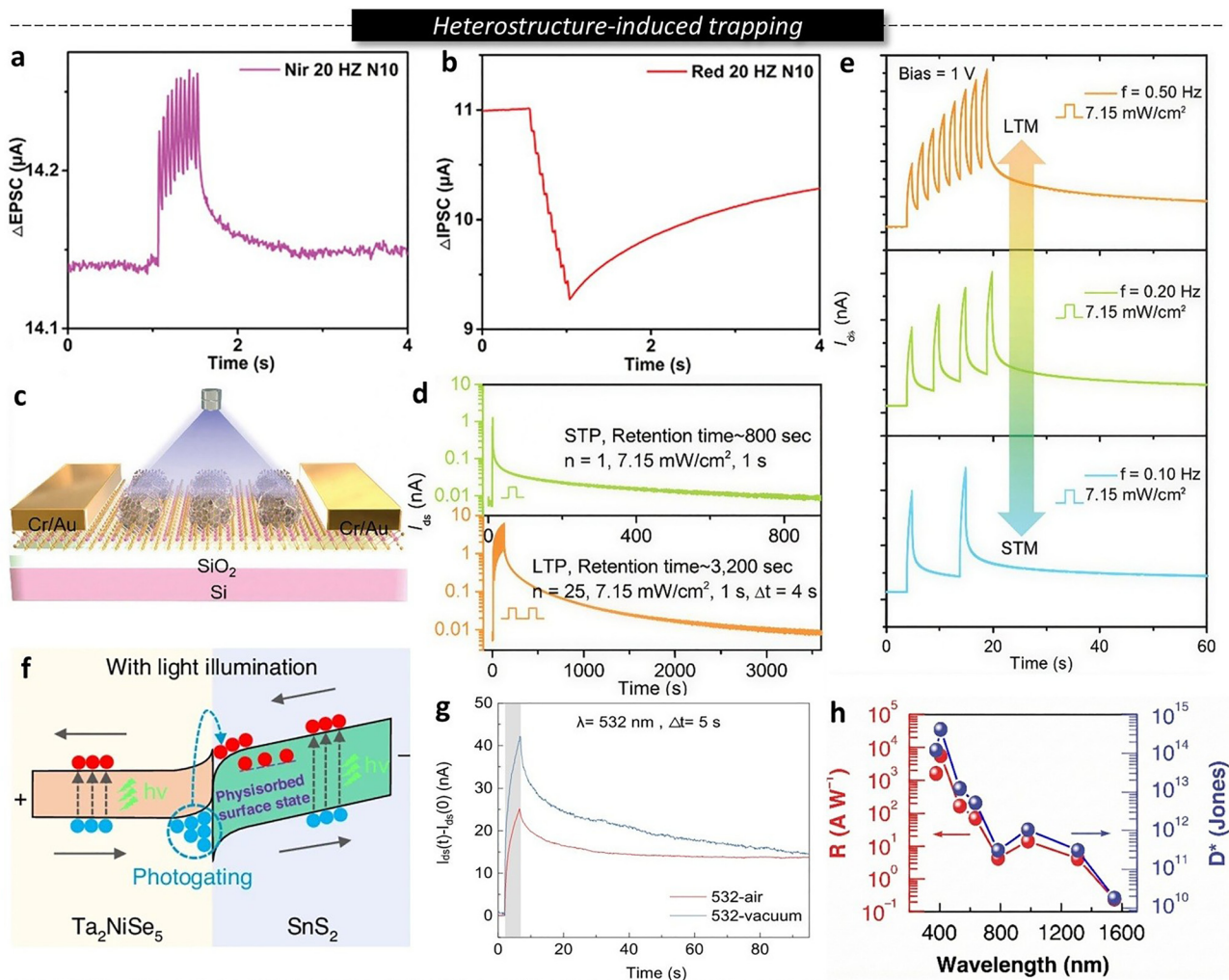


Fig. 6 (a) EPSC–time curve under NIR illumination. (b) IPSC–time curve under red illumination. (a) and (b) Reproduced with permission.¹⁴¹ Copyright 2021 Wiley-VCH GmbH. (c) Device structure of MoS₂@Fe₇S₈ transistor. (d) Retention time comparison based on light pulse counts. (e) STM to LTM conversion based on light pulse frequencies. (c)–(e) Reproduced with permission.¹⁴² Copyright 2024 Wiley-VCH GmbH. (f) Band diagram to explain the device mechanism. (g) Current–time curve to compare PPC effect under air and vacuum condition. (h) Responsivity and detectivity based on wavelength region. (f)–(h) Reproduced with permission.¹⁴³ Copyright 2025 Springer Nature.

While planar heterojunctions enable versatile spectral discrimination, novel three dimensional architectures offer a geometric approach to optimizing charge trapping for high linearity neuromorphic computing without the need for external gating. Deng *et al.* proposed a gate free neuromorphic phototransistor exhibiting long retention times and highly linear synaptic weight modulation by utilizing a heterostructure composed of carrier transportation and trapping layers.¹⁴² This was realized using a unique core shell heterostructure, where a dome shaped MoS₂ shell covers metallic Fe₇S₈ core (Fig. 6c). Under illumination, EHPs are generated in the MoS₂ shell, after which electrons are driven into the metallic Fe₇S₈ core by the built-in potential and Schottky barrier formed at the interface, subsequently becoming trapped in the core's abundant intrinsic defect sites. Based on this defect-based trapping mechanism, the device achieves impressive retention times over 3200 s for repeated pulses (Fig. 6d) and exceptional

linearity in synaptic conductance modulation, thereby proving its suitability for neuromorphic computing (Fig. 6e).

Complementary to engineering internal structural defects, utilizing surface interactions with ambient gas molecules provides an additional degree of freedom to extend carrier lifetimes and maximize device responsivity. Tan *et al.* proposed physisorption assisted optoelectronic synaptic transistors designed to enhance responsivity and retention time through carrier separation within a heterostructure and localized state formation *via* surface physisorption.¹⁴³ In this device, the formation of a Ta₂NiSe₅/SnS₂ type-II heterostructure induces a built-in potential that blocks photogenerated holes to trigger the photogating effect (Fig. 6f). O₂ and H₂O molecules adsorbed on the SnS₂ surface create localized states that trap electrons and suppress recombination (Fig. 6g). This dual mechanism effectively extends carrier lifetime and maximizes the persistent photoconductivity effect. By utilizing the heterostructure and



atmospheric physisorption, the device achieved exceptional performance across the UV to NIR spectrum, including a responsivity exceeding 166.3 A W^{-1} , a high EQE of 38810%, and a specific detectivity of 2.50×10^{14} Jones (Fig. 6h).

Suppressing undesirable defect sites is a crucial strategy to maximize trapping efficiency in heterostructure devices. Ercan *et al.* proposed this by employing a thickness-optimized p-6P template to induce weak epitaxial growth of DNTT channel, resulting in a highly ordered and defect-minimized interface.¹⁴⁴ This structure rapidly transfers photogenerated electrons into deep trap sites within p-6P layer. By intentionally minimizing interface traps and facilitating electret-based charge trapping, the device achieves a PPF ratio of 206% and operates with a low energy consumption of 0.54 fJ per synaptic event under zero-gate bias.

The strategic construction of heterostructures offers a versatile platform to decouple charge generation from recombination, thereby overcoming the limitations of single material devices. As demonstrated, the ability to spatially separate carriers *via* band alignment and guide them toward specific trap sites enables the realization of broadband responsivity, high linearity, and robust memory retention. However, this increased structural complexity introduces challenges regarding interfacial quality and long-term stability. Relying on mechanisms like surface physisorption or specific defect engineering requires precise control to prevent environmental instability and unwanted recombination. From this point of view, the future advancement of heterostructure based synaptic devices relies on optimizing the synergy between band engineering and trap distribution to achieve a balance between maximized trapping efficiency and reliable device operation.

3.3. Nanostructure-defined traps

In a nanostructured device, geometric surface morphology and an expanded interfacial area are often associated with variations in the formation and spatial distribution of charge trap states. From a synaptic perspective, these structurally induced trap states enable temporary charge storage and time dependent carrier release. Under optical stimulation, photogenerated carriers can be selectively captured by traps associated with nanostructure defined interfaces, leading to gradual conductance modulation rather than abrupt switching. By controlling parameters such as porosity and interface density, the spatial accessibility and lifetime of trapped charges can be effectively tailored, enabling a continuum of plasticity behaviors ranging from short term to long term memory.^{145–147} This structural approach provides a versatile route to optoelectronic synapses, where learning behavior emerges from the interplay between light excitation and trap modulated carrier dynamics.

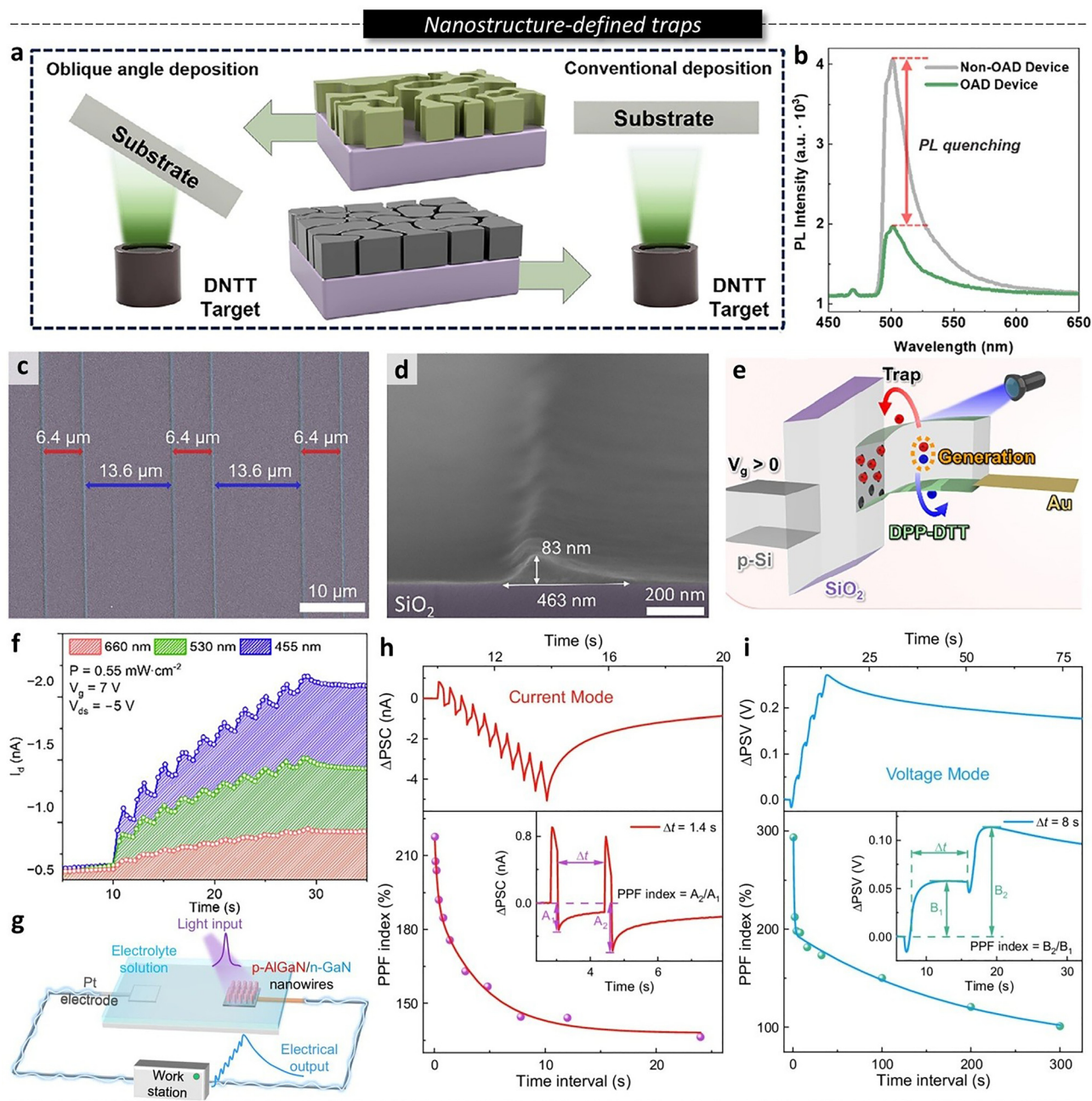
Lee *et al.* demonstrated that oblique angle deposition (OAD) can be used to deliberately induce nanostructured morphologies in organic semiconductor channels, enabling optoelectronic synaptic behavior without introducing additional functional layers.¹⁴⁸ By depositing the active material at a high oblique angle, porous and anisotropic structures were formed, leading to spatially nonuniform interfaces within the

channel. By controlling the thermal deposition angle, porous and anisotropic morphologies are formed distinct from conventionally deposited planar films (Fig. 7a). Scanning electron microscopy (SEM) revealed nonuniform grain boundaries and void rich regions, indicating that the nanostructure formation originates from shadowing effects inherent to the OAD process. From a trap-based dynamics, these OAD induced morphological features provide spatially heterogeneous interfaces where localized charge trap states can be formed preferentially. Instead of introducing additional trap layers or complex device structures, photoresponsive trapping behavior can be achieved through structural modification alone. Photoluminescence quenching observed in the nanostructured films suggests an increased contribution of nonradiative recombination pathways, which are frequently linked to carrier trapping and subsequent relaxation dynamics (Fig. 7b). Under optical stimulation, photogenerated carriers are selectively trapped at morphology defined interfacial trap sites, leading to gradual conductance modulation characteristic of synaptic operation. The gate tunable response further indicates that the trapped charges interact with the channel electrostatics, enabling controlled potentiation and depression dynamics.

In contrast to OAD induced nanostructured films, nanowire based channel architectures reported by Choi *et al.* rely on geometric confinement along elongated nanowire channels to regulate charge transport and trapping behavior.¹⁴⁹ The elongated geometry of nanowires gives rise to extended interfaces along the channel, where surface and interfacial states may contribute to charge trapping behavior (Fig. 7c and d). Within these nanowire structures, photogenerated carriers are preferentially captured at trap states distributed along the nanowire surface and at the nanowire and dielectric interface. These traps primarily influence carrier lifetime, enabling a gradual accumulation of channel conductance under optical stimulation (Fig. 7e). This behavior manifests as a progressive increase in postsynaptic current with repeated stimulation, consistent with synaptic potentiation driven by carrier trapping and delayed release (Fig. 7f).

Liu *et al.* reported a nanowire based optoelectronic synapse that integrates trap-mediated charge storage with electrolyte assisted charge dissipation, enabling dual modal synaptic plasticity.¹⁵⁰ While nanowire architectures are similarly employed, the synaptic mechanism differs from earlier general nanowire synapses by incorporating an additional electrochemical dissipation pathway. The device employs vertically aligned p-AlGaIn/n-GaN nanowires immersed in an electrolyte, where photoexcitation generates carriers that are partially stored within the nanowires while concurrently interacting with the surrounding chemical environment. This architecture introduces a distinct trapping landscape defined not only by the nanowire surface and nanowire–dielectric interface, but also by the nanowire–electrolyte junction (Fig. 7g). Upon optical stimulation, photogenerated carriers accumulate within the nanowires and relax through processes associated with photo induced band bending and electrolyte-mediated electrochemical interactions. The persistence of trapped carriers enables





synaptic weight modulation beyond the illumination period, producing STP or LTP depending on the electrical boundary condition, with rapid relaxation in current mode and prolonged charge retention in voltage mode (Fig. 7h). The nanowire geometry amplifies the influence of interfacial trap states by increasing the accessible surface area for trapping and electrochemical interaction, illustrating that synaptic behavior arises

from the coupled interplay between trap-assisted charge storage and electrolyte-mediated processes (Fig. 7i).

Semiconducting single-walled carbon nanotubes (sc-SWCNTs) are a promising class of nanomaterials for next-generation electronic devices due to their high charge-carrier mobility ($> 20 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$), low threshold voltage ($< 2 \text{ V}$), and excellent mechanical properties.^{151,152} However, as-synthesized



SWCNTs exhibit a range of chiralities, necessitating post-synthesis separation to isolate semiconducting species for applications such as field-effect transistors. The use of conjugated polymers has emerged as an effective approach for the selective extraction and purification of sc-SWCNTs.¹⁵³ A variety of polyfluorene- and polythiophene-based copolymers have been reported in the literature to enable high-purity sc-SWCNT separation. Importantly, the molecular structure of the polymer influences not only the selectivity of nanotube extraction, its processability but also its optical absorption characteristics.¹⁵⁴ As a result, polymer–nanotube complexes can exhibit distinct photoresponses depending on the polymer structure and the wavelength of incident light. Dallaire *et al.* demonstrated that variations in polymer structure can induce repeatable and reversible threshold voltage shifts (ΔV_T) ranging from 0 to 15 V under illumination, depending on the chosen polymer and excitation wavelength.¹⁵⁵ sc-SWCNTs are also prone to interfacial charge traps, which can be engineered through interfacial modification of the dielectric layer. Tousignant *et al.* demonstrated tunable changes in sc-SWCNT device performance and charge-trap density using green bilayer dielectrics^{156–158} and ionic-based dielectrics^{159–161} as viable transistor platforms. These findings highlight polymer-wrapped sc-SWCNTs as a powerful platform for tunable light-responsive devices, positioning them as promising candidates for phototransistors and optoelectronic synapses.

Beyond utilizing polymers to modify other nanomaterials, the intrinsic self-assembly properties of polymers can be directly applied to engineer highly ordered, morphologically tailored trap environments. Mulia *et al.* proposed synaptic phototransistors utilizing carbohydrate-based block copolymers (BCPs).¹⁶² While hydroxyl groups within sugar blocks trap electrons under illumination, solvo-microwave annealing induces highly ordered orientations, thereby successfully optimizing the morphology of charge trap sites. Rather than the number of trapped electrons, optimized orientation of nanostructure and morphological ordering are the critical factors that govern trap efficiency and neuromorphic capability. In terms of morphology-dependent trap efficiency development, Ercan *et al.* proposed that sonication and UV treatment induce the growth of nanofibrils, conformational reorganization, and π - π stacking, leading to improved molecular ordering.¹⁶³ These methods increase the interfacial area available for charge trapping in one-dimensional polymer/perovskite composite nanostructures and create efficient pathways for hole transport.

Nanostructured synaptic device offers several advantages for trap/de-trap-based optoelectronic synapses. Their unique geometric features and enlarged interfacial areas increase the density and accessibility of charge trapping sites, allowing synaptic plasticity to be achieved through intrinsic structural design rather than additional functional layers. However, nanostructure-enabled trapping also introduces inherent limitations. The spatially heterogeneous distribution of trap states can lead to device-to-device variability and reduced reproducibility. In addition, the increased role of interfaces may accelerate degradation under prolonged operation, posing

challenges for long-term stability and large-scale integration. While nanostructured architectures provide a powerful platform for taking advantage of charge traps as functional synaptic elements, careful control of interface quality, structural uniformity, and environmental coupling remains essential for translating these concepts into reliable and scalable neuromorphic systems.

3.4. Chemical and electrochemical doping

Chemical doping has traditionally been employed to modulate carrier concentration and threshold voltage. However, doping can also reshape the electronic properties by introducing impurity-related states within the band structure. From a synaptic perspective, such modifications provide an additional degree of freedom for regulating temporal responses, enabling gradual conductance modulation and memory effects that extend beyond the duration of stimulation.^{164,165} Accordingly, doping can be considered not only as a means of tuning conductivity, but also as a viable approach for introducing trap-assisted plasticity in optoelectronic synapses.^{166,167}

Ma *et al.* investigated chemical doping of WSe₂ through SnCl₄ treatment as a means of modifying charge trapping behavior in optoelectronic synaptic devices.¹⁶⁸ X-ray photoelectron spectroscopy revealed systematic shifts in the W 4f and Se 3d core levels after doping, indicating a treatment-induced modification of the electronic structure consistent with p-type behavior (Fig. 8a and b). The appearance of distinct Sn 3d peaks further confirms the presence of Sn species associated with the WSe₂ channel, supporting the involvement of impurity-related electronic states beyond simple surface adsorption effects (Fig. 8c). These impurity-related states modify the carrier dynamics under optical stimulation, facilitating residual photoconductive responses through trap-assisted charge storage. As shown in Fig. 8d, SnCl₄-treated WSe₂ devices exhibit a gradual and cumulative modulation of excitatory postsynaptic current under repeated optical stimulation, in contrast to the more transient responses observed in pristine devices. The influence of chemical doping is further reflected in image-based photoresponse measurements (Fig. 8e–g), where image reconstruction based on the photoresponse of doped devices reveals enhanced contrast depending on the applied cut-off frequency.

Distinct from impurity-induced doping in solid-state semiconductors, alternative strategies based on electrochemical doping have also been reported. In this context, Chen *et al.* presented an optoelectronic synapse based on photon modulated electrochemical doping, in which light indirectly regulates charge retention through ion transport within an organic electrochemical transistor architecture.¹⁶⁹ Different from conventional solid-state doping approaches that rely on static impurity states, this strategy uses light-induced modulation of electrochemical doping, introducing a dynamic charge retention landscape governed by coupled electronic and ionic processes. As illustrated in Fig. 8h, optical stimulation perturbs the electrochemical state of the channel, inducing ion redistribution within the organic electrochemical transistor. The



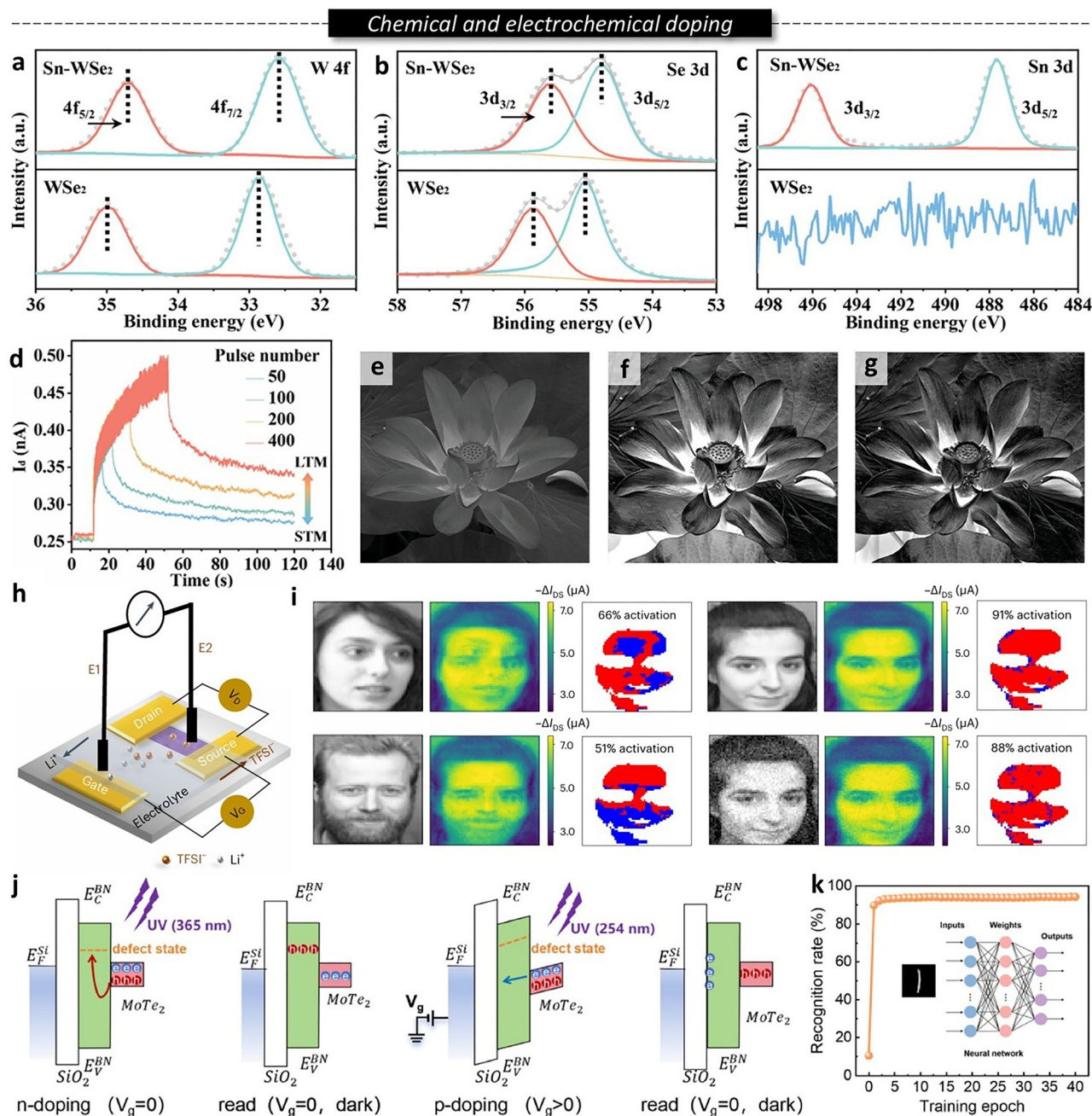


Fig. 8 (a) W 4f peak, (b) Se 3d peak, and (c) Sn 3d peak transfer after SnCl₄ solution treatment with comparison between Sn-WSe₂ and WSe₂. (d) Current–time curve based on applied pulse counts, showing conversion from short-term to long-term memory. (e) Pristine image for high-pass filtering. High-pass filtered image with (f) 0.95 Hz and (g) 5 Hz cut-off frequency. (a)–(g) Reproduced with permission.¹⁶⁸ Copyright 2024 Wiley-VCH GmbH. (h) Device structure of organic electrochemical transistor. (i) Various human images for facial recognition simulation. (h) and (i) Reproduced with permission.¹⁶⁹ Copyright 2023 Springer Nature. (j) Energy band diagram to explain operation mechanism based on illuminated wavelength region. (k) Neural network simulation recognition rate. (j) and (k) Reproduced with permission.¹⁷⁰ Copyright 2025 Wiley-VCH GmbH.

redistributed ions modulate the effective doping level of the channel, resulting in a gradual relaxation of the channel conductance after illumination. Importantly, the synaptic behavior in this system is governed by the interplay between electronic excitation and ionic redistribution, rather than by fixed defect states. The degree of conductance retention and the emergence of STP or LTP can be tuned by optical parameters

and gate bias conditions, reflecting modulation of electrochemical doping dynamics. In Fig. 8i, the device was evaluated using a facial image recognition task, where spatial features of the input face image were reconstructed from the synaptic response under different signal-processing conditions. This behavior enables spatial image representation with memory-like traits, demonstrating that electrochemical doping provides



a viable ion-mediated pathway for synaptic functionality that complements conventional trap-based approaches.

Another approach utilizes optically induced charge trapping to reversibly modulate the doping state of 2D semiconductors without introducing chemical dopants or mobile ions. In this strategy, the effective carrier polarity of the channel is controlled through photoexcitation of defect states in the insulating layer and at the semiconductor-dielectric interface. Pei *et al.* demonstrated a UV-programmable optoelectronic synapse based on a MoTe₂/h-BN transistor, where the channel doping polarity can be switched between n-type and p-type states depending on the UV wavelength and gate bias conditions.¹⁷⁰ As illustrated in Fig. 8j, UV illumination induces charge transfer into defect states within the h-BN layer or at its interface, thereby programming the effective doping state of the MoTe₂ channel without introducing chemical impurities. Depending on the UV wavelength and gate bias conditions, this optically induced charge trapping enables reversible switching between n-type and p-type channel behavior. Based on the resulting synaptic characteristics, the device performance was further evaluated in a neural network simulation for handwritten digit recognition (Fig. 8k). By mapping experimentally extracted synaptic weight updates to a virtual neural network, recognition accuracies exceeding 94% were achieved, indicating that optically programmed solid-state doping can effectively support neuromorphic computing.

The chemical and electrochemical doping provide a versatile means to modulate the synaptic behaviors of optoelectronic devices. By precisely controlling the concentration and distribution of dopants, it is possible to tailor the trap density and energy levels, thereby optimizing essential synaptic functions such as memory retention and plasticity. However, despite these advantages, several challenges remain. The long-term stability of doped devices can be compromised by the diffusion of dopants or chemical degradation over time. Furthermore, achieving high spatial uniformity and reproducibility in large-scale fabrication remains a hurdle for practical neuromorphic integration.

3.5. Floating-gate charge trapping architectures: intentionally induced charge trap site

While the preceding Sections 3.1–3.4 focused on synaptic behaviors emerging from unintended defects or intrinsic material properties, floating-gate architectures represent a distinct approach where charge-trapping sites are deliberately engineered into the device structure. In these systems, a discrete trapping layer is spatially isolated by a dielectric or tunneling barrier, allowing for the deterministic injection and storage of photogenerated carriers. Because the trapped carriers are physically confined by these potential barriers, they are less likely to be released without specific external triggers (such as electrical reset pulses or detrapping mechanisms). This configuration enables the realization of distinct volatile and non-volatile states, which naturally leads to superior LTP and robust memory characteristics.¹⁷¹ Floating-gate-based optoelectronic synapses have been widely reported as a reliable platform for

achieving precise and stable weight modulation in neuromorphic computing.^{172,173}

By utilizing 2D Te nanoplates as the floating-gate, Zha *et al.* proposed a multifunctional floating-gate memory device capable of switching between volatile and non-volatile characteristics.¹⁷⁴ The device operation is governed by the depth of carrier trapping determined by the pulse stimulus intensity. High intensity optical or electrical pulses make carriers capture deep traps within the floating-gate, resulting in non-volatile behavior (Fig. 9a). In contrast, low intensity stimuli lead carriers to capture in shallow traps at the MoS₂ channel or h-BN interface, exhibiting volatile characteristics (Fig. 9b and c).

Beyond modulating memory retention characteristics through stimulus intensity, achieving selective synaptic plasticity based on the spectral wavelength of light enables more sophisticated visual information processing. By modulating synaptic plasticity based on wavelength selective responses, Kang *et al.* proposed a spectrally tuned floating-gate synaptic transistor.¹⁷⁵ The device utilizes (*E*)-2-(2-((6-(di-*p*-tolylamino)-4,4-dimethyl-4*H*-indeno[1,2-*b*]thiophen-2-yl)methylene)-3-oxo-2,3-dihydro-1*H*-inden-1-ylidene)malononitrile (Dta-Inth-IC) as a red sensitive floating-gate and dinaphtho[2,3-*b*:2',3'-*f'*]selenopheno[3,2-*b*]selenophene (DNSS) as a blue sensitive channel. Synaptic behavior is governed by the wavelength dependent carrier dynamics, specifically the distinct recombination rate. Under red illumination, EHPs are generated within the floating-gate, and photogenerated holes subsequently transfer to the channel, resulting in the effective accumulation of electrons in the floating-gate. In contrast, blue illumination generates carriers primarily within the channel where rapid recombination dominates (Fig. 9d). This leads to minimal electron injection into the floating-gate, resulting in weak synaptic potentiation (Fig. 9e).

While spectral tuning optimizes optical perception, the ultimate goal of neuromorphic hardware is to seamlessly integrate these optical functions with robust electrical memory operations, which can be realized through advanced nano floating-gate architectures. By introducing perovskite nanocrystals (NCs) based structure, Moon *et al.* proposed nano floating-gate transistors capable of implementing both electrical memory and photosynaptic functions.¹⁷⁶ The device features a unique architecture where NCs are embedded within the insulating polymer layer (PS) (Fig. 9f). The operation relies on the dual functionality of this nanocomposite layer. Under illumination, NC within the PS layer acts as a photocarrier generation layer to generate EHPs. The photogenerated holes are transferred to the channel to enhance conductivity, while the electrons are trapped within the NCs (Fig. 9g). When electrical bias is applied, NC-PS operates as a tunneling layer, facilitating the transport of carriers between the channel and floating-gate *via* tunneling (Fig. 9h).

The floating-gate architecture serves as a robust platform for realizing reliable and precise optoelectronic synapses by physically isolating charge storage sites from the transport channel. As demonstrated, the presence of a discrete trapping layer



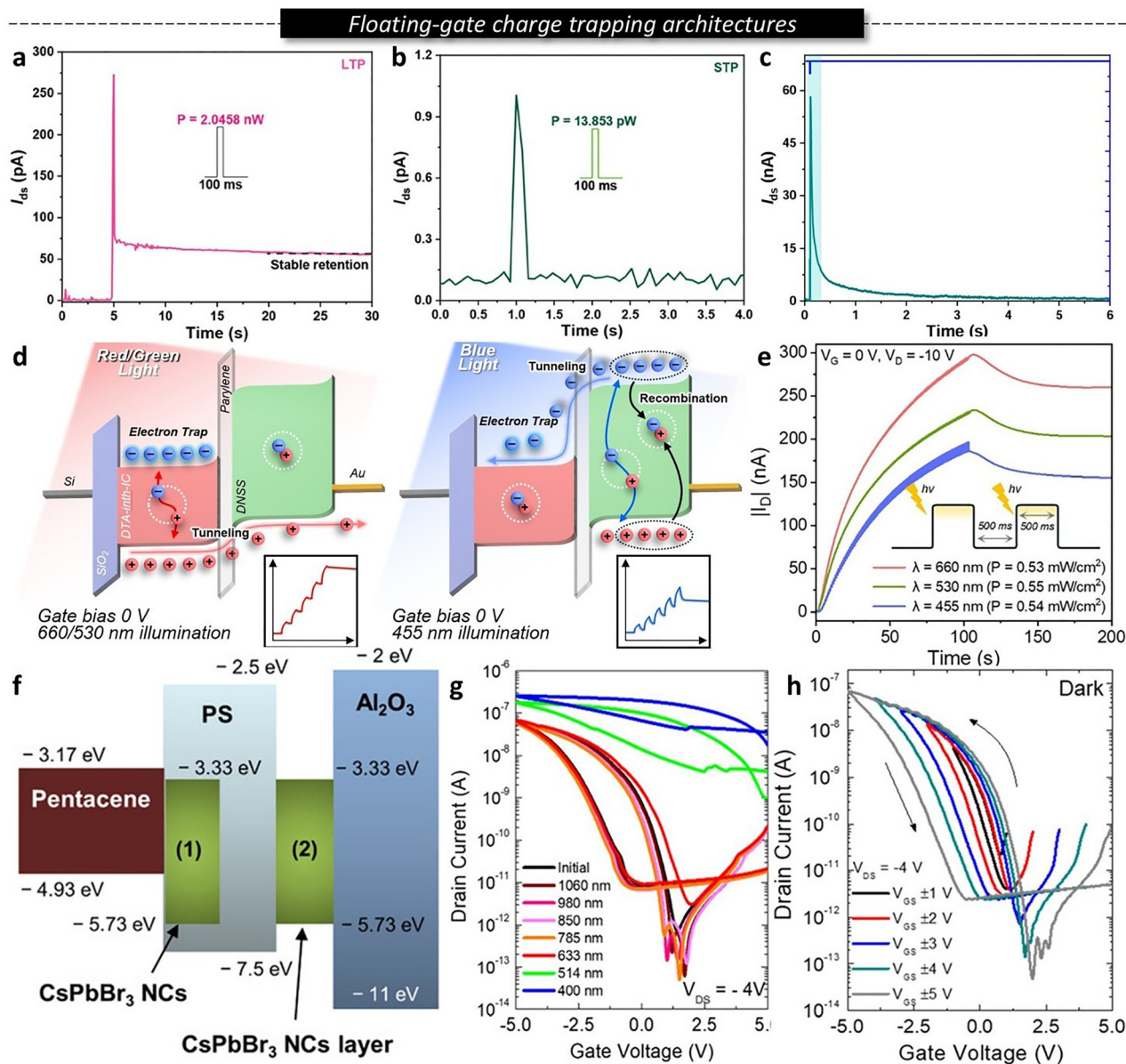


Fig. 9 Current–time curve with (a) high and (b) low light intensity. (c) Current–time curve with weak voltage pulse. (a)–(c) Reproduced with permission.¹⁷⁴ Copyright 2024 Wiley-VCH GmbH. (d) Energy band diagram to explain device operation under blue and red illumination. (e) Current–time curve based on illuminated light wavelength. (d) and (e) Reproduced with permission.¹⁷⁵ Copyright 2025 Wiley-VCH GmbH. (f) Energy band diagram of NCs based structure. (g) Transfer curve based on illuminated wavelength region. (h) Transfer curve based on applied voltage bias. (f)–(h) Reproduced with permission.¹⁷⁶ Copyright 2023 Wiley-VCH GmbH.

protected by a tunneling barrier allows for the deterministic regulation of carrier injection and retention, enabling versatile functionalities ranging from intensity dependent plasticity switching to spectrally tuned recognition and dual mode operations. However, the performance of these devices is critically dependent on the quality and dimensions of the tunneling barrier, where a tradeoff often emerges between programming speed and data retention time. Furthermore, the structural complexity of embedding nanostructured floating-gates within insulating layers requires rigorous fabrication control to prevent leakage currents.

Conclusion and future challenges

This review summarizes recent progress in optoelectronic synaptic devices that exploit charge trapping phenomena as functional elements rather than parasitic defects. We discussed how trap-mediated carrier dynamics can be engineered across different wavelength regimes and device architectures to realize synaptic functions such as analog memory, persistent photoconductivity, and light-responsive plasticity. We have reviewed various trap-assisted optoelectronic devices categorized by their absorbed wavelengths and operational methodology. While it is



demonstrated that the trapping/de-trapping mechanisms positively influence the enhancement of the device performance, several limitations and challenges remain for future development. Regarding wavelength-dependent devices, (i) UV absorbing devices have stability issue due to high energy of incident light. (ii) In visible-absorbing devices, background illumination randomly fills charge traps, uncontrollably altering synaptic weights and causing noise interference. (iii) In IR devices, their narrow bandgaps promote thermally activated and random trap/de-trap dynamics, which severely degrade synaptic memory retention. Methodologically, (iv) interface trap-based devices have difficulty with precise trap density regulation due to various trap origins such as vacancies, impurities, and surface adsorbates.^{15,177,178} (v) Heterostructure-based designs have structural complexity from bandgap alignment and interface quality. (vi) Nanostructure-based devices have high surface-to-volume ratios, amplifying environmental sensitivity to cause uncontrolled fluctuations in surface trap density and severe device-to-device variability. (vii) Doping-based devices have dopant diffusion and ionic migration issues, causing the spatial distribution of traps to dynamically fluctuate over time, disrupting stability. (viii) Floating-gate-based devices have parasitic charge leakage through the tunnelling layer, causing uncontrolled de-trapping to lead to unstable synaptic weight retention. Despite these limitations, the strategic utilization of charge traps to induce photosynaptic functionality still holds significant promise. Charge trapping provides an intrinsic mechanism for analog memory formation, enabling gradual conductance modulation that closely resembles biological synaptic plasticity. Moreover, trap-assisted dynamics allow diverse temporal responses such as short-term plasticity, long-term memory, and adaptive photoresponse, which are essential for neuromorphic vision systems. By carefully engineering trap energetics, spatial distribution, and interfacial environments through advanced material synthesis and device architectures, it becomes possible to transform charge traps from unpredictable defects into controllable functional elements. In this point of view, continued efforts in trap engineering, interface control, and device integration are expected to offer new opportunities for highly efficient, adaptive, and intelligent photosynaptic devices.

By comparing diverse trap generation and control strategies, this work provides a unified perspective on the physical mechanisms underlying trap-enabled neuromorphic behavior. These studies revisit the growing role of charge traps as a versatile platform for multifunctional optoelectronic synapses and their potential relevance to future neuromorphic hardware. Continued advances in trap engineering, material design, and device architectures will further transform charge traps from unwanted defects into controllable functional elements for next-generation intelligent optoelectronic systems.

Author contributions

S. K. (Seungme Kang) and S. K. (Suhyeon Kim) contributed equally to this work. S. K. (Seungme Kang) and S. K. (Suhyeon

Kim): conceptualization, investigation, visualization, writing – original draft. B. H. L.: investigation, writing – original draft, writing – review & editing. S. N., H.-S. K. and H. Y.: funding acquisition, supervision, project administration, writing – review & editing.

Conflicts of interest

There are no conflicts to declare.

Data availability

This paper is a review article, and all data and figures referenced have been previously published.

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Notes and references

- 1 S. Morab, M. M. Sundaram and A. Pivrikas, *Materials*, 2023, **16**, 4691.
- 2 Y. Jeong, H. Kim, J. Oh, S.-Y. Choi and H. Park, *J. Electron. Mater.*, 2023, **52**, 3914–3920.
- 3 S. Kim, H. Yoo and J. Choi, *Sensors*, 2023, **23**, 2265.
- 4 X. Ma, Y.-Y. Liu, L. Zeng, J. Chen, R. Wang, L.-W. Wang, Y. Wu and X. Jiang, *ACS Appl. Mater. Interfaces*, 2021, **14**, 2185–2193.
- 5 D. Zhang, C. Liu, K. Zhang, Y. Jia, W. Zhong, W. Qiu, Y. Li, T. Heumüller, K. Forberich and V. M. Le Corre, *Energy Environ. Sci.*, 2023, **16**, 5339–5349.
- 6 H. F. Iqbal, Q. Ai, K. J. Thorley, H. Chen, I. McCulloch, C. Risko, J. E. Anthony and O. D. Jurchescu, *Nat. Commun.*, 2021, **12**, 2352.
- 7 T. Yanase, F. Uehara, I. Naito, T. Nagahama and T. Shimada, *ACS Appl. Nano Mater.*, 2020, **3**, 10462–10469.
- 8 J. Li, A. Babuji, L. Fijahi, A. M. James, R. Resel, T. Salzillo, R. Pfattner, C. Ocal, E. Barrena and M. Mas-Torrent, *ACS Appl. Mater. Interfaces*, 2023, **15**, 5521–5528.
- 9 B. Mikake, T. Kobayashi, H. Mizobata, M. Nozaki, T. Shimura and H. Watanabe, *Appl. Phys. Express*, 2023, **16**, 031004.



- 10 T. Fan, N. Tang, J. Wei, S. Zhang, Z. Sun, G. Li, J. Jiang, L. Fu, Y. Zhang and Y. Yuan, *Micro Nanostruct.*, 2023, **176**, 207525.
- 11 H.-W. Lee, M. Kim, J. H. Jun, U. Choi and B. H. Lee, *Nanomaterials*, 2025, **15**, 1484.
- 12 J. Park, D. Gil, S. J. Park, J. W. Ahn, M. Choi, P. Lang, J. Jang, D.-K. Kim and J.-H. Bae, *Materials*, 2025, **18**, 5142.
- 13 S. Park, S. H. Kim, H. Lee and K. Cho, *npj Flexible Electron.*, 2024, **8**, 71.
- 14 H. Kim, S.-M. Yoo, B. Ding, H. Kanda, N. Shibayama, M. A. Syzgantseva, F. F. Tirani, P. Schouwink, H. J. Yun and B. Son, *Nat. Commun.*, 2024, **15**, 5632.
- 15 J.-M. Park, S. Jang, M. Song, K.-S. An, Y. Kang, J. Kim and H.-S. Kim, *Commun. Mater.*, 2025, **6**, 280.
- 16 J.-M. Park, H. Lee, G. Lee, S. C. Jang, Y. H. Chang, H. Hong, K.-B. Chung, K. J. Lee, D. H. Kim and H.-S. Kim, *ACS Appl. Mater. Interfaces*, 2022, **15**, 1525–1534.
- 17 J. B. Ko, S.-I. Cho and S.-H. K. Park, *ACS Appl. Mater. Interfaces*, 2023, **15**, 47799–47809.
- 18 L. Cheng, M. Liu, C. Huang, G. K. Mavlonov, S. Isamov, J. Li and J. Zhang, *J. Phys. D: Appl. Phys.*, 2025, **59**, 015102.
- 19 J. H. Cho, J. Y. Go, T. T. Bui, S. Mun, Y. Kim, K. Ahn, Y. Y. Noh and M. G. Kim, *Adv. Electron. Mater.*, 2023, **9**, 2201014.
- 20 A. K. Rai, A. A. Shah, J. Kumar, S. Chattaraj, A. B. Dar, U. Patbhaje and M. Shrivastava, *ACS Nano*, 2024, **18**, 6215–6228.
- 21 Z. Li, B. Li, X. Wu, S. A. Sheppard, S. Zhang, D. Gao, N. J. Long and Z. Zhu, *Science*, 2022, **376**, 416–420.
- 22 H. Shen, J. Ren, J. Li, Y. Chen, S. Lan, J. Wang, H. Wang and D. Li, *ACS Appl. Mater. Interfaces*, 2020, **12**, 58428–58434.
- 23 K. Jeong, D. y Shin, J. M. Park, D. J. Yi, H. Hong, H. S. Kim and K. B. Chung, *Adv. Sci.*, 2025, **12**, 2407923.
- 24 S. C. Jang, G. Lee, I. Park, B. Noh, J.-M. Park, J. Lee, K. J. Lee and H.-S. Kim, *J. Mater. Chem. C*, 2025, **13**, 6614–6623.
- 25 S. H. Song, J. H. Song, J. Park, H. Yoo and E. K. Lee, *J. Mater. Chem. C*, 2025, **13**, 16657–16666.
- 26 G. Woo, D. H. Lee, Y. Heo, E. Kim, S. On, T. Kim and H. Yoo, *Adv. Mater.*, 2022, **34**, 2107364.
- 27 X. Zhang, L. Xu, R. Liang, S. Zong, J. Li, Z. Zhu, S. Luo, Z. Song and X. Liu, *IEEE Trans. Electron Devices*, 2024, **71**, 3015–3019.
- 28 H. Chen, S. Zheng, S. Du, Y. Jing, J. Sun and X. Liu, *Appl. Surf. Sci.*, 2025, 163557.
- 29 X. Song, J. Xu, L. Liu, Y. Deng, P.-T. Lai and W.-M. Tang, *Nanotechnology*, 2020, **31**, 135206.
- 30 K.-Y. Chen, C.-C. Yang, C.-Y. Huang and Y.-K. Su, *RSC Adv.*, 2020, **10**, 9902–9906.
- 31 J. H. Min, S. C. Jang, K. J. Kim, Y. S. Rim and H.-S. Kim, *Mater. Today Electron.*, 2025, 100178.
- 32 G. Lee, S. C. Jang, J. H. Lee, J. M. Park, B. Noh, H. Choi, H. Kweon, D. H. Kim, H. Y. Kim and H. S. Kim, *Adv. Funct. Mater.*, 2024, **34**, 2405530.
- 33 H. Zhao, G. Lin, P. Cui, J. Zhang and Y. Zeng, *Phys. Status Solidi A*, 2022, **219**, 2100760.
- 34 H. Y. Kim, S.-I. Cho, D. Y. Shin, K.-B. Chung, S.-H. K. Park and J. B. Ko, *J. Alloys Compd.*, 2025, **1020**, 179353.
- 35 S. Aktas and M. Caglar, *Mater. Sci. Eng., B*, 2024, **308**, 117587.
- 36 S. Li, Z. Yin, Y. Li, X. Dong, T. Luo, M. Xi, L. Bai, X. Cao, X. Liang and Y. Cao, *Carbon*, 2025, **237**, 120154.
- 37 K. Ito, K. Tomita, D. Kikuta, M. Horita and T. Narita, *J. Appl. Phys.*, 2021, **129**, 084502.
- 38 E. Brzozowski, M. Kaminski, A. Taube, O. Sadowski, K. Krol and M. Guziewicz, *Materials*, 2023, **16**, 4381.
- 39 S. C. Jang, J. Shim, H. Jang, Y. Lee, S. Biswas, J. Park, H. Shin, H. Kim, S. Kim and H.-S. Kim, *J. Inf. Disp.*, 2025, **26**, 341–356.
- 40 Q. Tang, X. Chen, J. Wan, H. Wu and C. Liu, *IEEE Trans. Electron Devices*, 2020, **67**, 3129–3134.
- 41 J. P. Braga, C. A. Amorim, G. R. De Lima, G. Gozzi and L. Fugikawa-Santos, *Mater. Sci. Semicond. Process.*, 2022, **151**, 106984.
- 42 H. Shin, Y. Han, M. Kim, J. Y. Park, W. Shin, Y.-J. Kim, H.-K. Lee, C.-H. Kim and H. Yoo, *ACS Appl. Electron. Mater.*, 2025, **7**, 10805–10814.
- 43 Y. Han, S. Lee, E. K. Lee, H. Yoo and B. C. Jang, *Adv. Sci.*, 2024, **11**, 2309221.
- 44 J. Seo, C.-H. Kim and H. Yoo, *IEEE Trans. Electron Devices*, 2024, **71**, 3020–3025.
- 45 Y. Jeon, Y. J. Shin, Y. Jeon and H. Yoo, *Org. Electron.*, 2023, **122**, 106914.
- 46 Y. Han, D. H. Lee, E.-S. Cho, S. J. Kwon and H. Yoo, *Micromachines*, 2023, **14**, 1394.
- 47 D. H. Kim, H. J. Choi, D. Kim, C. S. Mun and G.-T. Kim, *ACS Appl. Nano Mater.*, 2025, **8**, 4729–4740.
- 48 C. Li, Q. Wu, A. Liang, G. Chen, S. Chen, Z. Su and G. Liang, *Surf. Interfaces*, 2024, **52**, 104853.
- 49 K. Ko, T. Park, H. Yoo and J. Hur, *J. Alloys Compd.*, 2023, **969**, 172472.
- 50 E. Park, T. Park, H. Yoo and J. Hur, *J. Alloys Compd.*, 2022, **918**, 165502.
- 51 T. Park, D. Kim, B. Shin, J. Hur and H. Yoo, *Adv. Opt. Mater.*, 2022, **10**, 2102542.
- 52 G. Woo, E. K. Lee, H. Yoo and T. Kim, *ACS Appl. Mater. Interfaces*, 2021, **13**, 25072–25081.
- 53 A. Choudhury, R. K. Gupta, R. Garai and P. K. Iyer, *Adv. Mater. Interfaces*, 2021, **8**, 2100574.
- 54 A. Liang, Y. Gao, R. Asadpour, Z. Wei, B. P. Finkenauer, L. Jin, J. Yang, K. Wang, K. Chen and P. Liao, *J. Am. Chem. Soc.*, 2021, **143**, 15215–15223.
- 55 E. K. Lee, H. Abdullah, F. Torricelli, D. H. Lee, J. K. Ko, H. H. Kim, H. Yoo and J. H. Oh, *ACS Nano*, 2021, **15**, 17769–17779.
- 56 A. Ali, A. Tooshil, M. R. M. Arnob, W.-S. Lee, J. Lee, R. Choi, J. Jang and J.-H. Lee, *ACS Appl. Electron. Mater.*, 2025, **7**, 9212–9218.
- 57 S. Park, S.-I. Cho, H. Y. Kim, S.-H. K. Park and J. B. Ko, *ACS Appl. Mater. Interfaces*, 2025, **17**, 66801–66814.
- 58 Y. Wu, F. Yuan, S. Yang, E. Li, W. Wang, Y. Liu, X. Yang, J. Wen, L. Hua and Y. Yang, *Sci. Adv.*, 2025, **11**, eadv4138.



- 59 Y. Zhao, C. Li, J. Jiang, B. Wang and L. Shen, *Small*, 2020, **16**, 2001534.
- 60 C. Tan, S. Yin, J. Chen, Y. Lu, W. Wei, H. Du, K. Liu, F. Wang, T. Zhai and L. Li, *ACS Nano*, 2021, **15**, 8328–8337.
- 61 M. Chen, Z. Zhang, Z. Lv, R. Zhan, H. Chen, H. Jiang and J. Chen, *ACS Appl. Nano Mater.*, 2022, **5**, 351–360.
- 62 Z. Li, Z. Chen, Z. Shi, G. Zou, L. Chu, X.-K. Chen, C. Zhang, S. K. So and H.-L. Yip, *Nat. Commun.*, 2023, **14**, 6441.
- 63 M. He, Z. Xu, C. Zhao, Y. Gao, K. Ke, N. Liu, X. Yao, F. Kang, Y. Shen and L. Lin, *Adv. Funct. Mater.*, 2023, **33**, 2300282.
- 64 H. Lee, B. Moon, S. Y. Son, T. Park, B. Kang and K. Cho, *ACS Appl. Mater. Interfaces*, 2021, **13**, 16722–16731.
- 65 N. Zagni, A. Chini, F. M. Puglisi, P. Pavan and G. Verzellesi, *Phys. Status Solidi A*, 2020, **217**, 1900762.
- 66 S. Lee, T. Park, J. Hur and H. Yoo, *ACS Photonics*, 2022, **9**, 4005–4016.
- 67 S. Kumar, A. Salunke and S. Pradhan, *ACS Appl. Opt. Mater.*, 2024, **2**, 128–138.
- 68 I. S. Lee, J. W. Na, K. Kwak, J. B. An and H. J. Kim, *Appl. Surf. Sci. Adv.*, 2025, **29**, 100839.
- 69 R. Pendurthi, D. Jayachandran, A. Kozhakhmetov, N. Trainor, J. A. Robinson, J. M. Redwing and S. Das, *Small*, 2022, **18**, 2202590.
- 70 S. Chen, E. Li, R. Yu, H. Yang, Y. Yan, Y. Hu, H. Chen and T. Guo, *J. Mater. Chem. C*, 2021, **9**, 9972–9981.
- 71 D. Liu, H. Yu and Y. Chai, *Adv. Intell. Syst.*, 2021, **3**, 2000150.
- 72 C. Pan, C.-Y. Wang, S.-J. Liang, Y. Wang, T. Cao, P. Wang, C. Wang, S. Wang, B. Cheng and A. Gao, *Nat. Electron.*, 2020, **3**, 383–390.
- 73 J. Li, P. Dwivedi, K. S. Kumar, T. Roy, K. E. Crawford and J. Thomas, *Adv. Electron. Mater.*, 2021, **7**, 2000535.
- 74 S. M. Lee, J.-M. Park, S. Ahn, S. C. Jang, H. Kim and H.-S. Kim, *ACS Appl. Electron. Mater.*, 2024, **6**, 5371–5378.
- 75 J.-M. Park, H. Hwang, M. S. Song, S. C. Jang, J. H. Kim, H. Kim and H.-S. Kim, *ACS Appl. Mater. Interfaces*, 2023, **15**, 47229–47237.
- 76 W. Choi, J. Shin, Y. J. Kim, J. Hur, B. C. Jang and H. Yoo, *Adv. Mater.*, 2024, **36**, 2312831.
- 77 D. Ielmini and S. Ambrogio, *Nanotechnology*, 2019, **31**, 092001.
- 78 S. Kim, Y. Jeon, E. K. Lee, Y. J. Kim, C.-H. Kim and H. Yoo, *Nano Lett.*, 2024, **24**, 2025–2032.
- 79 Y. Jeon, J. Seo and H. Yoo, *J. Alloys Compd.*, 2023, **938**, 168687.
- 80 B. Rajendran, A. Sebastian, M. Schmuker, N. Srinivasa and E. Eleftheriou, *IEEE Signal Process. Mag.*, 2019, **36**, 97–110.
- 81 V. N. Balaji, P. B. Srinivas and M. K. Singh, *Mater. Today: Proc.*, 2022, **51**, 850–853.
- 82 Y. Sandamirskaya, M. Kaboli, J. Conradt and T. Celikel, *Sci. Rob.*, 2022, **7**, eabl8419.
- 83 D. Kim, H. Bang, H. W. Baac, J. Lee, P. L. Truong, B. H. Jeong, T. Appadurai, K. K. Park, D. Heo and V. B. Nam, *Adv. Funct. Mater.*, 2023, **33**, 2213064.
- 84 S. Hong, S. H. Choi, J. Park, H. Yoo, J. Y. Oh, E. Hwang, D. H. Yoon and S. Kim, *ACS Nano*, 2020, **14**, 9796–9806.
- 85 Y. Kim, C. W. Lee and H. W. Jang, *J. Electron. Mater.*, 2025, **54**, 3609–3650.
- 86 S. Kang, S. Sohn, H. Kim, H. J. Yun, B. C. Jang and H. Yoo, *ACS Appl. Mater. Interfaces*, 2024, **16**, 11758–11766.
- 87 J. Kim, S. Song, J. M. Lee, S. Nam, J. Kim, D. K. Hwang, S. K. Park and Y. H. Kim, *Small*, 2023, **19**, 2301186.
- 88 Q. Lv, J. Shi, C. Chen, H. Sun, H. Chen, X. Li, J. Chen, H. Lin and Z. Chen, *ACS Appl. Mater. Interfaces*, 2025, **17**, 47302–47313.
- 89 S. H. Chung, J. H. Song, W. W. Lee, H. Yoo, H.-R. Lim and E. K. Lee, *Synth. Met.*, 2025, 117919.
- 90 S. Park, S. Kim, S. Kim, K. Park, D. Ryu and S. Kim, *Adv. Opt. Mater.*, 2025, 2500634.
- 91 J. Park, Y. Jang, J. Lee, S. An, J. Mok and S. Y. Lee, *Adv. Electron. Mater.*, 2023, **9**, 2201306.
- 92 J. Shin, S. Kim, B. C. Jang and H. Yoo, *Dyes Pigm.*, 2023, **208**, 110882.
- 93 P. A. Hind, P. Kumar, U. Goutam and B. Rajendra, *Opt. Mater.*, 2024, **153**, 115579.
- 94 H. Jiang, H. Ji, Z. Ma, D. Yang, J. Ma, M. Zhang, X. Li, M. Wang, Y. Li and X. Chen, *Light: Sci. Appl.*, 2024, **13**, 316.
- 95 X. Peng, X. Xu, Y. Wang, Y. Zhao, H. Li, C. Fan and L. Ma, *J. Alloys Compd.*, 2025, 185454.
- 96 H. Guo, J. Guo, Y. Wang, H. Wang, S. Cheng, Z. Wang, Q. Miao and X. Xu, *ACS Appl. Mater. Interfaces*, 2024, **16**, 66948–66960.
- 97 Y. Li, M. Zhao, X. Ma, L. Zhang, S. Zhao, W. Strupinski, X. Zeng, M. Zhang and Y. Hao, *Adv. Funct. Mater.*, 2025, 2423333.
- 98 G. Lee, S. Jeong, H. Kim, Y. J. Kim, S. Oh, J. Choi and H. Yoo, *npj Flexible Electron.*, 2025, **9**, 65.
- 99 H. F. Haneef, A. M. Zeidell and O. D. Jurchescu, *J. Mater. Chem. C*, 2020, **8**, 759–787.
- 100 J. Jia, A. Suko, Y. Shigesato, T. Okajima, K. Inoue and H. Hosomi, *Phys. Rev. Appl.*, 2018, **9**, 014018.
- 101 Y. Huang, K. Wu, Y. Sun, Y. Hu, Z. Wang, L. Yuan, S. Wang, D. Ji, X. Zhang and H. Dong, *Nat. Commun.*, 2024, **15**, 626.
- 102 I. Amit, D. Englander, D. Horvitz, Y. Sasson and Y. Rosenwaks, *Nano Lett.*, 2014, **14**, 6190–6194.
- 103 H. Chen, W. Zhang, M. Li, G. He and X. Guo, *Chem. Rev.*, 2020, **120**, 2879–2949.
- 104 D. Zhao, Y. Shao, S. Zhang, T. Li, B. Chi, Y. Zhu, F. Liu, Y. Liang and S. Du, *Electronics*, 2025, **14**, 2982.
- 105 A. Musiienko, J. Pipek, P. Praus, M. Brynza, E. Belas, B. Dryzhakov, M.-H. Du, M. Ahmadi and R. Grill, *Sci. Adv.*, 2020, **6**, eabb6393.
- 106 V. Volosov, S. Cascino, M. Saggio, A. Imbruglia, F. Di Giovanni, C. Fiegna, E. Sangiorgi and A. Tallarico, *Solid-State Electron.*, 2023, **207**, 108699.
- 107 A. Pacheco-Sanchez, J. N. Ramos Silva, N. Mavredakis, E. Ramírez-García and D. Jiménez, *2023 38th Conference on Design of Circuits and Integrated Systems (DCIS)*, Málaga, Spain, 2023.
- 108 Z. Wang, H. Gao, D. Wu, J. Meng, J. Deng and M. Cui, *Molecules*, 2024, **29**, 2104.
- 109 Y. Li and G. Shen, *Cell Rep. Phys. Sci.*, 2022, **3**, 101037.



- 110 H. Fang and W. Hu, *Adv. Sci.*, 2017, **4**, 1700323.
- 111 M. Planck, *Ann. Phys.*, 1901, **4**, 1.
- 112 M. A. Green, *Sol. Energy Mater. Sol. Cells*, 2008, **92**, 1305–1310.
- 113 T. Tiedje, E. Yablonovitch, G. D. Cody and B. G. Brooks, *IEEE Trans. Electron Devices*, 1984, **31**, 711–716.
- 114 M.-S. Lee, J.-W. Lee, C.-H. Kim, B.-G. Park and J.-H. Lee, *IEEE Trans. Electron Devices*, 2015, **62**, 569–573.
- 115 D. Jeon, S. H. Lee and S.-N. Lee, *Materials*, 2025, **18**, 2931.
- 116 X. Ma, Y. Zhang, P. Tan, X. Feng, Y. Hao, G. Xu, X. Zhao, N. Gao, X. Hou and Q. Hu, *InfoMat*, 2025, e70016.
- 117 W. J. Lee, S. H. Sohn and I. K. Park, *Adv. Opt. Mater.*, 2025, **13**, 2402636.
- 118 C. Xie, C. Li, H. Yu, C. Fu, W. Yang, L. Yang and Z. Huang, *Nano Lett.*, 2025, **25**, 14686–14694.
- 119 Z. Liang, X. Wang, Z. Song, Q. Wang, X. Tang, J. Wu, L. Bu and G. Lu, *ACS Appl. Mater. Interfaces*, 2024, **16**, 65091–65099.
- 120 W. Zhu, J. Sun, Y. Wang, Y. Li, H. Bai, Q. Wang, L. Han, Q. Zhang, H. Wu and C. Song, *Adv. Mater.*, 2024, **36**, 2403624.
- 121 B. H. Jeong, J. Lee, M. Ku, J. Lee, D. Kim, S. Ham, K.-T. Lee, Y.-B. Kim and H. J. Park, *Nano-Micro Lett.*, 2025, **17**, 78.
- 122 Z. Yin, L. Shan, R. Ci, D. Hao, G. Miao, L. Tian, G. Liu and F. Shan, *Appl. Phys. Lett.*, 2025, **126**, 103302.
- 123 L. Chen, W. He, D. Wang, S. Jiao, Y. Han, X. Fan, Z. Shi, Y. Zhang, D. Ling and Y. Bi, *J. Colloid Interface Sci.*, 2025, **689**, 137252.
- 124 Y. Chen, Y. Kang, H. Hao, X. Xie, J. Zeng, T. Xu, C. Li, Y. Tan and L. Fang, *Adv. Funct. Mater.*, 2023, **33**, 2209781.
- 125 J. H. Kim, M. Stolte and F. Würthner, *ACS Nano*, 2022, **16**, 19523–19532.
- 126 H. Wu, Z. Liu, H. Wang, C. Li, X. Gu, R. Guo and L. Dong, *Opt. Lasers Eng.*, 2025, **184**, 108556.
- 127 A. Bessonov, A. Rozanov, R. White, G. Suwito, I. Medina-Salazar, M. Lutfullin, D. Gusev and I. Shikov, *Drones*, 2025, **9**, 553.
- 128 X. Liu, S. Dai, Y. Jin, J. Zhang, Z. Guo, T. Sun, L. Li, P. Guo, H. Gao and H. Liang, *Nat. Commun.*, 2025, **17**, 197.
- 129 H. Gao, X. Jiang, X. Ma, M. Ye, J. Yang, J. Zhang, Y. Gao, T. Li, H. Wang and J. Mei, *Nat. Commun.*, 2025, **16**, 5241.
- 130 S. Shim, S. Kim, D. Lee, H. Kim, M. J. Kwon, S. Y. Cho, W. A. Lestari, J. Seo, D. Yeo and J. Na, *Small*, 2025, 2410892.
- 131 T. Yan, Y. Cai, Y. Wang, J. Yang, S. Li, X. Zhan, F. Wang, R. Cheng, F. Wang and J. He, *Sci. China Inf. Sci.*, 2023, **66**, 160404.
- 132 W. Luan, Z. Zhao, H. Li, Y. Zhai, Z. Lv, K. Zhou, S. Xue, M. Zhang, Y. Yan and Y. Cao, *J. Phys. Chem. Lett.*, 2024, **15**, 8845–8852.
- 133 L. Jiang, B. Wang, F. Ni, W. Xu, X. Wang, L. Zheng and L. Qiu, *ACS Photonics*, 2024, **11**, 3187–3196.
- 134 F.-C. Wu, C.-Y. Chen, Y.-W. Wang, C.-B. You, L.-Y. Wang, J. Ruan, W.-Y. Chou, W.-C. Lai and H.-L. Cheng, *ACS Appl. Mater. Interfaces*, 2024, **16**, 41211–41222.
- 135 M. M. Islam, D. Dev, A. Krishnaprasad, L. Tetard and T. Roy, *Sci. Rep.*, 2020, **10**, 21870.
- 136 L. Hu, J. Yang, J. Wang, P. Cheng, L. O. Chua and F. Zhuge, *Adv. Funct. Mater.*, 2021, **31**, 2005582.
- 137 Y. E. Kim, S. Kang, H. Kim, Y.-J. Kim, S. Oh and H. Yoo, *ACS Appl. Mater. Interfaces*, 2025, **17**, 57379–57391.
- 138 J. Wang, Y. Zhang, D. Xie, Y. Zhang, Y. Li, B. Liu, Q. Han, B. Wu, C. Ge and H. Zheng, *Nano Energy*, 2024, **120**, 109128.
- 139 Y. J. Kim, K.-J. Lee and M. Kim, *ACS Appl. Mater. Interfaces*, 2025, **17**, 53757–53766.
- 140 H.-y. Liu, H. Yang and Y. Zheng, *Phys. Chem. Chem. Phys.*, 2024, **26**, 6228–6234.
- 141 X. Huang, Q. Li, W. Shi, K. Liu, Y. Zhang, Y. Liu, X. Wei, Z. Zhao, Y. Guo and Y. Liu, *Small*, 2021, **17**, 2102820.
- 142 Y. Deng, S. Liu, X. Ma, S. Guo, B. Zhai, Z. Zhang, M. Li, Y. Yu, W. Hu and H. Yang, *Adv. Mater.*, 2024, **36**, 2309940.
- 143 F. Tan, C. Chang, N. Zhang, J. An, M. Liu, X. Zhao, M. Che, Z. Liu, Y. Shi and Y. Li, *Light: Sci. Appl.*, 2025, **14**, 122.
- 144 E. Ercan, C.-C. Hung, G.-S. Li, Y.-F. Yang, Y.-C. Lin and W.-C. Chen, *Nanoscale Horiz.*, 2023, **8**, 632–640.
- 145 Z. Long, Y. Ding, X. Qiu, Y. Zhou, S. Kumar and Z. Fan, *J. Semicond.*, 2023, **44**, 092604.
- 146 S. Xin, Y. Chang, R. Zhou, H. Cong, L. Zheng, Y. Wang, Y. Qin, P. Xu, X. Liu and F. Wang, *J. Mater. Chem. C*, 2023, **11**, 722–729.
- 147 C. Liu, X. Shen, S. Fan, T. Xu, J. Zhang and J. Su, *ACS Appl. Electron. Mater.*, 2023, **5**, 4657–4666.
- 148 G. Lee, Y. E. Kim, H. Kim, H. K. Lee, J. Y. Park, S. Oh and H. Yoo, *Small*, 2025, **21**, 2501997.
- 149 W. Choi, J. S. Yoon, W. W. Lee, G. H. Hong, H. Kim, S. Oh, Y. Tea Chun and H. Yoo, *Small*, 2025, e06440.
- 150 X. Liu, D. Wang, W. Chen, Y. Kang, S. Fang, Y. Luo, D. Luo, H. Yu, H. Zhang and K. Liang, *Nat. Commun.*, 2024, **15**, 7671.
- 151 B. Mirka, D. Fong, N. A. Rice, O. A. Melville, A. Adronov and B. H. Lessard, *Chem. Mater.*, 2019, **31**, 2863–2872.
- 152 N. A. Rice, W. J. Bodnaryk, B. Mirka, O. A. Melville, A. Adronov and B. H. Lessard, *Adv. Electron. Mater.*, 2019, **5**, 1800539.
- 153 B. Mirka, N. A. Rice, P. Williams, M. N. Tousignant, N. T. Boileau, W. J. Bodnaryk, D. Fong, A. Adronov and B. H. Lessard, *ACS Nano*, 2021, **15**, 8252–8266.
- 154 M. Ourabi, S. Garg, B. Mirka, R. Ewenike, M. N. Tousignant, M. Ranne, A. Adronov and B. H. Lessard, *ACS Appl. Nano Mater.*, 2023, **6**, 11242–11251.
- 155 N. J. Dallaire, B. Mirka, J. G. Manion, W. J. Bodnaryk, D. Fong, A. Adronov, K. Hinzer and B. H. Lessard, *J. Mater. Chem. C*, 2023, **11**, 9161–9171.
- 156 M. N. Tousignant, N. A. Rice, J. Niskanen, C. M. Richard, D. Ritaine, A. Adronov and B. H. Lessard, *Adv. Electron. Mater.*, 2021, **7**, 2100700.
- 157 M. N. Tousignant, B. Ronnasi, V. Tischler and B. H. Lessard, *Adv. Mater. Interfaces*, 2023, **10**, 2300079.
- 158 M. N. Tousignant, Z. S. Lin, J. Brusso and B. H. Lessard, *ACS Appl. Mater. Interfaces*, 2023, **15**, 3680–3688.



- 159 B. Ronnasi, M. N. Tousignant and B. H. Lessard, *J. Mater. Chem. C*, 2023, **11**, 3197–3205.
- 160 B. Ronnasi, S. P. McKillop, M. Ourabi, M. Perry, H. A. Sharp and B. H. Lessard, *ACS Appl. Mater. Interfaces*, 2024, **16**, 65425–65435.
- 161 M. N. Tousignant, M. Ourabi, J. Niskanen, B. Mirka, W. J. Bodnaryk, A. Adronov and B. H. Lessard, *Flexible Printed Electron.*, 2022, **7**, 034004.
- 162 T. Mulia, E. Ercan, M. Mumtaz, Y.-C. Lin, R. Borsali and W.-C. Chen, *Carbohydr. Polym.*, 2024, **344**, 122476.
- 163 E. Ercan, Y. C. Lin, W. C. Yang and W. C. Chen, *Adv. Funct. Mater.*, 2022, **32**, 2107925.
- 164 Y.-W. Song, Y.-H. Chang, J. Choi, M.-K. Song, J. H. Yoon, S. Lee, S.-Y. Jung, W. Ham, J.-M. Park and H.-S. Kim, *Appl. Surf. Sci.*, 2023, **631**, 157356.
- 165 Y. Hu, Y. Lin, X. Zhang, Y. Zhao, L. Li, Y. Zhang, H. Lei and Y. Pan, *Nanoscale Horiz.*, 2025, **10**, 1354–1364.
- 166 J. Jiang, W. Xu, Z. Sun, L. Fu, S. Zhang, B. Qin, T. Fan, G. Li, S. Chen and S. Yang, *Small*, 2024, **20**, 2306068.
- 167 J. Li, K. Chen, C. Wu, F. Wu, S. Li, Z. Wu, W. Tang, Z. Fang and D. Guo, *Appl. Phys. Lett.*, 2025, **126**, 222104.
- 168 M. Ma, C. Huang, M. Yang, D. He, Y. Pei, Y. Kang, W. Li, C. Lei and X. Xiao, *Small*, 2024, **20**, 2406402.
- 169 K. Chen, H. Hu, I. Song, H. B. Gobeze, W.-J. Lee, A. Abtahi, K. S. Schanze and J. Mei, *Nat. Photonics*, 2023, **17**, 629–637.
- 170 B. Pei, X. Han, Y. Wang and J. Liu, *Small*, 2025, 2500184.
- 171 J. Park, Y. Yun, S. Bae, Y. Jang, S. Shin and S. Y. Lee, *Adv. Sci.*, 2025, **12**, 2500568.
- 172 X. Hu, R. Hao, L. Luo, Y. Zhang, Y. Li and Z. Zhang, *Laser Photonics Rev.*, 2024, **18**, 2400319.
- 173 Y. Zeng, W. Lv, Z. Hou, W. Huang, Z. Yu, Z. Han, R. Zhan, T. Zeng, Y. Luo and Y. Lin, *Adv. Sci.*, 2025, **12**, e10063.
- 174 J. Zha, Y. Xia, S. Shi, H. Huang, S. Li, C. Qian, H. Wang, P. Yang, Z. Zhang and Y. Meng, *Adv. Mater.*, 2024, **36**, 2308502.
- 175 S. Kang, J. Park, J. Hong, J. Park, J. Lee, H. Kim, W. Shin, E. Bestelink, R. A. Sporea and S. Oh, *Adv. Funct. Mater.*, 2025, e25060.
- 176 B. J. Moon, Y.-S. Song, D. Son, H. Y. Yang, S. Bae, S.-K. Lee, S. H. Lee and T.-W. Kim, *Small Sci.*, 2023, **3**, 2300068.
- 177 L. H. de Lima, W. S. E. Silva, I. A. S. Prior, R. Landers and A. de Siervo, *J. Phys. Chem. C*, 2023, **127**, 8795–8802.
- 178 J. Byeon, J. Eom, T. Kim, J. Lim, M. Jung, Y. Lim, H. Park, J. Hong, S. Pak and S. Cha, *ACS Appl. Electron. Mater.*, 2024, **6**, 1763–1769.

