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Electrically erasable multi-level charge trapping memory with metal nanoparticle engineering for organic synaptic transistors†

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The development of wearable neuromorphic electronics is critical for advancing human–machine interfaces, personalized healthcare, and brain-inspired computing. Organic synaptic transistors (OSTs) have emerged as promising candidates due to their biocompatibility, mechanical flexibility, and tunable optoelectronic properties by molecular design. However, achieving efficient electrical erasing in charge-trapping-based OSTs remains challenging, particularly for oligomeric semiconductors with relatively large bandgaps. Here, we introduce a novel approach to enhance the vertical electric field in OSTs by incorporating metal nanoparticles (NPs) on top of a wide-bandgap organic semiconductor, significantly improving erase operations. The proposed device demonstrates an enlarged memory window and successful realization of 30 distinct potentiation and depression states, overcoming the write-once-read-many limitation observed in conventional charge-trapping devices. Furthermore, neural network simulations employing our multi-level memory states achieved an 87.3% classification accuracy on hand-written digit dataset, comparable to software-based systems. This work provides a simple yet efficient strategy for engineering neuromorphic transistors, paving the way for next-generation artificial intelligence hardware.

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1. Introduction

The growing demand for human–machine interfaces, personalized healthcare, and brain-inspired computing highlights the critical need for wearable neuromorphic platforms that seamlessly integrate with the human body.[1–8] These flexible neuromorphic electronics address the fundamental limitations of conventional electronic systems by enabling real-time health monitoring, personalized information processing, and interactive communication, while mimicking the brain's neural processing with ultralow power consumption (Fig. 1a).[9–15] Among the various materials used in flexible neuromorphic electronics, organic artificial synapses have garnered significant attention due to their tunable optical and electrical properties through molecular design, scalability, low-cost fabrication, biocompatibility, and mechanical flexibility.[16–28] In particular, organic synaptic transistors (OSTs) based on charge-trapping mechanisms have been extensively studied for their advantages, including the ability to achieve multiple memory states by modulating the trapped charge density and their excellent data retention characteristics.[29–33]

Among the diverse organic semiconductors employed in charge-trapping-based organic synapses, oligomeric semiconductors offer excellent crystallinity and high uniformity due to their compatibility with vacuum deposition processes, which prevents damage to underlying layers.[34–36] However, most oligomeric semiconductors possess a relatively large bandgap of approximately 2.0 eV, which has been reported to hinder electrical erase operations in charge-trapping devices.[37–39] During the erase process, the channel region remains in a depleted state due to the high minority charge injection barrier, resulting in only a negligible vertical electric field from the semiconductor to the gate, ultimately preventing effective electrical erase operations (Fig. 1(b)). This phenomenon is also observed in large-bandgap inorganic semiconductors such as GaN, SiC, and emerging metal-oxide semiconductors like In–Ga–Zn oxide. To overcome this limitation, strategies such as incorporating high-work-function materials as source/drain (S/D)

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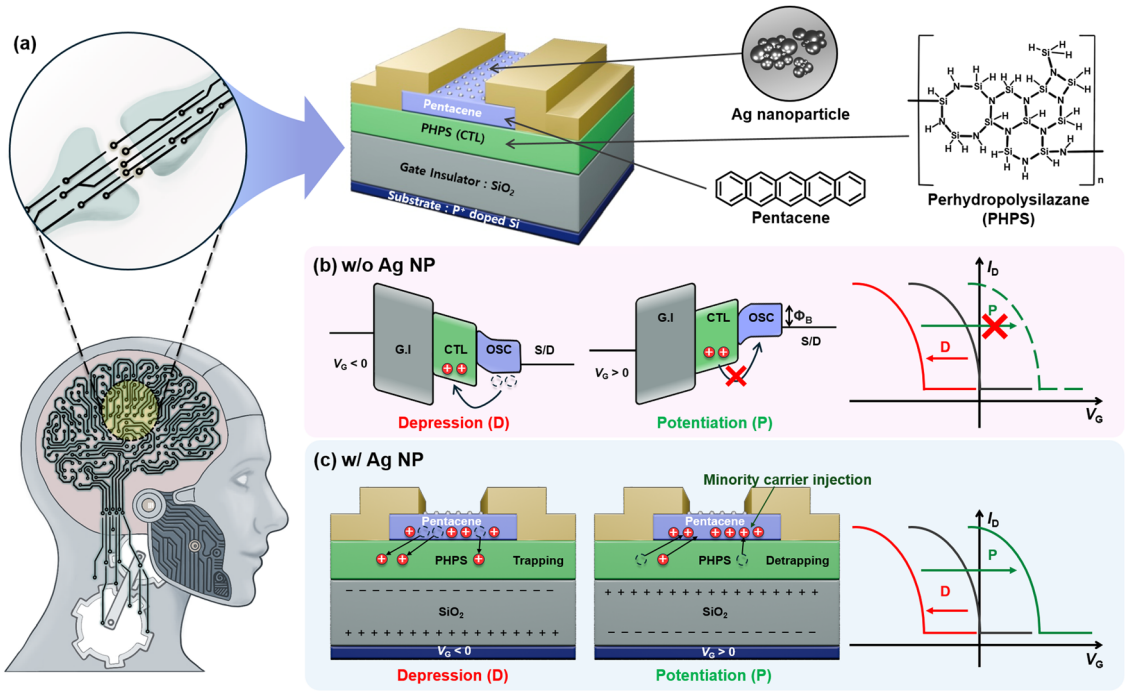

Fig. 1 (a) Schematic of charge-trapping-based OSTs with metal NPs for electrically writable (depression; *D*) and erasable (potentiation; *P*) multi-memory states in neuromorphic computing. (b) Challenges in electrical erase operations (*P*) of charge-trapping-based OSTs with oligomeric semiconductors. (c) Realization of electrically writable (*D*) and erasable (*P*) multi-memory states by introducing metal NPs on top of the OSC layer.

electrodes and scaling down the channel length to 20 nm to enhance the vertical electric field strength have been proposed in inorganic memory devices, enabling erase performance.[39] As a solution to this challenge in artificial synaptic devices, optical erasing operations have been widely explored.[38–40] However, these approaches introduce complex driving schemes that rely on a combination of electrical writing and optical erasing, device instability, or costly and intricate fabrication processes. These limitations hinder the practical implementation of neuromorphic electronics in real-world applications.

In this work, we propose a novel strategy for organic synaptic transistors that addresses this long-standing challenge without relying on optical assistance or complex fabrication techniques. Specifically, we introduce a vertical field-engineering strategy by incorporating metal nanoparticles (NPs) on top of a wide-bandgap oligomeric semiconductor (Fig. 1). The embedded NPs locally enhance the vertical electric field across the channel during erase operations, enabling fully electrical control of both potentiation and depression in charge-trapping-based OSTs—a capability rarely demonstrated in previous oligomer-based synaptic devices. Without this enhancement, the depleted channel region resulted in only a negligible electric field applied to charge trap layer (CTL), preventing effective electrical erase operations. Importantly, this strategy provides a generalizable and scalable solution to achieving fully electrical weight modulation in a broad range of organic semiconductors with large bandgaps.

As a result, the proposed NP-embedded OST exhibits a significantly enlarged memory window of up to 64 V (depending on NP thickness) and demonstrates 30 distinct, electrically controlled potentiation and depression states. In contrast, reference devices without NPs operated only in a write-once-read-many (WORM) mode, lacking electrical erasability. The multi-level conductance states of our device were successfully utilized as synaptic weights in a neural network for handwritten digit classification using the MNIST dataset, achieving a recognition accuracy of 87.3%, approaching the performance of an ideal software-based system.

2. Methods

For both the devices with and without Ag NPs, p-type doped silicon substrates were oxidized to form a 200 nm thick SiO_2 layer, which served as the gate insulator. To fabricate the CTL, an 18 wt% solution of perhydropolysilazane (PHPS) was diluted in dibutyl ether, and a 2 wt% PHPS solution was used. The solution was spin-coated at 500 rpm for 5 s, followed by 3000 rpm for 40 s, and subsequently annealed at 100 °C for 2 h.[40,41] The oligomeric semiconductor (OSC), pentacene, was thermally vacuum-deposited at a rate of 0.5 Å s^{-1} to form a 50 nm thick semiconductor layer. Next, Au was thermally vacuum-deposited at a rate of 1 Å s^{-1} to create a 50 nm thick source/drain (S/D) electrode. The channel length and width of the devices were 200 μm and 1 mm, respectively. For the OSTs incorporating Ag NPs, Ag NPs with thicknesses ranging from 2 nm to 15 nm were deposited *via* thermal vacuum deposition at a rate of 1 Å s^{-1} to induce a sufficiently strong electric field throughout the entire CTL (Fig. 1d). The electrical characteristics of the devices were

measured under ambient conditions using an HP4155A and 4200A-SCS semiconductor parameter analyzer. A scanning electron microscope (SU8230, AMETEK) was used to analyze the surface morphology of the thermally deposited Ag NPs. Additionally, two-dimensional (2D) finite-element numerical simulation was performed using a commercially available software package (ATLAS, Silvaco). This simulator self-consistently solves the drift-diffusion and Poisson's equations in a user-defined 2D mesh that is designed to mimic the cross-section of the actual device. In this study, we used this method to specifically quantify the electric potential distribution in the channel and the CTL regions, which is known to strongly affect the gate programming and erasing efficiency of the memory transistors.

3. Results and discussion

Firstly, scanning electron microscope (SEM) was used to observe surface of the pentacene and the formation of Ag NPs on top of pentacene, an OSC. Fig. S1a and b (ESI†) show the SEM images of the surface morphology of pentacene and 5-nm-thick Ag NPs deposited on pentacene, respectively. Fig. S1a (ESI†) displays typical pentacene grains without the formation of Ag NPs, while Fig. S1b (ESI†) shows the surface of smaller Ag NP grains deposited on pentacene, with a grain size similar to that of the pentacene in Fig. S1a (ESI†).[42] From this, we confirmed the successful formation of Ag NPs on the pentacene layer through the thermal evaporation of 5-nm thick Ag.

To investigate the effect of Ag NPs on the electric field distribution in OSTs, we conducted numerical simulations of the electrical potential distribution (Fig. 2 and Fig. S2, ESI†). The simulation results, shown in Fig. 2a–d, illustrate the potential distribution without and with Ag NPs during the write (Fig. 2a and b) and erase operations (Fig. 2c and d). The simulations were performed on a portion of the source electrode and in a 200-nm-wide region near the source electrodes (green dotted box in Fig. S2, ESI†). Specifically, for the device with Ag NPs, the simulation assumed that both the size and

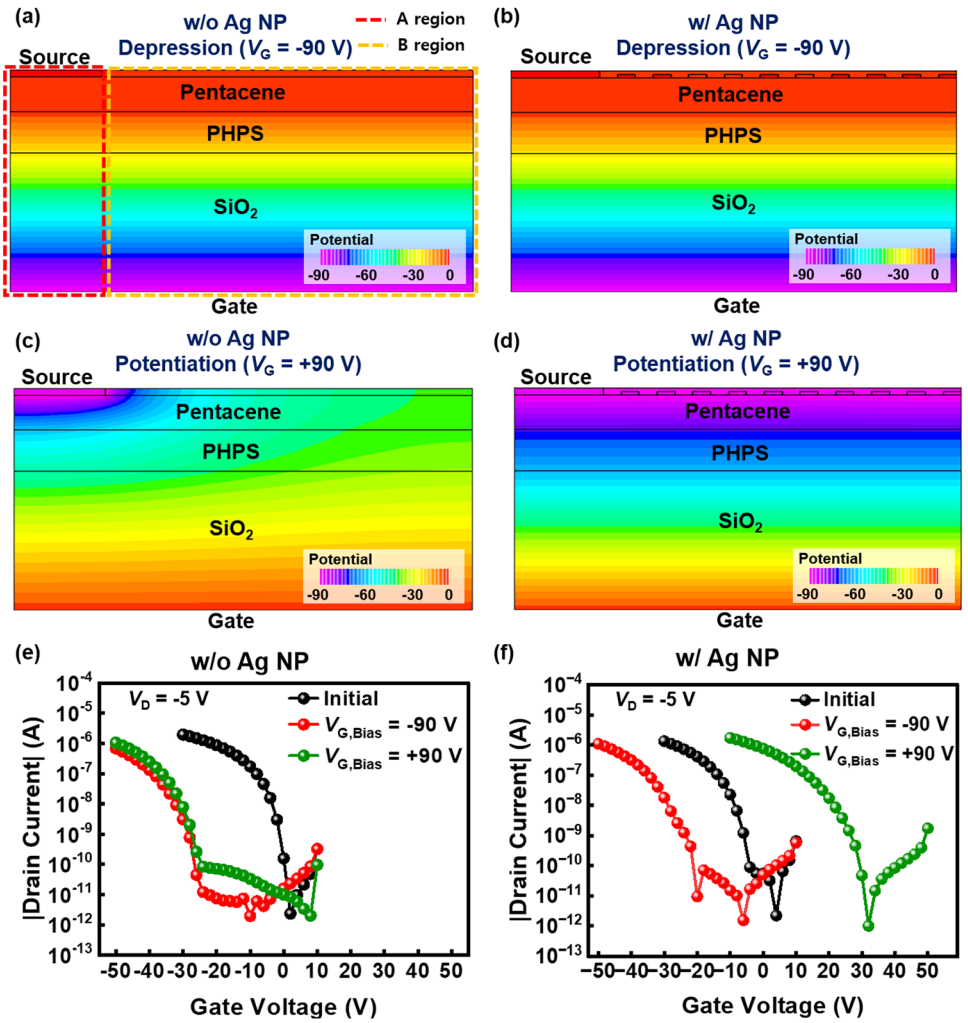

Fig. 2 Simulated potential distribution results without and with Ag NPs during the (a) and (b) write (depression) and (c), (d) erase (potentiation) operations. Transfer curves of the devices (e) without and (f) with Ag NPs after writing (red line) and erasing (green line), with the black lines representing the initial transfer curves.

spacing of the metal nanoparticles were on the order of 10 nm. In our device structure, where a 5-nm-thick Ag nanoparticle layer was deposited on a relatively thick (50-nm) pentacene OSC layer, the influence of Ag diffusion is expected to be negligible. Therefore, the effect of Ag diffusion was not considered in our numerical simulations. In both cases, with and without Ag NPs, the region where the S/D and gate electrode overlap is designated as region A (red dotted line in Fig. 2 and Fig. S2, ESI†), while the region where the gate electrode overlaps the channel without overlapping the S/D is referred to as region B (orange dotted line in Fig. 2 and Fig. S2, ESI†). Fig. 2a and b show the electric potential distribution of OSTs without and with Ag NPs, respectively, during the write operation at a gate voltage of −90 V. Under this condition (V_G = −90 V), holes accumulate readily at the OSC/insulator interface in both devices, increasing the conductivity of the OSC layer. Consequently, the potential distributions in regions A and B remain similar, ensuring the application of a sufficient vertical electric field to the CTL, which facilitates hole trapping. It should be noted that the PHPS CTL possesses a high density of both electron and hole trap sites, allowing the capture of charge carriers depending on the applied electric field. Under a negative gate bias, holes accumulate at the OSC/PHPS interface and are subsequently trapped at the hole trap sites within the PHPS CTL, resulting in nonvolatile memory behavior.[38,40] Accordingly, successful write operations are observed in both OST devices, as evidenced by the negative shift in the transfer curves (red lines with circles in Fig. 2e and f). During the erase operation under a positive gate voltage ($V_{G,Bias}$ = +90 V), electrons encounter a high injection barrier from the S/D electrode to the OSC layer, leaving the OSC layer in a depletion state. Region A where the thickness between the source and gate electrodes is on the order of several hundred nanometers, exhibits a vertical potential gradient under conditions of the OSC depletion (Fig. 2c and Fig. S2, ESI†). In contrast, in region B, the vertical potential gradient diminishes as the distance from the source increases, implying that the CTL experiences an insufficient electric field. As a result, hole detrapping does not occur in region B, rendering the erase operation ineffective. Fig. S2 (ESI†) presents the simulated result of the entire device without Ag NPs under an erasing voltage ($V_{G,Bias}$ = +90 V), clearly showing the negligible potential gradient throughout region B. This corresponds to the transfer curve of the device without Ag NPs, which remains unchanged even at V_G = +90 V (green line with circles in Fig. 2e). In contrast, the OST device with Ag NPs exhibits a vertical potential gradient across both regions A and B during the erase operation, unlike the device without Ag NPs (Fig. 2d). Due to the nanoscale gaps between the source electrode and the NPs, as well as between adjacent NPs, and the conductive nature of Ag NPs, the potential gradient across these nanoscale gaps in lateral direction is negligible. Consequently, these NPs could effectively form an nearly identical potential to that of the source electrode. As a result, a significant potential difference is established in the vertical direction from the OSC to gate electrode, even in region B, where there is no direct overlap with the source electrode. This leads to the generation of a strong bottom-up electric field during the erase operation at positive V_G, thereby enabling successful hole detrapping and erasing of the device with 5-nm thick Ag NPs, as shown in the green line with circles in Fig. 2f. Fig. S3 (ESI†) presents the transfer curves of devices incorporating 2-nm and 10-nm thick Ag NPs after the writing and erasing processes. Both devices successfully exhibit writing and erasing characteristics, as indicated by the red and green lines in Fig. S3 (ESI†), respectively.

Fig. 3a presents a graph of the memory on-current and memory off-current as a function of Ag NP thickness. The values were extracted from Fig. 2e, f, and Fig. S3 (ESI†). For the device without Ag NPs (corresponding to a 0-nm Ag NP thickness), the drain current at a gate voltage of −15 V was defined as the memory on-current and memory off-current. For devices from 2-nm to 15-nm thick Ag NPs, the drain current at a gate voltage of 0 V was used. As the NP thickness increases from the Ag-free device, off-currents remains relatively constant, while the on-current exhibits an increasing trend from 1.57×10^{-10} A to 2.30×10^{-6} A. However, when the Ag NP thickness reaches 15 nm or more, the source and drain become shorted, causing the compliance current (10 mA) to flow. This phenomenon would be attributed to the complete coverage of Ag NPs over the pentacene surface, leading to direct connection between the source and drain electrodes. Fig. 3b shows the memory window of the OSTs as a function of Ag NP thickness. Here, the threshold voltage was defined as the gate voltage at which the drain current reaches 1 nA in each transfer curve, while the memory window was determined by the difference in threshold voltage between the write and erase operations.[43–45] For the device without Ag NPs (0-nm Ag NPs), the memory window is negligible. However, for devices with Ag NP thicknesses ranging from 2 nm to 10 nm, the memory window significantly increased from 43 V to 64 V, exceeding 50 V as the NP thickness increased. The mobility values remained relatively constant at approximately 0.07 $cm^2 V^{-1} s^{-1}$ for devices with Ag NP thicknesses ranging from 0 nm to 5 nm (Fig. 3c). In contrast, a significant increase in mobility to 0.22 $cm^2 V^{-1} s^{-1}$ was observed for the device with a 10-nm-thick Ag NP layer. This enhancement is presumably due to the extensive coverage of Ag NPs on the pentacene layer, as evidenced in Fig. S4 (ESI†), which likely improves the effective conductivity of the channel. In addition, the devices without Ag NPs and those with 2-nm, 5-nm, and 10-nm thick Ag NPs exhibit similar values of 2.20, 2.57, 2.41, and 1.70 V dec^{-1}, respectively, within the margin of error (Fig. 3d). Fig. 3e presents the reliable memory characteristics observed over 10 cycles of writing and erasing processes. This evaluation involved analyzing the threshold voltage shift in two types of OSTs—one without Ag NPs and one with Ag NPs. The threshold voltage was defined as in Fig. 3a.[43] As demonstrated in Fig. 2, the device without Ag NPs failed to perform the erase operation after the write operation, resulting in nearly similar threshold voltages for both states. In contrast, in Ag NP-deposited devices, the threshold voltage shifts repeatedly in the negative direction after the write operation and in the positive direction after the erase operation, unlike in the Ag-free device. Fig. 3f and g illustrate the retention characteristics of OSTs without and with Ag NPs. As shown in Fig. 3f, the erase operation does not occur in the Ag-free device, leading to

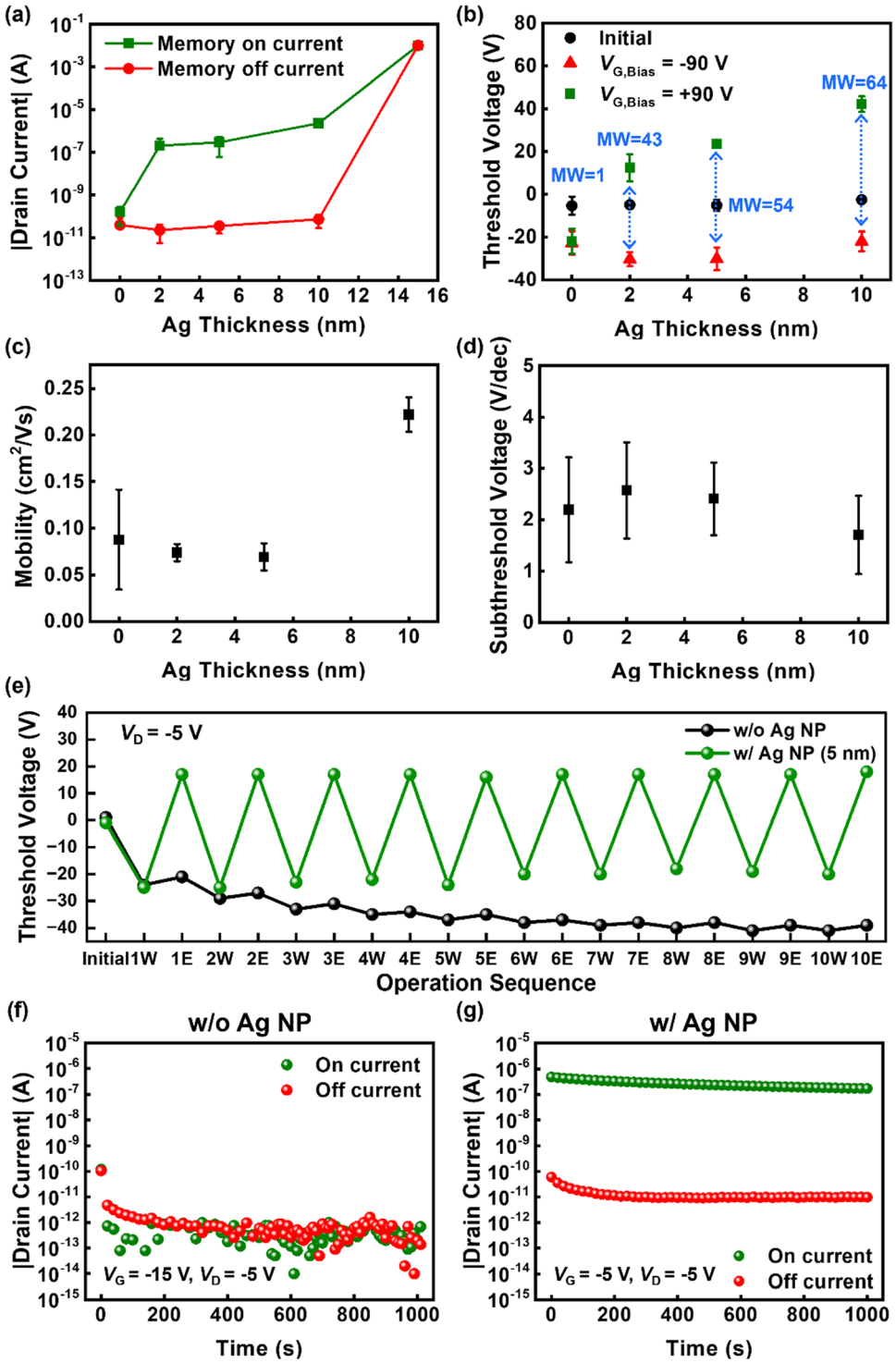

Fig. 3 (a) Graph of the memory on-current and memory off-current, (b) memory window, (c) mobility values, and (d) subthreshold voltage values of the OSTs as a function of Ag NP thickness. (e) Ten cycles of writing and erasing processes. Retention characteristics of OSTs (f) without and (g) with Ag NPs.

negligible differences between the on-current and off-current. However, in the OST with 5-nm thick Ag NPs, the on-current (4.81×10^{-7} A) and off-current (9.38×10^{-12} A) were maintained for up to 1000 s. Similarly, OSTs with 2-nm and 10-nm thick Ag NPs exhibited good retention characteristics, comparable to the 5-nm thick device (Fig. S5, ESI†). To explore the applicability of other metal materials, Au and Al—both widely used in organic electronics—were employed as S/D electrodes in the proposed OSTs with metal NPs. Fig. S6 (ESI†) presents the electrical characteristics of NP-based OSTs with three different metal electrodes (Au, Ag, and Al) as a function of deposition thickness. In the case of Au NPs, the device exhibited both writing and

erasing operations, similar to Ag NP-based devices. However, it showed relatively higher off-current levels even at a metal thickness of 2 nm (Fig. S6a, ESI†). This can be attributed to the low energy barrier between the Au NPs and the pentacene layer, which facilitates charge movement and results in a high off-current. At a thickness of 5 nm, the off-current further increased, leading to a low on/off current ratio of approximately one order of magnitude (Fig. S6b, ESI†). When the Au NP thickness reached 15 nm, the device ceased to function normally, as the source and drain electrodes became shorted, causing the current to reach the compliance level (Fig. S6c, ESI†). For comparison, the electrical characteristics of Ag NP-based devices are shown alongside Au and Al NP-based devices in Fig. S6d–f (ESI†). Regarding Al NPs, aluminum is easily oxidized, which inhibits charge transport. At thicknesses of 1 nm and 5 nm, the deposited Al failed to function as a conductive region capable of enhancing the vertical electric field during the erasing operation, unlike Au and Ag NPs. As a result, devices with 2-nm and 5-nm thick Al NPs did not exhibit erasing functionality (Fig. S6g and h, ESI†). Additionally, due to Al's tendency to form a continuous thin film, the Al NP-based device with a thickness of 7 nm became shorted between the source and drain electrodes, leading to a compliance current level (Fig. S6i, ESI†). From these results, we could conclude that Ag NPs, compared to Au and Al, provide an optimal energy barrier with the pentacene layer, while also benefiting from a higher work function than Al, which prevents oxidation. As a result, devices incorporating Ag NPs with thicknesses ranging from 2 nm to 10 nm demonstrated reliable writing and erasing operations along with good electrical performance. The sufficient process margin of Ag deposition thickness ensures the fabrication of reliable and stable synaptic transistors for next-generation computing components. Thus, Ag is an appropriate metal material for forming NPs in our proposed device.

To verify the applicability of Ag NP-based OSTs for neuromorphic computing, we first controlled the conductance of both devices (without and with Ag NPs) using gate voltage spikes, as shown in Fig. 4a and b. The multi-conductance levels, representing the memory states of the OSTs, demonstrate the devices'

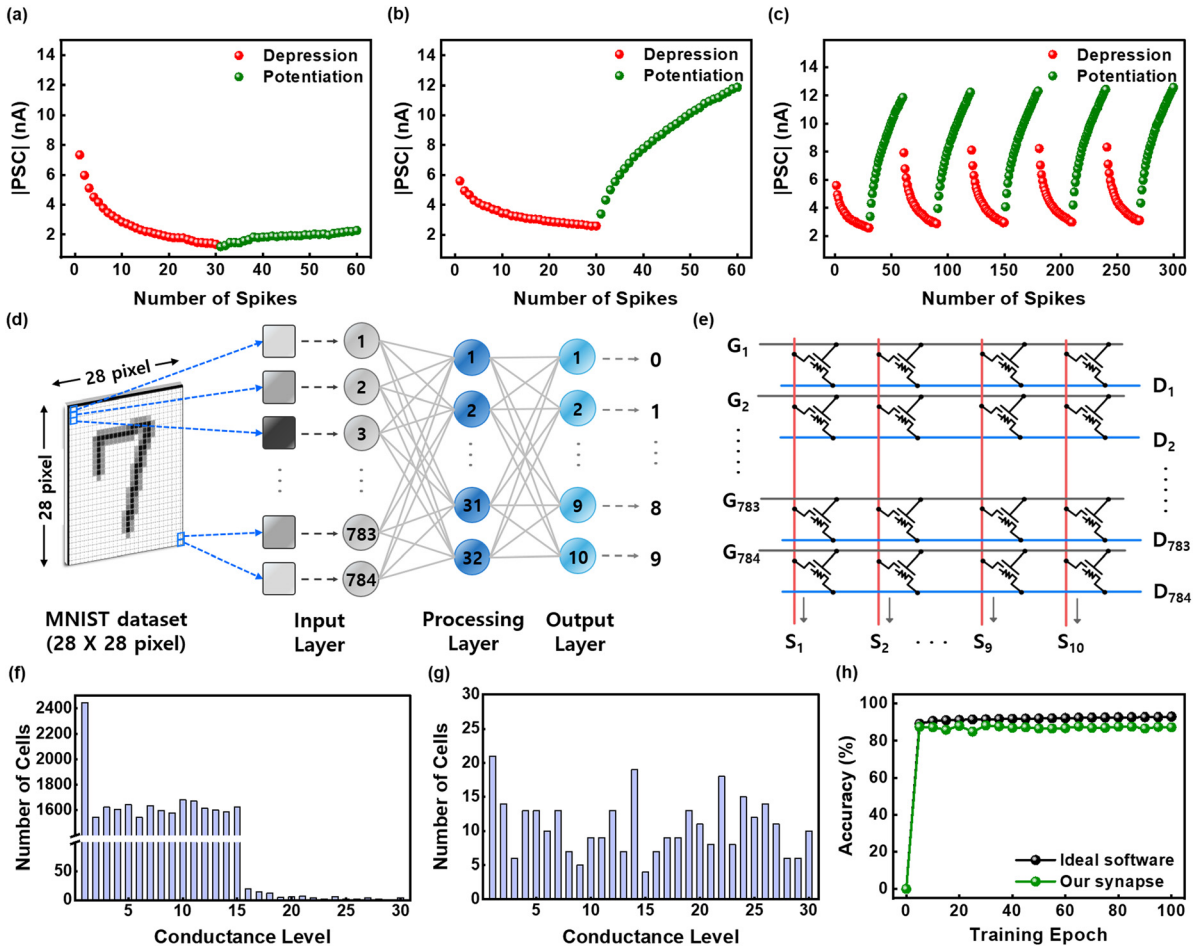

Fig. 4 (a) Multi-level conductance of both devices without and (b) with Ag NPs using gate voltage spikes. (c) Five cycles of 30-state potentiation and depression in the proposed device with Ag NPs. (d) Hardware neural network consisting of three layers (784 input neurons, 32 processing neurons, and 10 output neurons corresponding to digit classes) for recognizing handwritten digit. (e) OST cell arrays individually serving as artificial synapses connecting the neuron layers for hardware neural network. (f) Channel conductance-level distribution between the first and second neuron layers and (g) between the second and third layers after 100 training epochs. (h) Classification accuracy of the hardware neural network employing our OSTs, achieving 87.3% in classifying handwritten digits.

ability to reliably mimic the synaptic weights of biological synapses. In the reference device (Fig. 4a), depression characteristics were achieved at $V_G = -20$ V for 0.5 s at the read voltage of $V_D = -5$ V. Potentiation was induced using electrical spikes of $V_G = 39$ V at the read voltage of $V_D = -5$ V. However, during the potentiation process (erasing operation), the device failed to exhibit erasing behavior or synaptic potentiation characteristics due to an insufficient vertical electric field, instead maintaining constant conductance memory levels throughout the erasing process. In contrast, our proposed synaptic device incorporating Ag NPs exhibited 30 distinct levels of depression and potentiation. Furthermore, as shown in Fig. 4c, it demonstrated reliable operation of five cycles of 30-state potentiation and depression. Specifically, 30 depression levels were achieved at $V_G = -20$ V for at the read voltage of $V_D = -5$ V, while 30 potentiation levels were induced by electrical spikes of $V_G = 30$ V at the read voltage of $V_D = -5$ V. Note that the symmetry between potentiation and depression characteristics could be further enhanced by optimizing the erasing process, such as through tuning the erase pulse waveform and amplitude.[46] As previously explained, the presence of Ag NPs enhanced the vertical electric field strength in our device, enabling both the erasing process and synaptic potentiation (observed as a significant positive shift in the transfer curve away from its initial state). This resulted in an enlarged memory window, an increased on/off ratio, and stable potentiation/depression characteristics. By introducing Ag NPs to modulate the vertical electric field, we successfully demonstrated a 30-state multi-memory level and stable synaptic potentiation/depression properties, which could not be achieved in the reference OST. Our device exhibited superior performance metrics, including memory window, the number of distinct conductance states for potentiation and depression, conductance modulation ratio, and energy consumption, compared to previously reported oligomeric synaptic transistors demonstrating potentiation and depression characteristics solely controlled by electrical pulses (Table S1, ESI†).

To evaluate the potential of our proposed OSTs for computing applications, hardware-based neural networks were implemented using our device cells as artificial synapses. Numerical simulations were conducted to assess system performance in handwritten digit recognition tasks using the MNIST dataset. As illustrated in Fig. 4d, the neural network architecture comprised three layers: 784 input neurons, 32 hidden neurons, and 10 output neurons corresponding to digit classes. Our OST cells served as artificial synapses connecting the neuron layers (Fig. 4e). A non-negative weight was employed to efficiently map the weight value onto the conductance of the hardware synapse cell. To emulate real hardware behavior, ideal weights were calculated from software-based training for 100 epochs with 60 000 MNIST images. At the software training level, the softmax activation function was applied for the output value.[47] The training process utilized the adaptive momentum estimation optimizer[48] and the sparse categorical cross-entropy loss function.[49] The weights were quantized into 30 discrete levels, corresponding to the available conductance states of the synaptic devices. Fig. 4f and g show the resulting conductance distributions after training, corresponding to synaptic connections between the first and second neuron layers, and between the second and third layers, respectively. For performance evaluation, the system's ability to classify 10 000 test images from the MNIST dataset was examined. Notably, the hardware neural network employing our OSTs achieved a classification accuracy of 87.3%, approaching the ideal software-based accuracy of ~93.0% (Fig. 4h). This accuracy could likely be attributed to the gradual and linear potentiation characteristics of our devices.

These results highlight the potential of the developed OSTs as promising synaptic elements for hardware-based neural networks, capable of supporting advanced computing applications such as pattern recognition, image processing, and motion detection. Furthermore, the demonstrated multi-level conductance modulation and enlarged on/off current ratio provide valuable design insights for overcoming the intrinsic limitations of conventional charge-trapping devices, particularly their write-once-read-many (WORM) behavior in the absence of Ag nanoparticles.

4. Conclusions

In summary, we have demonstrated a novel approach to overcoming the longstanding challenge of electrical erase operations in charge-trapping-based OSTs by integrating metal NPs atop a wide-bandgap oligomeric semiconductor. The inclusion of Ag NPs effectively modulated the vertical electric field, enabling both electrical writing and erasing, which was previously unattainable in conventional devices. Our proposed strategy significantly expanded the memory window, achieving 30 distinct potentiation and depression states with stable retention and endurance characteristics. Furthermore, numerical simulations and experimental analyses confirmed that the enhanced vertical electric field facilitated efficient hole detrapping during the erase process, thereby enabling reliable bidirectional modulation of synaptic weights. This advancement was successfully applied to a neuromorphic computing system, where our Ag NP-based OSTs achieved an MNIST classification accuracy of 87.3%, comparable to ideal software-based implementations. The findings of this study provide a promising pathway for the development of next-generation flexible neuromorphic electronics. By addressing a key limitation in organic artificial synapses, our approach paves the way for the practical implementation of wearable and further bio-integrated neuromorphic systems, advancing the frontier of human–machine interfacing, personalized healthcare, and brain-inspired computing.

Author contributions

Y. H., Y.-W. L., H.-L. P., and M.-H. K. initiated and designed the experiments, analyzed the data, and wrote the draft of the manuscript. Y. H. and Y.-W. L. fabricated and characterized the devices. Y. H. measured the electrical characteristics of the

devices. C.-H. K. performed and analyzed numerical simulations. All authors discussed the results and commented on the manuscript.

Data availability

The data supporting this article have been included as part of the ESI.†

Conflicts of interest

The authors declare no competing financial interest.

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