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A vapor-liquid-solid (VLS) mechanism has been successfully applied to homoepitaxial growth of 4H-SiC films in chemical vapor deposition (CVD), the key to which is the use of a Si-Pt alloy flux in the CVD-VLS process. The n-type residual carrier density in the VLS-grown SiC films could be reduced down to the order of 10^{15} cm^{-3} despite a possible concern about impurities working as dopants incorporated into the grown films in VLS. The surface morphology essentially exhibited a bunched step-and-terrace structure, as similarly observed in solution-grown SiC crystals. Furthermore, the dislocation propagation behaviors, investigated by X-ray topography analysis, were also rather like in solution growth processes, different from those in conventional CVD processes. That is, threading dislocations can be converted to basal plane dislocations in their propagation in the CVD-VLS process, illustrating its potential of effectively reducing the total dislocation density in the resultant SiC thick films.

"VLS" is the abbreviation of "vapor-liquid-solid", a growth mechanism of crystals via liquid in vapor deposition. The term was first used by R. S. Wagner and coworkers in their work published in Applied Physics Letters in 1964 [1], in which they reported on the growth of single crystalline Si whiskers via Au droplets in chemical vapor deposition (CVD). Most studies on the VLS mechanism have been focusing on its applications to development of new fabrication processes for whiskers, nanowires and nanorods of various materials, such as Si and other compound semiconductors, as well as oxides and carbon nanotubes, as one of the most representative nano-technologies in material science. On the other hand, the VLS mechanism is also expected as a next generation vapor growth process for single crystal films. This is because the VLS mechanism has much potential to overcome the problems of vapor-deposited films, such as compositional deviation and relatively low crystallinity, inherent to non-equilibrium nature of the vapor deposition process, as well as further potential to, in principle, achieve as a high-speed growth as the solution growth process. Accordingly, this kind of VLS applications is often termed "Tri-Phase Epitaxy (TPE)" [2] or "Flux-mediated Epitaxy (FME)" [3, 4] to differentiate from the conventional VLS processes for whiskers and nanowires.

The first attempt to apply the VLS mechanism to the growth of single crystal SiC films can date back to the early 2000s (2002) by Ferro and his coworkers [5], and the followers include a group from Taiwan reporting in 2015 [6] and our group since our first publishment of VLS growth of SiC films in 2016 [7]. However, there has been a concern about a possible incorporation of additive impurities in the flux into VLS grown crystals and films, leading to a significant deterioration in their characteristics. In fact, the Al doping level reaches on the order of 10^{20} cm^{-3} in the VLS grown SiC films with the Al-added Si flux, as reported in our previous work [8,9]. The inclusion of such additive impurities can become a more serious problem if the VLS process is to replace the existing CVD process for high-speed growth of high-purity epitaxial SiC layers on SiC single crystal wafers.

Recently, we have found a new additive impurity of Pt, whose atomic radius is larger than those of Si and C atoms, to achieve the step-flow growth of 4H-SiC films on 4° off 4H-SiC (000-1) substrates at a growth temperature lower than 1500°C and to effectively suppress the step-bunching [10]. In addition, the VLS grown SiC films seem to include too little Pt atoms to be indetectable by SIMS, thereby exhibiting as excellent electric properties as SiC bulk single crystals used as substrates. Nevertheless, there is still a problem of the residual carrier density in the VLS grown SiC films, whose value could not be less than the order of 10^{18} cm^{-3} [10], and the quality of SiC films had not been enough as epitaxial layers on wafers. Since our VLS process is based on pulsed laser deposition (PLD) instead of

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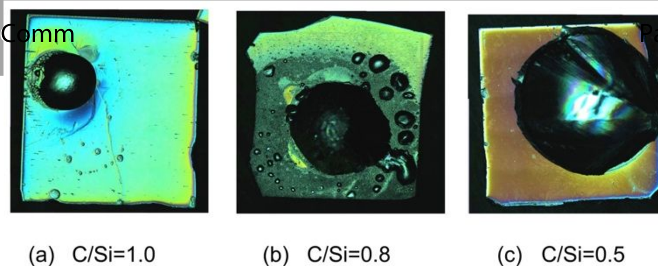
CVD, one of the origins of such large residual carrier density values in the SiC films is probably the impurities that have been included in the target used as a solid source of SiC, which would be difficult to circumvent in the PLD process. In contrast, CVD growth is a process conventionally employed for SiC homoepitaxial layers. Owing to development of step control epitaxy [11, 12] and site-competition [13, 14] techniques, specular surfaces with a perfect polytype stability and low doping concentrations less than 10^{15} cm^{-3} have come to be easily realized on Si-face 4H- and 6H-SiC homoepitaxial layers. In addition, low growth pressure conditions less than about 250 mbar also have enabled to reduce the doping concentration even in C-face SiC homoepitaxial layers [15]. That is, we have now come to be able to realize the doping concentration less than 10^{15} cm^{-3} regardless of the face polarity [16, 17].

With these backgrounds, in this study, we attempt CVD-based VLS growth of SiC films by using Si-Pt alloy flux to see the potentiality of how much the residual carrier density can be reduced in the VLS-grown SiC films. Furthermore, we investigate how the dislocations that originally exist in a SiC bulk single crystal substrate will propagate into the subsequent grown epitaxial layer by using X-ray topography. As a result, the residual carrier density could be reduced to as low as on the order of 10^{15} cm^{-3}, and the propagation behaviors of dislocations in the VLS process are found to be rather similar to those in the solution growth process than in the conventional CVD process.

4° off n-type C-face 4H-SiC (000-1) and Si-face (0001) substrates (7 mm × 7 mm) purchased from Cree. Inc were used as seed substrates after ultrasonic cleaning with ethanol, acetone and ultrapure water, consecutively. Prior to CVD experiment, Pt-Si alloy ($Si_{80}Pt_{20}$) flux was prepared on a substrate as follows: Si (0.625mmt: Shinetsu Chemical Co. or RYOKO Co.) and Pt (3 N, 0.1mmt: Nilaco Co.) in an arbitrary bulk amount were placed on the substrate and once melted together by annealing in a vacuum chamber up to a temperature of 1250 °C to ensure the homogeneous composition of the Pt-Si alloy. The Pt-Si alloy-covered substrate was then introduced into a standard CVD chamber system and SiC was deposited on that substrate. For all the films, the deposition time was set to 240 min in a total pressure of 250 mbar inside the chamber under the following growth conditions: the growth temperature was 1550 °C and the flow rates of H_2, SiH_4 and N_2 gases were 40 slm, 6.67 sccm and 0.1 sccm, respectively. On the other hand, the flow rate of C_3H_8 gas was varied from 1.11 to 2.24 sccm, according to which the supplied ratio of C/Si ratio was adjusted to be from 0.5 to 1.0. The Pt-Si alloy flux that remained after the deposition was removed by a multi-step chemical etching process with a mixed solution of nitric acid (HNO_3) and hydrofluoric acid (HF) (1 : 1), and aqua regia, a mixed solution of HNO_3 and hydrochloric acid (HCl) (1 : 3). The thickness of SiC films was estimated by using a technique of Fourier-transform infrared (FT-IR) spectroscopy in a wavelength range of 400 to 4000 cm^{-1} with a ceramic heater as the IR light source. The polytypes of the grown SiC films were identified by micro-Raman spectroscopy with a probe laser of 532.1 nm. The flux on the films and their surface morphology were observed with a



(a) C/Si=1.0 (b) C/Si=0.8 (c) C/Si=0.5

Fig. 1 Set of DIC images of SiC film samples as grown on Si-face substrates with different flow rates of C_3H_8. i.e., with different supplied C/Si ratios of 1.0, 0.8 and 0.5, respectively.

differential interference contrast (DIC) microscope and an atomic force microscope (AFM). To estimate the residual carrier density in the grown SiC films, a Schottky barrier diode was formed with a mercury probe contact to the film surface and the capacitance-voltage (C-V) measurement was carried out with a frequency of 1 MHz for Mott-Schottky analysis. To investigate the propagation of dislocations from a substrate into the over-grown layer through the CVD-VLS process, the reflective X-ray topography experiment was performed on BL-15 purposefully set up for X-ray imaging at the Kyushu Synchrotron Light Research Center. The wave length of the incident x-ray beam is 1.5 Å and the reflective g vector is g = –1–128.

Figure 1 displays a set of DIC images of SiC film samples as grown on Si-face substrates with different flow rates of C_3H_8. i.e., with three different supplied C/Si ratios of 1.0, 0.8 and 0.5, respectively. The spherical-like droplets, which are the Si-Pt alloy flux, are seen to remain on all the substrates after deposition. The droplet-like shape of the flux is due to the non-wettable nature of the SiC surface to Si-based liquid flux. As the C/Si ratio increases, the volume of the remaining flux was found to decrease and a similar trend was confirmed in the case of using C-face substrates instead (not shown). Considering the growth temperature as high as 1550 °C, this is probably because Si was gradually evaporated from the melted Si-Pt alloy during the deposition. When the supplied ratio of C/Si is, for example stoichiometric, the amount of Si having been evaporated cannot be compensated for, resulting in a decrease of the volume of flux. As a consequence, an appropriate C/Si ratio to keep the volume of the flux unchanged during the deposition was 0.5 by supplying excessive Si under the present growth conditions e.g., at the growth temperature of 1550 °C in the total pressure of 250 mbar. Incidentally, there are also seen some small droplets around the main large droplet in Fig. 1(b). This is probably due to some accidental gas flow effect by introducing gases in starting deposition.

Based on the above discussion, further DIC observation of the SiC film sample of **Figure 1(c)**, i.e., the SiC film grown at the present C/Si ratio of 0.5, was made after chemical etching to remove the flux, as shown in **Figure 2(a)**. It is found that the surface morphologies of the SiC film areas that have been covered with the flux before the chemical etching are completely different from those outside of the flux-covered area on the same substrate. In addition to this, even within the flux-covered area before the chemical etching, two typically,

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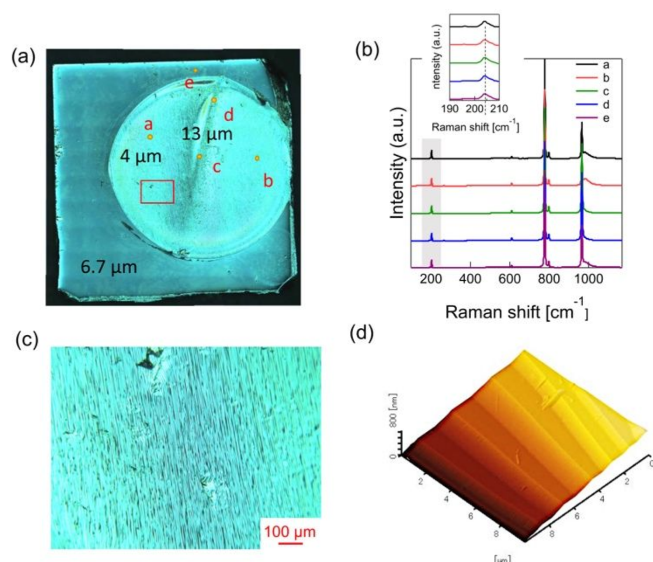

Fig. 2 (a) DIC image of the SiC film sample of Figure 1(c) after chemical etching to remove the flux. (b) Micro-Raman spectroscopy measurement for different point areas denoted by a-e in Figure 2(a). (c) Expanded DIC image of the area enclosed by the red square in Figure 2(a). (d) AFM image of a flat area in Figure 2(a) (10 µm ×10 µm).

different surface morphologies are observed. There is a mountain ridge-like morphology found to run straight across the center of the area, while the other part of the area exhibits a very flat surface. The direction along which the mountain ridge-like morphology is elongated, is confirmed to correspond to the gas flow direction. The reason for this correspondence might be somewhat related to the flux convection and the diffusion of the SiC source in the flux, whose behaviors probably depend on the gas flow direction, but is still much unknown at moment. According to the thickness estimation of the grown SiC film in different areas by FT-IR, the thickness is 6.7 µm for just CVD-grown SiC outside of the flux-covered area, a value typical of conventional CVD grown SiC films under the conditions similar to those in the present study. For SiC which was VLS-grown inside of the flux-covered area, the thickness is about 4 µm in the flat area, while it reaches as large as 13 µm in the area around the mountain ridge-like morphology. Such non-uniformity of the surface morphology and film thickness in the present VLS-grown SiC films by CVD is a challenge to be overcome, through understanding the formation mechanism of the mountain ridge-like morphology, which is seemingly depending on the gas flow conditions in CVD, in our future work.

Figure 2(b) is the results of micro-Raman spectroscopy measurement for different point areas denoted by **a-e** in **Figure 2(a).** The SiC is confirmed to be of the 4H-polytype for all the point areas, including the conventional CVD-grown film area of **e** outside of the flux-covered area. The dominant 4H-polytype is reasonable considering the homoepitaxial growth using 4° off 4H-SiC substrates at a growth temperature of 1550 ºC. It should be pointed out that the wavenumber of the FTA(+) peak is almost the same to be 204 cm^{-1} for all the SiC film areas, strongly suggesting that the SiC film should have a very low residual carrier density, according to the literature of Ref. 18. **Figure 2(c)**

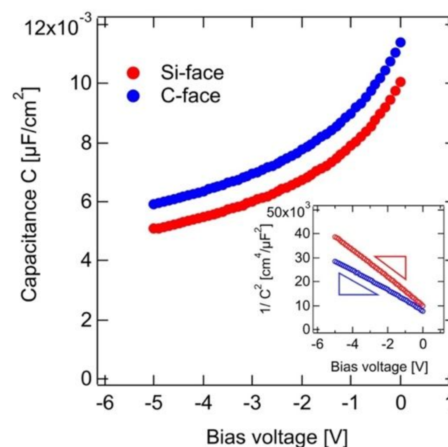

Fig. 3 C-V curves obtained for Schottky diodes which were formed with a mercury probe contact to the surfaces of SiC films VLS-grown under the present conditions on Si- and C-face substrates. The inset is Mott-Schottky plots constructed from the C-V curves.

is an expanded DIC image of the area enclosed by the red square in **Figure 2(a)**. There is macroscopically observed a uniform bunched step-and-terrace structure that has never been found on the SiC surfaces obtained by the conventional CVD process, but is rather close to a surface morphology often found in the solution growth. The obtained surface morphology is quite similar to those of SiC films which are VLS-grown with the Pt-Si flux by PLD and the characteristics of such a surface were confirmed reproducible even in the CVD-VLS process. In fact, AFM observation, as shown in **Figure 2(d)**, revealed that the steps of a flat surface area have an almost unique step height of ~150 nm in average, which is in good agreement with an average step height of ~200 nm in a SiC film VLS-grown by PLD with the Pt-Si flux. Moreover, the average tilt angle estimated from the AFM image is 3.6 º, which value corresponds to the off angle of the substrate (4º) used in this study. From these results, as far as the surface morphology is concerned, there are little difference between the VLS-grown SiC films by PLD and CVD, except for the formation of a mountain ridge-like morphology, which is seemingly depending on the gas flow conditions such as its direction in CVD.

Figure 3 shows a set of C-V curves obtained for Schottky diodes which were formed with a mercury probe contact to the surfaces of SiC films VLS-grown under the present conditions on Si- and C-face substrates as discussed in **Figure 1**, respectively. Mott-Schottky plot analysis, as shown in the inset of **Figure 3,** evaluated the residual carrier density of the SiC films; the carrier density values which were averaged over the depletion layer formed in the C-V measurement are 2.54×10^{15} cm^{-3} and 3.11×10^{15} cm^{-3} for the Si- and C-face SiC films, respectively. These values are almost the same, irrespective of their growth polarity, as low as the typical values of CVD-grown SiC films under the conditions similar to those in the present study, which suggests that no acceptors would affect the carrier type

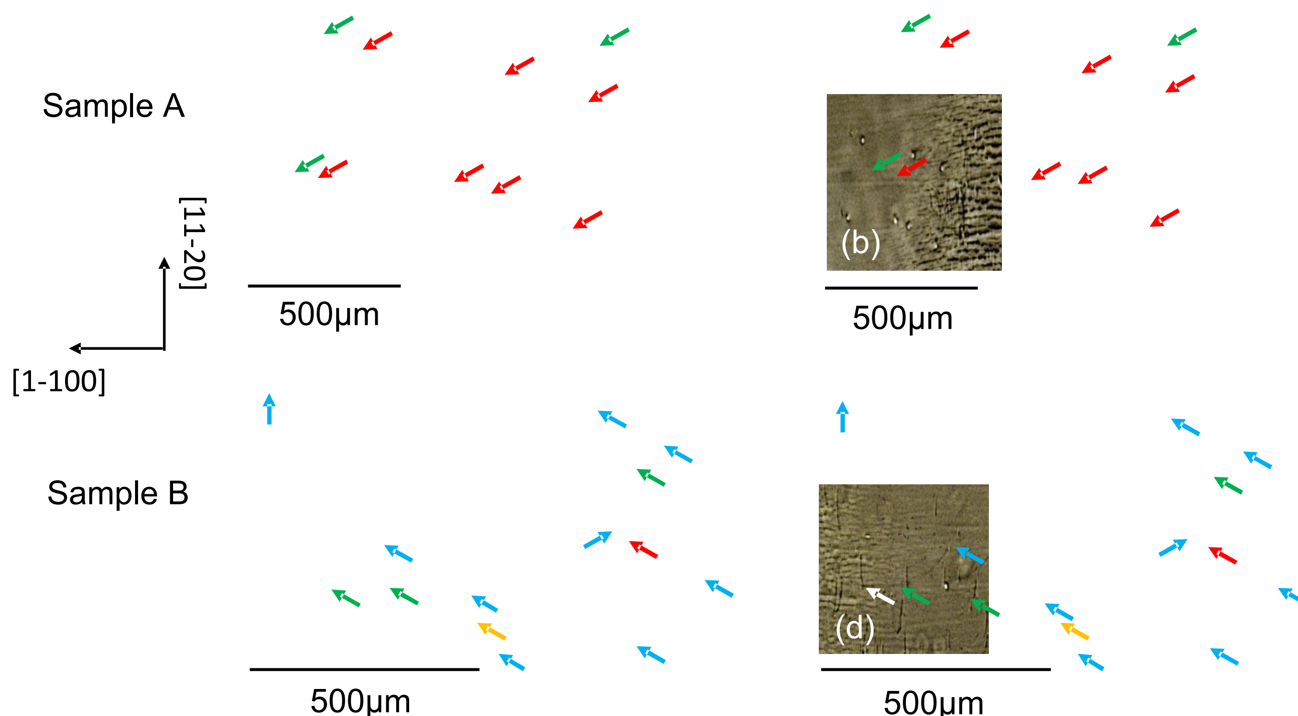

Fig. 4 X-ray topography images of two different samples, taken in the reflective mode, before and after the growth of SiC films prepared on C-face 4H-SiC substrates under the same conditions. (a)&(b) are a set of dislocation images of an area of the substrate for sample A, (c)&(d) are that for sample B.

in the SiC films. As mentioned in Introduction, the residual carrier densities in VLS-grown SiC films by PLD could not be less than the order of 10^{18} cm^{-3}, i.e., the present carrier density in the VLS-grown SiC films by CVD has been much reduced by three orders of magnitude. The encouraging result implies that intrinsic semiconductor films of SiC could be fabricated in the VLS mechanism, as long as an appropriate flux, such as Si-Pt alloy, were used.

Finally, it was investigated how the defects and dislocations that originally exist in a SiC bulk single crystal substrate will propagate into the subsequent grown epitaxial layer by using X-ray topography. **Figure 4** shows X-ray topography images of two different samples (sample A and sample B), taken in the reflective mode, before and after the growth of SiC films prepared on C-face 4H-SiC substrates under the present conditions. For these samples, the C/Si ratios of sample A and sample B are 0.65 and 0.5 by changing the C_3H_8 flow rate, respectively, while other growth conditions are exactly the same in these samples. **Figures 4(a)** and **4(b)** are a set of dislocation images of an area of the substrate for sample A and the SiC layer subsequently VLS-grown over the same area of the substrate, while **Figures 4 (c)** and **4 (d)** are a similar set of those for sample B. First of all, it is of great impact that many straight white lines identified as scratches, which had been generated by polishing the substrate surface, as found in **Figure 4(a)** and **4(c)** perfectly disappeared in the VLS- grown layer as shown in **Figure 4(b) and 4(d)**. In conventional CVD processes for 4H-SiC layers on SiC wafers, the wafer surface is often pre-treated with H_2 to remove such scratches from the surface. However, in the present VLS process by CVD, such an in-situ H_2 etching pre-treatment was not applied. This could be as a result of the etch back, which is a well-known phenomenon occurring at the liquid-solid interface in liquid or solution growth [19,20]. In fact, the Si-Pt alloy flux, according to our previous in-situ study with a confocal laser scanning microscope, is found to have a significant ability to etch back the substrate at the solution growth interface of SiC [10]. It is thus concluded that a similar etch back effect to that in the solution growth occurs even in the present CVD-VLS process with the Si-Pt alloy flux. Secondly, for sample A, there are observed at the substrate some threading screw dislocations (TSDs) and threading edge dislocations (TEDs), which are imaged as large and small white spots, as indicated by the red (TSD) and green (TED) arrows, respectively. In addition, the black lines in **Figure 4(a)** are identified as basal plane dislocations (BPDs). These TSDs and TEDs at the substrate are found to remain the same threading dislocations respectively, even after propagating into the VLS-grown SiC layer, as shown in **Figure. 4(b)**. The positions of these threading dislocations at the SiC layer are indicated by the same arrows as used in **Figure 4(a)**, respectively and their dislocation propagation behavior is quite similar to that found in the conventional CVD processes for 4H-SiC epitaxial layers [21]. On the other hand, when comparing between **Figure 4(c)** and **4 (d)**, a different dislocation propagation behavior can be found for sample B, which was even prepared nominally under the same conditions except for the C/Si ratio as sample A. It is clear that many BPDs imaged as black or white lines along the [11-20] direction are observed in the topographic image of sample B, as indicated by the light blue arrows in **Figure. 4(d)**. To look into how these BPDs had propagated from the substrate, their

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positions at the SiC layer were traced back to their original positions at the substrate, at any of which positions the weak white small spots, which are assigned as TEDs, were found, as indicated by the same light blue arrows in **Figure 4 (c)**. That is, TEDs at the substrate were converted to BPDs through the VLS growth process. In addition, the large white spot at the substrate indicated by the yellow arrow in **Figure 4(c)**, which is assigned as a TSD, is also converted to the BPD at the SiC layer indicated by the same yellow arrow in **Figure 4(d)**. These kinds of conversions from threading dislocations to BPDs in the growth of 4H-SiC homoepitaxial layers, which are characteristic of the solution growth processes [22], are possible even in the VLS process with liquid flux such as a Si-Pt alloy melt among vapor deposition processes, and will be never found, e.g., in the conventional CVD processes. In the solution growth process, most threading dislocations reportedly are converted to BPDs during the growth. This phenomenon might be explained as the result of the strong step-flow growth and image force at the step edges with relatively large step heights. By the comparison between sample A and B, the threading dislocations in sample B tend to be converted to BPDs more easily than those in sample A. For the CVD growth process of 4H-SiC films, lower C/Si ratios are found to enhance the step-flow growth mode [23]. If this holds true for the CVD-VLS process, the step-flow growth would be more enhanced in sample B than in sample A, and possibly affect the efficiency of converting threading dislocations into BPDs between sample A and sample B, though the speculation should be clarified in our future work. However, a careful comparison between **Figure 4 (c)** and **4(d)** revealed that all the threading dislocations observed at the substrate were not converted to BPDs at the SiC layer in the VLS process. At the substrate, for example, the TSD and some of the TEDs indicated by the red arrow and the green arrows, respectively in **Figure 4(c),** are found to remain the same threading dislocations respectively, even after propagating into the VLS-grown SiC layer. On the other hand, there were appeared some BPDs in **Figure 4(d)** which could not be traced back to the original positions of TEDs in **Figure 4 (c),** as indicated by the white arrows. According to M. Dudley's group in Stony Brook Univ.[24], scratches can generate TED-TED pairs or BPD-TED pairs, along them on a 4H-SiC substrate surface. As a possible origin of the BPDs whose origin is unclear, it is from such BPD-TED pairs that some BPDs newly developed into the VLS-grown SiC layer. However, since most BPD-TED pairs exist near the substrate surface the strong etch back process with the Pt-Si flux as already pointed out, should remove them prior to starting the VLS growth. Thus, a most probable case is that the BPDs whose origin is unclear in **Figure 4(d)** have resulted from the conversion of TEDs hidden by the scratch mat as found in **Figure 4 (c)**. Indeed, some scratches in **Figure 4(c)** are imaged as strong white lines. Nevertheless, these overall results suggest that the CVD-VLS growth process has a possibility to convert threading dislocations to BPDs in their propagation. However, the conversion behaviors are not so reproducible in the CVD-VLS process at the moment. Further investigations are highly required to clarify the mechanism of this dislocation conversion during the CVD-VLS growth.

In CVD-VLS growth of 4H-SiC films, potential of further improving their structural and electric properties was investigated by using a Si-Pt alloy flux. In this process, an appropriate C/Si ratio, as far as investigated, was determined to be 0.5, i.e., an excess condition of Si is favored to compensate for Si re-evaporating at a high growth temperature of 1550 ^{o}C, thereby stabilizing the Pt-Si flux during the process. The VLS-grown SiC films show some features similarly found in solution-grown SiC crystals. First, though it is not uniform in morphology, the film surface essentially exhibits a bunched step-and-terrace structure that has never been found in conventional CVD processes. Secondly, in the CVD-VLS process threading dislocations can be converted to basal plane dislocations in their propagation, which allows us to expect reduction of the total dislocation density of the SiC films after further optimization as compared with the conventional CVD processes. The most achievement is the n-type residual carrier density being as small as on the order of 10^{15} cm^{-3} in the VLS-grown SiC films.

Conflicts of interest

The authors declared that there is no conflict of interest.

Acknowledgments

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