Materials Advances

ROYAL SOCIETY OF CHEMISTRY

REVIEW

View Article Online
View Journal

Cite this: DOI: 10.1039/d5ma00713e

Toward AI-ready hardware: review of single-crystal halide perovskite FET fabrication and performance

Hyojung Kim

This article explores the latest developments in single-crystal halide perovskite field-effect transistors (FETs), focusing specifically on methods to mitigate ion migration and achieve stable operation at room temperature. Following the discussion on the interconnections between dimensionality, lattice softness, and defect statistics, we proceed to examine the methods of solution- and vapor-phase growth that yield layers free of grain boundaries and characterized by a minimal presence of mobile vacancies. The examination of composition tuning, spacer-cation engineering, and interface passivation strategies is conducted to assess their effectiveness in increasing the activation barrier for ionic drift while maintaining electronic transport integrity. Dielectric selection and contact metals are discussed. This review presents a mechanism-focused framework that links crystal dimensionality, ion migration regulation, and device geometry into practical design principles for stable single-crystal perovskite devices. The comparison of device structures, such as coplanar, floated, and vertical architectures, illustrates how field orientation and channel thickness influence the relationship between lattice polarization and carrier accumulation. This analysis outlines a feasible way for converting perovskite FETs to viable, energy-efficient logic, sensing, and photonic circuits suitable for production. The ongoing integration of crystal design and interface engineering is anticipated to address existing stability issues and accelerate the commercial use of flexible and wearable technologies.

Received 5th July 2025,
Accepted 1st October 2025

DOI: 10.1039/d5ma00713e

rsc.li/materials-advances

1. Introduction

The advancements in artificial intelligence inference, edge computing, and interconnected sensor networks have highlighted throughput constraints and considerable power consumption.[1–4] Future electronic components require materials that enable quick charge transport while allowing for low-temperature fabrication across large areas, leading to integrated systems that operate with minimal energy loss.[5–12] Among the candidate compounds, halide perovskites have garnered considerable attention owing to their exceptional ability to combine ionic movement with electronic conduction.[13–16] This feature increases their attractiveness for upcoming advancements in memory, logic, and photonic technologies.

Metal halide perovskites became known as adaptable semiconductors due to their ABX_3 lattice, which allows for extensive ionic substitution, processing at low temperatures, and robust optoelectronic coupling. Investigations into this family began in 1999 with two-dimensional (2D) phenylethylammonium tin iodide (PEA_2SnI_3), demonstrating that layered perovskites can enable gate-driven transport, even in the presence of their soft lattices.[17] The interest rose following the quick rise of perovskite photovoltaics, with three-dimensional (3D) methylammonium lead iodide ($MAPbI_3$) swiftly establishing itself as a model channel material. Initially, $MAPbI_3$ transistors functioned solely at low temperatures, as ionic drift and shallow defects obscured the inherent field effect at room temperature.[18,19] Pulse-biased measurements broadened the observable window into ambient conditions by detecting carrier modulation prior to its suppression by ion migration at extended times.

Continuous operation at room temperature was ultimately achieved as solvent-mediated surface cleaning and vacancy passivation minimized the presence of mobile ions in solution-processed films. The focus then transitioned to innovative compositions that might reduce toxicity issues and enhance carrier polarity. Sn-based perovskites exhibit intrinsic p-type behavior, while the incorporation of bismuth (Bi) and silver (Ag) alloys presents lead-free alternatives.[20–22]

In contrast to Pb-based lattices, Sn-based systems tend to the gradual oxidation of the metal center. This process leads to an increase in hole density, alters the electronic surroundings, and enhances scattering, ultimately resulting in a decline in mobility over time. Bi-based perovskites exhibit distinct

Department of Semiconductor Systems Engineering, Sejong University, Seoul 05006, Republic of Korea. E-mail: hyojungkim0912@sejong.ac.kr

oxidation processes that promote the formation of deep defects and interfacial byproducts, which compromise carrier injection and reduce the available gate window over extended operation periods. The differences lead to varying levels of threshold stability, hysteresis, and retention. Therefore, it is essential to combine reactive composition management with specific interface passivation and strong encapsulation to address these issues. A significant advancement occurred when the fields of composition and crystallization engineering produced fully inorganic $CsSnI_3$ thin films exhibiting exceptional structural coherence.[23,24] The results indicate that precisely adjusted stoichiometry and lattice rigidity can effectively limit ion migration while maintaining the favorable processing conditions characteristic of perovskites.

While these developments are promising, a thorough understanding of the relationships between lattice dimension, dielectric selection, contact energetics, and ambient stress remains lacking. The ability of the perovskite lattice to accommodate compositional variations creates a design space. However, the same flexibility that facilitates easy processing also encourages the formation of vacancies and the movement of ions. Dielectric layers are required to provide substantial capacitance while protecting the crystal against moisture and energetic oxidation. Contact metals require suitable work functions and chemical durability to prevent halide-induced corrosion, which can result in an increase in barrier height over time. It is essential to balance these interconnected factors to ensure dependable switching and scalable integration.

2. Structure, dimensionality, ion migration, and single-crystal halide perovskites

Halide perovskites exhibit the ABX_3 crystal structure, characterized by a monovalent A-site cation, a divalent B-site metal, and halide anions that are positioned at the corners and faces of corner-sharing BX_6 octahedra.[25,26] The ionic lattice allows for significant compositional substitution and octahedral distortion, enabling easy transitions between fully connected three-dimensional networks and their lower-dimensional derivatives. This structural flexibility results in adjustable optical gaps, enhanced photocarrier mobility, and significant resistance to point defects, characteristics that are driving current interest in electronic and optoelectronic applications. The tolerance factor t and the octahedral factor μ determine the geometric compatibility within the perovskite lattice.[27,28] The tolerance factor connects the radii of the A-site cation and the halide, whereas the octahedral factor evaluates the sizes of the B-site metal and the halide.[29] Dimensional engineering has led to the development of two-dimensional (2D) and quasi-two-dimensional (quasi-2D) halide perovskites, characterized by inorganic layers interspersed with bulky organic spacer cations, commonly represented as $(RNH_3)_2A_{n-1}B_nX_{3n+1}$.[28,30,31] As the layer number n approaches infinity, the structure converges to the conventional three-dimensional (3D) phase, while n equals one results in a monolayer analog. Integer n values within these boundaries produce quasi-2D crystals that connect the dimensional continuum.[32–34] This method provides a flexible pathway for customizing thickness and composition, all while maintaining the essential BX_6 structure.[28,30]

Quantum confinement arises inherently in quasi-2D perovskites. Inorganic layers serve as quantum wells, while the organic layers function as barriers that create dielectric contrast. The spatial separation of carriers leads to an increase in Coulombic attraction, resulting in higher exciton binding energies.[35–37] These characteristics are beneficial for light-emitting and photonic applications, but they may pose challenges for charge separation in photovoltaics. Effective utilization thus necessitates a careful balance between quantum confinement and the channels for exciton dissociation. The perovskite lattice can be conceptually cleaved along the ⟨100⟩, ⟨110⟩, and ⟨111⟩ directions, resulting in distinct families of layered materials.[38–40] Within the ⟨100⟩ family, Ruddlesden–Popper phases feature alternating 2D perovskite sheets and organic bilayers, while Dion–Jacobson phases incorporate divalent spacers to align adjacent inorganic layers without lateral offset.[41–45] Removal aligned with ⟨110⟩ results in more intricate intergrowths, whereas sectioning along ⟨111⟩ generates structures characterized by high exciton binding energies that constrain photovoltaic efficiency. While synthetic advancements have expanded available phases, maintaining precise control over slab distortion, deep trap density, and spacer selection is crucial for optimizing device performance.

The electronic bandgaps in halide perovskites exhibit significant tunability *via* precise lattice substitution techniques. While altering the B-site metal directly changes the relative locations of the valence and conduction edges, replacing the A-site cation with bigger alkylammonium ions changes the covalency of the B–X bond.[46–48] Further modification is accomplished through the alteration of bond angles, the induction of octahedral tilts, or the application of lattice strain. The reduction of size to the nanoscale brings about quantum-confinement effects, which significantly expand the possibilities for tailored optoelectronic functions.[49–53] The dynamics of ion migration indicate minimal defect formation energies and shallow barriers to migration. The influence of external bias can reverse the polarity of photovoltaic devices, independent of their architecture or the chemistry of the precursors, emphasizing the significant impact of mobile species. In matrices with fewer constraints, the orientation of organic A-site cations collaborates to expand transport channels and affects hysteresis behavior.[54–56] Factors in the environment, including moisture, thermal cycling, and illumination history, influence these processes as aging occurs.

Single-crystal halide perovskites produced through slow cooling or inverse-temperature crystallization demonstrate significantly reduced point-defect concentrations and lack grain boundaries.[57,58] The improvement in lattice integrity extends carrier lifetimes, reduces trap-mediated recombination, and enhances the stability of emissive yield. The energy barrier for ion migration increases in the absence of light, and drift currents remain constrained even with prolonged bias applied. While migration cannot be eradicated, enhanced crystallinity minimizes the

presence of mobile ions, presenting a viable pathway for the development of long-lasting devices. In addition to optical tuning, large single crystals exhibit wider absorption onsets compared to polycrystalline films, thus broadening the range of the solar spectrum that can be harvested. Lower trap density enhances carrier transport efficiency, while extended diffusion lengths can counteract the recombination associated with greater thickness.[59,60] The collective advantages highlight the promise of single-crystal perovskites for advanced photovoltaics and various optoelectronic applications, contingent upon overcoming the challenges of scalable fabrication and integration. Expanding on these property–defect relationships, we subsequently choose a synthesis that reduces vacancy formation and regulates layer orientation, ensuring that crystal growth directly influences the ion-migration necessary for stable AI-scale switching.

3. Synthesis of single crystal halide perovskites

Inverse temperature crystallization presents a highly effective method for swiftly acquiring high-quality perovskite single crystals. The procedure is initiated with the regulated heating of a precursor solution. With rising temperatures, the solubility of the perovskite components decreases, leading the medium to approach a state of supersaturation.[61,62] Upon reaching a critical level of supersaturation, molecular clusters form as nuclei, which start the process of crystallization. Additional heating allows the arranging of dissolved species into a structured lattice, resulting in the growth of these nuclei into apparent crystals. Following sufficient growth, reducing the temperature ensures the stability of the product and inhibits excessive expansion.[63,64] This methodology takes advantage of the unique solubility characteristics of lead-halide perovskites in specific polar aprotic solvents, where solubility decreases instead of increasing with temperature. As a result, crystals form promptly once the solution exceeds the supersaturation limit. The growth of single crystals requires alignment of solvent properties and solubility characteristics. *N*,*N*-dimethylformamide (DMF), dimethyl sulfoxide (DMSO), and γ-butyrolactone (GBL) represent the most commonly utilized options for hybrid organic–inorganic compositions.[65–69] $MAPbBr_3$ crystallizes most effectively from DMF, $MAPbI_3$ demonstrates enhanced crystal quality in GBL, and $MAPbCl_3$ shows optimal growth in DMSO. The production of phase-pure single crystals adequate for advanced optoelectronic applications requires careful solvent selection and optimal thermal gradients. In contrast to slow evaporation or anti-solvent techniques, inverse temperature crystallization significantly accelerates growth time, minimizes defect density, and produces bulk crystals characterized by narrow rocking curves, all of which directly improve carrier mobility and the reliability of devices.

A slow cooling temperature is a practical approach for obtaining single crystals, as it allows the saturated precursor solution to exhibit reduced solubility with decreasing temperature. Peng *et al.*

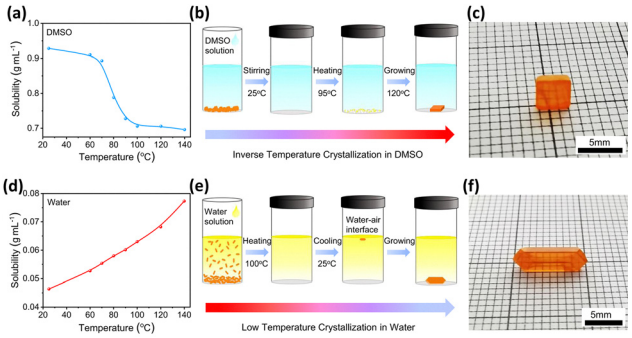

Fig. 1 (a) The solubility of $CsPbBr_3$ in DMSO varies with temperature. (b) Schematic representation of the inverse-temperature crystallization process in DMSO. (c) Optical image of the synthesized $CsPbBr_3$ single crystal. (d) The solubility of $CsPbBr_3$ in water is influenced by temperature. (e) A schematic illustration depicting the process of low-temperature crystallization in water. (f) Optical image of the synthesized $CsPbBr_3$ single crystal. Reprinted with permission.[70] Copyright 2021, Springer Nature.

have devised a strategy for low-temperature crystallization to cultivate $CsPbBr_3$ perovskite single crystals in an aqueous environment.[70] Fig. 1a illustrates the solubility of $CsPbBr_3$ as it varies with temperature in the optimized $CsBr:PbBr_2$ (1 : 2) DMSO precursor solution. A significant reduction is observed between 70 and 100 °C, with solubility decreasing from 0.9 g mL^{-1} to 0.7 g mL^{-1}. Fig. 1b illustrates the schematic layout of the inverse-temperature crystallization growth procedure performed in DMSO. Significantly, abundant $CsPb_2Br_5$ precipitates emerge when the solution temperature reaches 95 °C. As a result, an extra filtration step was added, leading to the growth of pure $CsPbBr_3$ single crystals at 120 °C with the aid of a small $CsPbBr_3$ seed. Fig. 1c displays a typical optical photograph of the DMSO-grown $CsPbBr_3$ crystals, showing a rectangular-prism morphology with a notable dimension exceeding 3 mm. Even with these initiatives, producing phase-pure, large-scale $CsPbBr_3$ crystals remains a significant challenge due to imbalanced stoichiometry, which encourages secondary nucleation. In contrast, Fig. 1d illustrates that in aqueous media containing HBr, the solubility of $CsPbBr_3$ decreases progressively with a reduction in temperature. The optimal precursor ratio of CsBr to $PbBr_2$ is set at 1 : 1 for aqueous growth, and the low-temperature crystallization strategy is depicted schematically in Fig. 1e. High-quality single crystals can emerge consistently when individual $CsPbBr_3$ seed crystals are placed at the bottom of the container. An optical image presented in Fig. 1f illustrates the aqueous-grown $CsPbBr_3$ crystals. A gradual cooling profile maintains a near-equilibrium state between dissolution and crystallization, thus promoting the growth of high-quality single crystals.

Also, Yuan *et al.* reported the controllable growth and fabrication of lead-free $MASnI_3$ perovskite single crystals utilizing an inverse-temperature crystallization method with GBL as the solvent.[71] A thorough examination of process parameters, such as precursor concentration, temperature ramp profile, and solvent composition ratio, enables the accurate adjustment of nucleation and crystal growth kinetics, ensuring dependable scalability.

The quantitative analysis reveals the unique solubility behavior of $MASnI_3$ in GBL. The verification of high experimental reproducibility follows, using the unique solubility profile and the process of inverse-temperature crystallization. The repeated use of a space-confinement technique results in the preparation of $MASnI_3$ single-crystal thin films with micron-scale thickness, which is considered optimal for the efficiency of tin perovskite solar cells. The $MASnI_3$ single-crystal thin films demonstrate distinct single-crystalline characteristics, featuring significant optical absorption with a clear band-edge onset, phase-pure X-ray diffraction patterns, and no detectable Sn(IV) signatures in X-ray photoelectron spectra.

Also, Yu *et al.* demonstrated that the steady-state inverse-temperature crystallization method has been developed to precisely regulate the growth process of single crystals by controlling the growth speed, resulting in a constant growth rate as the temperature increases.[72] Fig. 2a demonstrated that, following the conventional inverse-temperature crystallization protocol, the solution temperature typically rose at a steady rate of approximately 0.5 °C h^{-1} during this experiment. However, since the speed of crystal growth is influenced by temperature, ensuring a consistent heating slope resulted in an uneven rate of single-crystal growth. As a result, the dynamics of crystallization were adjusted to achieve steady-state growth, ensuring that the expansion of crystals occurred at a consistent rate during the entire growth cycle. By employing this strategy, growth speeds obtained through conventional inverse-temperature crystallization and the inverse-temperature crystallization method were summarized in Fig. 2b. Growth rates were calculated by graphing volume against time and differentiating the resulting curve at consecutive temperature checkpoints. This methodology yielded quantitative evidence indicating that the inverse-temperature crystallization method exhibited quasi-linear kinetics, whereas the conventional inverse-temperature crystallization demonstrated significant acceleration. The concentration of the solution consistently decreased as the temperature increased while the rate of crystal growth intensified, illustrating the influence of temperature on the dynamics of crystallization. To clarify the growth behavior in greater detail, nucleation and solubility diagrams of $MAPbBr_3$ were illustrated in Fig. 2c, dividing the concentration–temperature domain into unsaturated, stable, and unstable regions. Identifying the operational route within the stable window required a careful equilibrium between supersaturation and thermal driving force. Deviations into the unstable field-initiated burst nucleation, resulting in increased defect densities and destroying optical clarity. In the unsaturated region, the solution remained below saturation levels, effectively preventing nucleation; any temporary nuclei or crystals quickly dissolved.

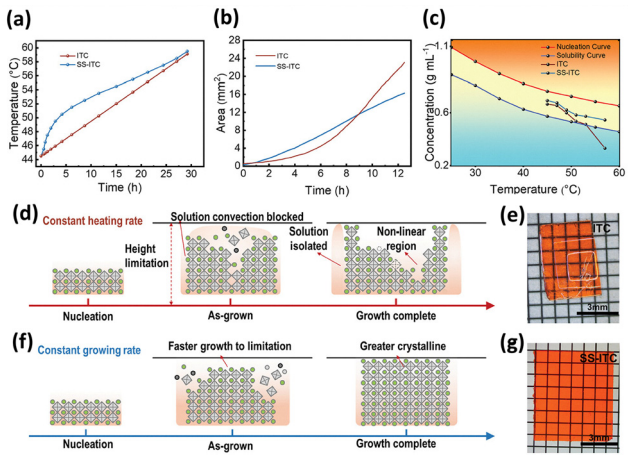

Fig. 2 (a) The temperature–time profile associated with the process of crystal growth. (b) The rate of growth of single crystals grown using the inverse-temperature crystallization method and the steady-state inverse-temperature crystallization method. (c) The nucleation curve alongside the solubility curve of $MAPbBr_3$ in DMF solvent. (d) The diagram illustrates the distinctions using inverse-temperature crystallization methods. (e) The images of single crystals were cultivated using the inverse-temperature crystallization method. (f) The diagram illustrates the distinctions using steady-state inverse-temperature crystallization methods. (g) The images of single crystals cultivated using the steady-state inverse-temperature crystallization method. Reprinted with permission.[72] Copyright 2024, Wiley-VCH GmbH.

In contrast to traditional inverse-temperature crystallization, the steady-state protocol maintains the solution within a stable region throughout the growth process, which is essential for producing high-quality crystals. Inconsistencies in crystal quality were explained by comparing the nucleation and growth routes for inverse-temperature crystallization, as illustrated schematically in Fig. 2d and f. Ring-like textures observed in specimens grown through inverse-temperature crystallization resulted from temporal fluctuations in growth velocity, leading to the development of non-linear expansion zones. At the same time, the depletion of solute around the growing crystals limited the expansion in their central areas. In contrast, the inverse-temperature crystallization method ensured meticulously controlled growth rates, thereby preventing the formation of non-linear domains. As a result, crystals grew uniformly after nucleation, and a higher initial heating rate accelerated supersaturation, enabling specimens to reach the vertical limit swiftly and avoid non-linear patterns. Fig. 2e and g illustrate photographic comparisons of crystals generated through the inverse-temperature crystallization technique and the inverse-temperature crystallization method, respectively. Examination revealed no significant difference in size between the crystals generated by the two methods.

The process of anti-solvent crystallization offers a straightforward method for producing large perovskite single crystals. The method takes advantage of the differences in solubility between the growth solvent and a volatile anti-solvent by carefully controlling vapor diffusion; the liquid composition within the vessel is gradually altered until supersaturation occurs and nuclei begin to form.[73–75] Following this, an influx of vapor allows a gradual decrease in solubility, enabling several nuclei to develop into centimeter-scale bulk crystals. This approach offers a significant benefit due to its limited dependence on thermal control. In contrast to inverse-temperature crystallization, the evolution of crystals in this method is predominantly influenced by mass transfer rather than heating. As a

result, the processes become more straightforward in terms of reproducibility and scaling, as the need for precise temperature control, specialized devices, and significant thermal gradients is eliminated. Consistent crystal quality can thus be attained under ambient or only slightly elevated temperatures.

Qin reported the synthesis of a $CsPbBr_3/Cs_4PbBr_6$ composite material featuring a hexagonal tower structure, achieved through a rapid anti-solvent vapor-assisted technique.[76] The methylene chloride acts as an anti-solvent, volatilizing at approximately 40 °C when heated and subsequently entering the precursor solution in a gaseous form. The solubility of cesium, lead, and bromide ions in methylene chloride is significantly lower compared to their solubility in DMF. When the DMF solution is combined with dichloromethane, the $CsPbBr_3/Cs_4PbBr_6$ composite material precipitates from the mixed solution. The duration of this reaction process ranges from 3 to 10 min, contingent upon the volatilization temperature. During the anti-solvent vapor-assisted experiment, the introduction of anti-solvent vapor into the precursor solution induces a localized change in solubility near the gas molecules. This rapid alteration leads to significant precipitation, allowing for uniform crystallization of the material within a brief period, ultimately yielding a composite material with excellent dispersion.

Also, Ding *et al.* introduced a strategy for regulating crystallization kinetics aimed at the mass production of thin $Cs_3Bi_2Br_9$ platelet single crystals through an anti-solvent-mediated cooling crystallization method.[77] $Cs_3Bi_2Br_9$ single crystals produced *via* the conventional slow-cooling crystallization method, without the use of ligands or spatial confinement, exhibited polyhedral geometries. A protocol for additive-mediated slow-cooling crystallization was established to modulate kinetic parameters, resulting in the successful production of thin $Cs_3Bi_2Br_9$ single crystals. The additive-mediated slow-cooling crystallization strategy successfully produced batch-scale platelike $Cs_3Bi_2Br_9$ crystals characterized by uniform morphology, significant lateral dimensions, and a notably shortened preparation time. Thin $Cs_3Bi_2Br_9$ crystals appeared 3 s following the injection of the anti-solvent in Fig. 3a. An image obtained through scanning electron microscopy (SEM) displayed a platelet with a smooth surface, measuring approximately 152 μm in lateral dimension and around 1.5 μm in thickness Fig. 3b. The energy-dispersive X-ray spectroscopy (EDS) mapping and spectra presented in Fig. 3b validate the uniform distributions of Cs, Bi, and Br, as well as the anticipated stoichiometry of $Cs_3Bi_2Br_9$. The X-ray diffraction (XRD) patterns for polyhedral $Cs_3Bi_2Br_9$ grown by conventional slow cooling crystallization and platelet crystals produced by additive-mediated slow-cooling crystallization are shown in Fig. 3c. Each reflection corresponds to the characteristic $Cs_3Bi_2Br_9$ peaks, demonstrating impurity-free crystal growth. Reflections aligned with the {001} facets of the thin platelets displayed remarkably intense signals, indicating a pronounced crystallographic orientation. The selected-area electron diffraction (SAED) pattern, as shown in Fig. 3d, exhibits clearly defined hexagonal spot sets, confirming the single-crystal nature and outstanding crystallinity.

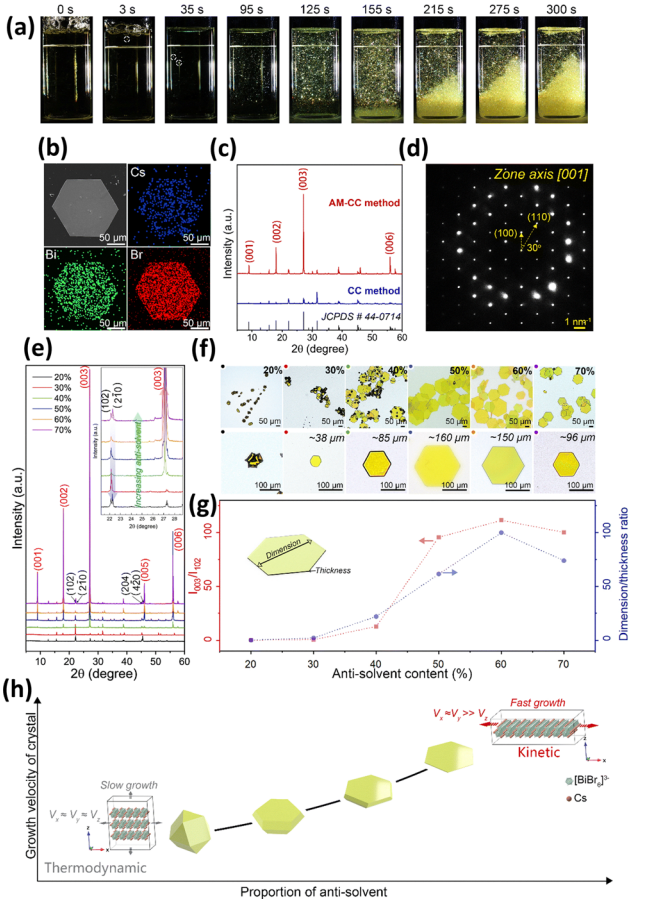

Fig. 3 (a) Images recording the reaction process following the injection of anti-solvent throughout 300 s. (b) SEM and EDS mapping images of $Cs_3Bi_2Br_9$ platelets are presented. (c) The XRD pattern of the $Cs_3Bi_2Br_9$ polyhedra and $Cs_3Bi_2Br_9$ platelets is presented. (d) Selected area electron diffraction pattern of a thin $Cs_3Bi_2Br_9$ platelet. (e) XRD patterns and (f) optical images of $Cs_3Bi_2Br_9$ platelets have been obtained and analyzed. (g) Correlation of intensity ratio I_{003}/I_{102}, dimensions/thickness of the $Cs_3Bi_2Br_9$ platelets, and the proportion of anti-solvent. (h) Schematic representation illustrates growth behavior influenced by the regulation of crystallization kinetics. Reprinted with permission.[77] Copyright 2025, The Royal Society of Chemistry.

The growth of reduced-dimensional lead-free metal halide perovskite *via* additive-mediated slow-cooling crystallization was systematically examined, focusing on the effects of the proportion and identity of the anti-solvent on crystal morphology. The XRD pattern shown in Fig. 3e demonstrated a progressive increase in the relative intensity of {001} reflections as the anti-solvent content increased. Concurrently, thin hexagonal platelets emerged gradually, with their lateral dimensions expanding in Fig. 3f. The morphological evolution shows in Fig. 3g, where the dimension-to-thickness ratio reaches its maximum at approximately 100. As shown in Fig. 3f, the lower formation energy of $Cs_3Bi_2Br_9$ crystal facets oriented perpendicular to the *z*-axis resulted in the introduction of an anti-solvent, which created a rapid crystallization kinetic driving force. This immediately increased growth velocities along the *x* and *y* directions, ultimately leading to the formation of

$Cs_3Bi_2Br_9$ platelets. The additive-mediated slow-cooling crystallization synthesis demonstrated that a high anti-solvent fraction contributed to an accelerated kinetic factor, promoting the growth of larger, thinner $Cs_3Bi_2Br_9$ platelet single crystals. Batch reproducibility was confirmed through various preparations, and the optical clarity of the resulting platelets was found to be appropriate for optoelectronic characterization.

In solution-based methods, the production of single crystals typically involves the gradual evaporation of the solvent from a precursor. As molecules transition from the liquid phase, the concentration of solute increases until the point of supersaturation is achieved, leading to the formation of nuclei. The gentle warming of the solution can enhance evaporation, a notion similar to inverse temperature crystallization. However, the solubility profile in an evaporation-driven scheme remains lower than that observed in inverse temperature crystallization. The growth rate is determined by the intricate balance between the supply and removal of solvent, requiring precise control over temperature, airflow, and vessel geometry to achieve uniform large crystals. It is essential to choose a solvent that dissolves the halide salts to a moderate extent without excessive dissolution. An intermediate affinity solvent enables gradual supersaturation, inhibits spontaneous nucleation, and promotes a continuous layer-by-layer addition process, resulting in centimeter-scale perovskite single crystals.

With the resulting single crystals available, the device layout and dielectric/contact selections are determined to align fields and minimize ionic screening, effectively converting crystal quality into the FET metrics that dictate AI inference efficiency (threshold stability, subthreshold slope, ON/OFF ratio, and mobility).

4. Performance parameters of perovskite FETs

A FET operates as a three-terminal device that utilizes an applied electric field to guide charge through a semiconductor system, serving as a fundamental component of contemporary electronics. The architecture features a gate electrode, accompanied by source and drain contacts, with a thin semiconductor film connecting these contacts and a gate dielectric that ensures electrical isolation of the gate while maintaining control over the channel. When appropriate voltages are applied to the gate (V_{GS}) and drain (V_{DS}), the gate potential reorganizes carriers within the channel, thus controlling the current flow between the source and drain.[78,79] Two fundamental layout families prevail in the fabrication practices of contemporary manufacturing. In floated configurations such as top gate bottom contact and bottom gate top contact, the semiconductor is positioned between the dielectric layer and the metallic electrodes. The substantial overlap reduces contact resistance and significantly enhances drive current across various levels. Coplanar formats such as bottom gate bottom contact and top gate top contact position the dielectric on the same side of the semiconductor as the electrodes, thus simplifying the lithography process.[80,81] However, this geometry frequently results in an uneven charge density near the channel, where Schottky barriers typically form. The presence of unwanted capacitance due to gate overlap can reduce the apparent mobility and interfere with switching speeds. The process of selecting a layout requires optimal electrical performance, such as ease of manufacturing, cost efficiency, yield, and scalability. Floated designs enhance carrier injection, whereas coplanar configurations integrate seamlessly with conventional patterning techniques.

Coplanar layouts provide a straightforward approach for scaling across extensive substrates, as they align seamlessly with existing lithography, printing, and encapsulation processes, while accommodating web handling for flexible foils. Floated architectures offer enhanced contact injection; however, they typically necessitate more precise alignment and multilayer stacking, which can complicate yield and reliability when subjected to bending in comparison to planar methods. Vertical transistors present an intriguing combination of density and short-channel control. However, they depend on precise thickness management and conformal patterning of stacked electrodes. This positions them as promising candidates for specialized high-performance pixels and neuromorphic tiles, though they are not yet fully prepared for roll-to-roll or panel-level manufacturing. Electrical factors significantly influence overall throughput, requiring attention to mechanical alignment and backend compatibility. The biases applied to the gate and drain collaboratively establish the electric-field distribution throughout the channel, which in turn influences the behavior of the FET.[82–84] As V_{GS} exceeds a certain threshold, carriers accumulate at the semiconductor–dielectric interface, and their surface density corresponds to the gate overdrive level. If V_{GS} remains beneath that threshold, the channel does not possess carriers and stays inactive.[85–87] The onset voltage indicates the threshold at which the drain current surpasses the inherent noise level. The subthreshold slope indicates the rate at which current transitions from OFF to ON, thus reflecting the overall interface trap density and the capacitance of the gate insulator. The ON/OFF current ratio measures the extent to which the conductive state exceeds leakage, serving as a crucial indicator of device reliability.[88,89] The strength of coupling is influenced by the thickness of the oxide and its breakdown field, while the channel length can range from a few micrometers to several hundred. Broad channels produce quantifiable current for preliminary evaluation.[90–92] High permeability oxides or polymer insulators enable the use of thinner gate films and lower operating voltages; however, they also present challenges concerning interface dipoles and long-term thermal endurance. The selection of electrode material has a significant impact on the final electrical performance and stability metrics of the device. The use of evaporated gold in p-type transport aligns with the valence band, facilitating hole flow, while alternative metals adjust their energy levels to achieve n-type or ambipolar conduction. Silver (Ag), nickel (Ni), and titanium (Ti) show instances where the band alignment is adjusted to favor

electrons or effectively balance both types of carriers.[93–95] Even metals considered inert can chemically react at the perovskite surface when subjected to bias or illumination, leading to the formation of interfacial compounds or experiencing halide corrosion. This ongoing evolution progressively modifies injection barriers during extended operation. Monolayers designed on bottom contact electrodes can efficiently adjust work function without changing the bulk metal; however, this method is significantly less accessible in top contact configurations. A dual-gate platform enables distinct potentials above and below the channel, allowing for precise tuning of carrier density, which enables the selection of electron or hole flow as needed for adaptable circuits.[96–98] Opposite-polarity voltages applied to the two gates enable the coexistence of different carrier types within a single channel, a crucial characteristic for complementary logic constructed from a semiconductor layer. The formulation of dielectrics plays a crucial role in determining the reliability of devices, particularly in terms of breakdown strength and stability. A polymer insulator applied directly onto perovskite effortlessly adheres to surface irregularities, providing effective protection against unwanted ambient moisture for the grains. The process of atomic layer deposition for oxide dielectrics offers enhanced breakdown strength and sustained lower leakage, contingent upon maintaining gentle processing temperatures and chemicals suitable for the sensitive perovskite interface.[99,100] The capacitance of the gate insulator determines the effective bias window, and any charge that becomes trapped at the interface alters the threshold, making it challenging to evaluate mobility with precision and comprehensiveness. Mobile ions serve as a notable and enduring contributor to hysteresis and general temporal drift in devices. These species fully modify channel conductance and modify local potentials at electrodes, subsequently leading to variations in injection barrier height. Maintaining control over ion motion through composition tuning, passivation, or encapsulation is essential for achieving stability in large-area arrays.

In addition to reducing uncontrolled drift, single-crystal perovskite FETs can be tailored to harness subtle, field-programmable ionic redistribution at specifically designed interfaces. This capability allows for conductance updates and synaptic weighting akin to transistors, which are enabled by electrical or optical pulses. By combining defect-lean lattices with asymmetric contacts and dual-gate field profiles, the same architecture can alternate between stable switching and reconfigurable analog states, establishing these devices as viable components for AI-ready neuromorphic hardware. The subsequent case studies in 3D single-crystal FETs exemplify these design principles, showing how surface chemistry and contact energetics transform material and layout selections into consistent performance at room temperature.

5. 3D single-crystal halide perovskite FETs

Recent advancements in crystal engineering and interface design have sparked renewed interest in 3D halide perovskite single-crystal FETs. This section provides the essential strategies and performance metrics that helped achieve stable, low-hysteresis operation in 3D perovskite single-crystal FETs. She *et al.* revealed that a three-step, solution-driven approach for surface cleaning and passivation effectively reduced ionic defect populations at halide perovskite $MAPbI_3$ surfaces, all while preserving the integrity of the crystal lattice.[101] The process began with an initial rinse that removed loosely attached defective components, followed by a healing phase that maintained the film's surface structure while allowing ionic vacancies to recombine and ended with a final rinse. The carrying out of the trilogy in a *tert*-amyl alcohol/cyclohexane co-solvent achieved an optimal balance of polarity. The relevant precursors and ionic impurities maintained adequate solubility to migrate toward or away from the interface. At the same time, the extraction of methylammonium or iodide, in addition to slow dissolution–recrystallization dynamics that could compromise the lattice, was effectively avoided. The treatment effectively inhibited ionic defect migration and produced FETs that exhibited minimal hysteresis in both p-type and n-type operating modes. Following electrical characterization revealed that threshold voltages shifted by less than 1 V during extended bias cycling in ambient humidity, emphasizing the chemical durability provided by the surface protocol across numerous cycles. The further refinement of contact resistance and grain morphology presents a promising opportunity for achieving additional performance enhancements. The devices using this approach demonstrated n- and p-type mobilities of 3.0 $cm^2\ V^{-1}\ s^{-1}$ and 1.8 $cm^2\ V^{-1}\ s^{-1}$, respectively, at 300 K; additionally, n-type transport achieved 9.2 $cm^2\ V^{-1}\ s^{-1}$ at 80 K.

Also, Senanaya *et al.* clarified the sources of operational instabilities and developed a feasible approach to address them, resulting in $RbCsFAMAPbI_3$ FETs that demonstrate minimal hysteresis, stable threshold voltages ($\Delta V_{th} < 2$ V over 10 hours of continuous operation), and room-temperature mobilities exceeding 1 $cm^2\ V^{-1}\ s^{-1}$, which provides exceptional electronic performance.[102] The integration of various A-site cations, such as strain-relieving Cs and passivation-focused Rb, proves to be an effective strategy for reducing vacancy populations and limiting ion migration in perovskite FETs. This approach enhances operational stability and charge transport when subjected to electric stress. Furthermore, subjecting the perovskite layer to positive-azeotrope solvent treatments that act as Lewis bases or acids significantly reduces defect density. It dramatically enhances both performance and long-term stability for n-type or p-type perovskite electronic devices functioning in ambient conditions.

Zhou *et al.* presented a method for polymer grain-boundary passivation that effectively managed harmful ion migration in methylammonium lead iodide $MAPbI_3$ FETs.[103] The chosen additive, polycaprolactone, effectively passivated $MAPI_3$ boundaries, resulting in a significant reduction of hysteresis in the transistor transfer curves compared to pristine $MAPbI_3$ devices prepared under the same conditions. Furthermore, the addition of polycaprolactone enhanced the ON/OFF ratio to 50 and the mobility to 3×10^{-3} $cm^2\ V^{-1}\ s^{-1}$ at a loading concentration of 1 mg mL^{-1}, whereas the untreated transistors exhibited

values of 40 and 1 × 10^{-3} cm^2 V^{-1} s^{-1}. At the maximum concentration of polycaprolactone, measured at 4 mg mL^{-1}, the $MAPbI_3$ transistor exhibited the least amount of hysteresis. It even showed potential for ambipolar transport, differing from the dominant n-type charge-carrier behavior observed in the control group of pristine devices. The results corresponded to the successful reduction of iodide ion migration and simultaneous passivation of boundary-associated traps by polycaprolactone. This was supported by an observed increase in the measured activation energy (E_a) for ion motion following the incorporation of the additive, accompanied by improved photoluminescence emission intensity and an extended decay lifetime.

Also, Zou *et al.* outlined a method for constructing high-performance perovskite FETs that functioned at room temperature, utilizing a Schottky junction formed between a monolayer-graphene source contact and a $MAPbBr_3$ microplate.[104] Fig. 4a and b illustrate pseudo-color images of the microplates, each with a thickness of 3.88 μm. The images demonstrate an exceptionally smooth surface and a well-defined perimeter. Fig. 4c illustrates the architecture of the device. In this structure, the graphene layer served as the bottom source electrode, directly interfacing with the perovskite active layer, while an Au film operated as the top drain electrode. The output curves presented in Fig. 4d were collected at various gate voltages, illustrating effective gate control. The transistor exhibited ambipolar transport due to the presence of a gate-tunable Schottky barrier situated between the graphene electrode and the perovskite lattice, which assisted the dynamic regulation of carrier-injection barriers *via* electrostatic gating. The operating principle has been explained through the energy-band alignment depicted in Fig. 4e. Graphene exhibited a work function

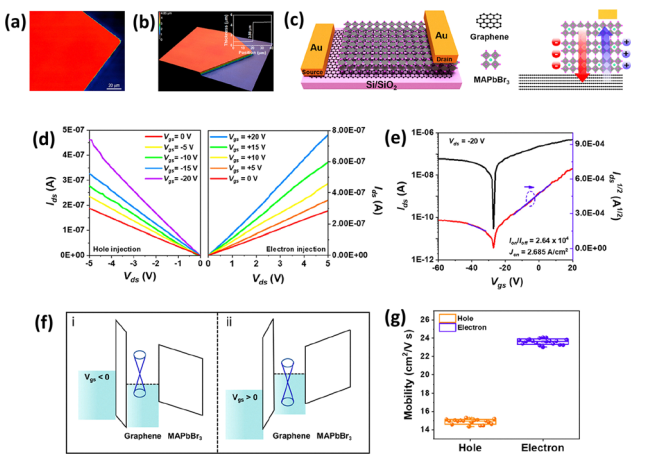

Fig. 4 (a) Pseudocolor plot and (b) 3D pseudocolor plot of the $MAPbBr_3$ microplate. The thickness is 3.88 μm. (c) Schematic illustration of the FET based on $MAPbBr_3$ microplates. (d) The output characteristics under different gate biases. (e) The band structure under (i) negative gate voltage and (ii) positive gate voltage at zero drain–source bias. (f) The transfer characteristics. (g) The statistics of carrier mobilities of 20 devices. Reprinted with permission.[104] Copyright 2022, American Chemical Society.

that could be adjusted around its charge-neutrality point. Due to the weak electrostatic shielding and low state density of graphene, the barrier height at the graphene–perovskite interface exhibited significantly greater sensitivity to gate bias compared to the barrier at the Au–perovskite interface located above. With negative gate bias applied, holes were collected at the graphene/perovskite interface, causing a downward shift in the graphene Fermi level. This shift led to a decrease in the hole-injection barrier, resulting in a significant negative, hole-dominated drain current. On the other hand, applying a positive gate bias elevated the graphene Fermi level, creating a significant barrier to hole movement and facilitating electron injection; as a result, the direction of the drain–source current changed. This adjustable Schottky barrier demonstrated significant improvements in the ON/OFF ratio and current density. The FET displayed a U-shaped transfer curve with clear p-type and n-type branches at varying V_{GS}, as illustrated in Fig. 4f, thus confirming its ambipolar behavior. During the sweep of V_{GS} from −60 V to −27 V, with the drain–source voltage V_{DS} held constant at −20 V, the device exhibited a clear transition between off and on states, achieving an ON/OFF ratio of 2.64 × 10^4 and a current density of 2.69 A cm^{-2}. Fig. 4g presents a summary of the statistical mobility distribution derived from 20 identically processed FETs. The saturation mobilities were measured at 23.39 cm^2 V^{-1} s^{-1} for electrons and 14.93 cm^2 V^{-1} s^{-1} for holes. Regardless of whether the transistor was biased into an n-channel or p-channel window, the exceptional field-effect metrics were traced to two factors. The drain-to-source electric field was oriented parallel to the gate-induced field, significantly reducing ion-migration effects.

Yang *et al.* reported that the epitaxial synthesis of all-inorganic halide perovskite $CsPbBr_3$ single crystals was achieved under near-ambient conditions through a simple yet controlled solution method.[105] Two representative crystalline substrates, $SrTiO_3$, and mica, serve as lattice templates for growth, corresponding to ionic epitaxy and van der Waals epitaxy, respectively. The process of epitaxial deposition of $CsPbBr_3$ single crystals on both layers occurs within a space-confined geometry. In this environment, a supersaturated precursor film gradually transforms into the perovskite phase, all while minimizing convective flow. Micrographs obtained from optical microscopy (Fig. 5a) and scanning electron microscopy (SEM, Fig. 5b) show that the crystals grown on $SrTiO_3$ display mirror-flat facets and lateral dimensions nearing several hundred μm, a scale that is advantageous for device integration. The delineated rectangular shape directly illustrates the cubic symmetry that is intrinsic to the $CsPbBr_3$ lattice. High-resolution atomic force microscopy (AFM, Fig. 5c) provides additional confirmation of a pristine, even, and uniform surface with a root-mean-square roughness of ≤1 nm, demonstrating the exceptional quality of the sample and the remarkable uniformity of thickness across the terrace. Thermal evaporation was employed to deposit Ti/Au source–drain contacts onto the $CsPbBr_3$ crystal. This was succeeded by the application of a 250 nm poly(methyl methacrylate) (PMMA) film, which serves as the gate dielectric while maintaining the epitaxial alignment

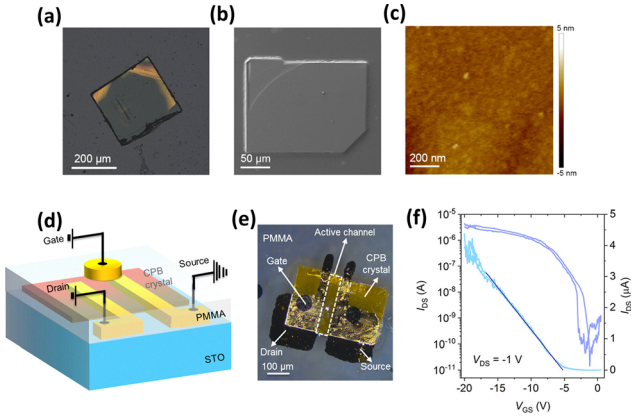

Fig. 5 (a) Optical image depicting the CPB single crystal, characterized by a regular rectangular shape, positioned on the $SrTiO_3$ substrate. (b) Top-view SEM image of the $CsPbBr_3$ single crystal. (c) Tapping-mode AFM topography imaging reveals the smooth and uniform surface of the epitaxially grown single crystal. (d) Diagram illustrating the structure of the FET. (e) Top view of the FET device utilizing a $CsPbBr_3$ single crystal, incorporating PMMA as the gate dielectric. (f) Dual-sweep transfer curves of the FET at a source–drain voltage of −1 V. Reprinted with permission.[105] Copyright 2021, American Chemical Society.

with the underlying $SrTiO_3$ support (Fig. 5d). A Ti/Au stack was subsequently utilized as the gate electrode, carefully deposited on the PMMA layer. Fig. 5e presents a detailed top-view optical micrograph of the completed FETs, showing an active channel length (L) of 50 μm and a channel width (W) of 300 μm, dimensions that effectively balance current drive and parasitic resistance. Fig. 5c presents dual-sweep transfer curves, specifically the source–drain current (I_{DS}) as a function of the gate voltage (V_{GS}) obtained from the $CsPbBr_3$ single-crystal device, which operates within a stable p-type transport regime. The outstanding electrical performance is attributed to atomically coherent epitaxy, which produces crystals free of threading dislocations or planar faults that could serve as deep centers. The transfer characteristics show minimal hysteresis, a trait that has been consistently documented but rarely addressed in the context of solution-processed halide perovskite electronics. Fig. 5f demonstrates that the hysteresis observed during extensive continuous and cyclic operation at room temperature for each $CsPbBr_3$ single-crystal FET is insignificant, even when subjected to bidirectional gate bias. Ion migration, caused by vacancy or interstitial defects, serves as the primary mechanism that induces hysteresis, which partially shields the gate electric field. This results in moderate field-effect mobility and constrained operational stability in halide perovskite FETs.

Bruevich *et al.* reported the intrinsic charge conduction regime in lead halide perovskite FETs, showing a transport landscape that had previously been obscured by defect-mediated scattering.[106] This significant development arises from three synchronized advancements. Initially, the enhanced vapor-phase epitaxy method yields extensive single-crystal $CsPbBr_3$ films characterized by atomically smooth terraces and remarkably low levels of structural defects and electronic traps, specifically within the range that influences device performance. Additionally, thin film and surface diagnostics, such as X-ray diffraction and photoelectron spectroscopy, validate the exceptional chemical purity and crystallographic order of the material. Also, perfect trap-free transistors exceeded all previous performance benchmarks. These devices enable direct assessments of intrinsic FET and gated Hall mobilities as they relate to temperature variations. As the temperature decreases, the mobility increases from approximately 30 $cm^2\ V^{-1}\ s^{-1}$ under ambient conditions to around 250 $cm^2\ V^{-1}\ s^{-1}$ at 50 K, distinctly showing band-like transport constrained by phonon scattering.

Zhou *et al.* demonstrated that a FET constructed from a $CsPbBr_3$ microplatelet through van der Waals epitaxial growth, where a monolayer graphene substrate acted as the source contact and established a vertical Schottky junction.[107] Fig. 6a presents a schematic representation of the vertical device. In this configuration, the SiO_2 layer on the silicon wafer served as the gate dielectric, allowing the applied gate potential to effectively penetrate the graphene and modulate charge populations within the $CsPbBr_3$ crystal. The graphene served as both the source and drain electrodes: one section stayed on the basal graphene sheet. In contrast, another section was positioned on the $CsPbBr_3$ microplate, creating a vertical stack with the gate bias vector in a line parallel to the drain–source bias vector. Fig. 6b and c present optical microscopy images of the 3.88 μm thick microplate acquired prior to and following Au deposition. The photographs demonstrated that the evaporated metal on the $CsPbBr_3$ surface was positioned on a plane separate from that of the graphene substrate, thus validating the intended step geometry. A cross-sectional SEM was recorded after metal

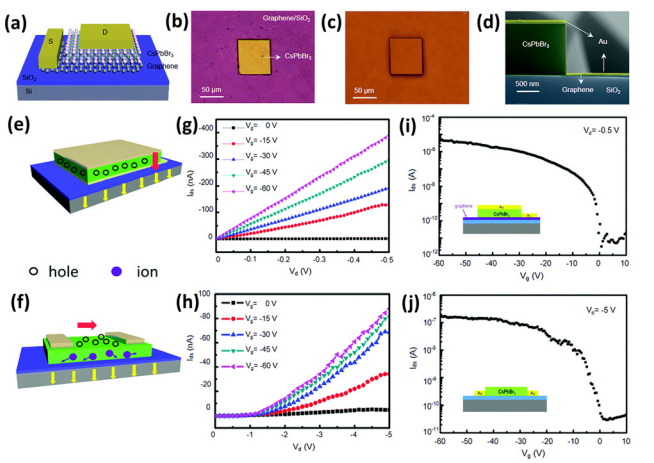

Fig. 6 (a) A schematic illustration of the vertical transistor using $CsPbBr_3$. (b) Optical image showing a typical $CsPbBr_3$ single-crystal that has been grown on a graphene substrate through the process of van der Waals epitaxy. (c) Optical image of the $CsPbBr_3$ single-crystal following the thermal evaporation of metal electrodes. (d) Cross-sectional SEM image of $CsPbBr_3$ following thermal evaporation. Carrier transport diagrams for (e) vertical and (f) planar transistors, respectively. Output characteristics of (g) vertical transistors and (h) planar transistors. Transfer characteristics of (i) vertical transistors and (j) planar transistors. Reprinted with permission.[107] Copyright 2020, The Royal Society of Chemistry.

evaporation to rigorously verify the deposition strategy, as shown in Fig. 6d. A typical cuboid associated with the single crystal was observed, enveloped by a thin metallic layer, with an additional layer of the same metal also applied to the substrate. Fig. 6e illustrates that the conductive channel length matched the thickness of the $CsPbBr_3$, and this exceptionally short pathway provided the device with swift response and field-effect characteristics. The issue of ion migration, typically a concern in perovskite electronics, was low in this instance due to the alignment of the gate field and the drain–source field in the same direction. Conversely, planar transistors experience gate screening due to the movement of ions, as illustrated in Fig. 6f. The output characteristics illustrated in Fig. 6g revealed that the drain–source current I_{DS} increased as the gate voltage V_{GS} became more negative, signifying p-type majority transport. The significant variation of I_{DS} with V_{GS} demonstrated remarkable gate modulation. Fig. 6i illustrates that the ON/OFF ratio exceeded 10^6 at room temperature, exceeding similar MoS_2 devices by approximately one to 2 orders of magnitude. The measured planar channel length was 20 μm, significantly exceeding that of the vertical counterpart. At a drain bias of −0.5 V, the planar output curve depicted in Fig. 6h exhibited a nearly flat response. Even when V_{DS} was increased to −5 V, substantial current was observed only with considerable gate swings, resulting in an ON/OFF ratio of only 5×10^3, which is approximately three decades lower than that of the vertical device. Fig. 6j presents the transfer curve of the planar transistor obtained at V_{DS} = −5 V. As V_{GS} approached −40 V, the current steadily reached a saturation point. The current density measured was 0.01 A cm^{-2} at V_{DS} = −5 V and V_{GS} = −60 V, which is 3 orders of magnitude lower than that observed in the vertical configuration.

Halide perovskites exhibited exceptional optical characteristics that were utilized in the development of phototransistors with improved responsiveness. Nonetheless, the constraints of limited current modulation at ambient temperature, significant environmental sensitivity, a lack of dependable patterning techniques, and moderate carrier mobility have impeded advancements in perovskite phototransistors. This has resulted in experimentation being confined mainly to rigid silicon or glass platforms, where improv ed morphological quality could be guaranteed in advance. Khorramshahi *et al.* recorded the modulation of ambient temperature currents in $MAPbI_3$ phototransistors.[108] The resulting phototransistor used a top-gate architecture with a lateral drain-channel-source arrangement. Phototransistor functioned in both linear and saturation regimes in the absence of light and under white illumination, producing varying current ranges that corresponded to the specific optical excitation conditions applied. The transistor demonstrated p-type transport characteristics, with an estimated field-effect mobility of approximately 1.7×10^{-3} cm^2 V^{-1} s^{-1}.

Driven by the existing constraints in 3D lattices, utilize layered 2D single crystals, where the dielectric confinement and spacer-cation manipulation enhance ionic activation barriers, allowing lower-voltage, memory-compatible AI circuits.

6. Layered 2D single-crystal halide perovskite FETs

Layered 2D halide perovskite single crystals present an appealing alternative to their 3D, showing enhanced dielectric confinement, superior moisture and thermal durability, and significantly reduced ion migration. The implementation of these features results in reduced hysteresis and enhanced bias stability, which together expand the functional range for low-power, high-gain FETs. The following section emphasizes the essential synthetic approaches and device designs that take advantage of these benefits to realize millimeter-scale 2D perovskite FETs with competitive electronic performance.

Ulaganathan *et al.* reported the growth of phase-pure, millimeter-scale, 2D $(BA)_2FAPb_2I_7$ single crystals using a slow-evaporation, constant-temperature solution method.[109] Fig. 7a depicts the FET fabricated from a single crystal and exposed to a 488 nm laser. The I_{DS} was observed under a constant V_{DS} in both dark and illuminated conditions; as illustrated in Fig. 7b, the current exhibited a linear increase with rising photon flux. Fig. 7c demonstrates the relationship between the extracted photocurrent and the incident laser power (P), whereas Fig. 7d shows the responsivity (R_λ) measured at 488 nm. A peak R_λ of approximately 5.0 A W^{-1} at 3.5 μW was attained without implementing any supplementary sensitization strategy.

Adjusting the back-gate voltage (V_{BG}) proved to be a significant tool for further improvement. As V_{BG} was varied from 0 to +120 V, there was a substantial increase in R_λ, reaching 63 A W^{-1}. Fig. 7e illustrates transfer curves obtained within the range of −80 V to +120 V, showing a significant increase in channel current with positive gating. This behavior confirmed n-type conduction and validated that electrons acted as the predominant carriers within the $(BA)_2FAPb_2I_7$ lattice. Fig. 7f illustrates the progression of R_λ about gate bias, demonstrating a steady increase from 3.8 A W^{-1} at 0 V to 63 A W^{-1} at +120 V.

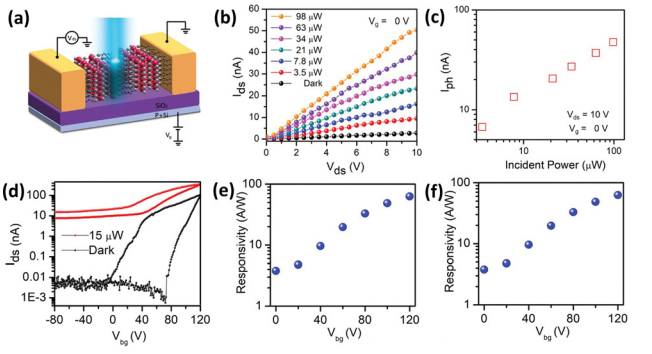

Fig. 7 (a) A schematic illustration of the $(BA)_2FAPb_2I_7$ FET device is presented. (b) I_{DS}–V_{DS} curves were measured in the absence of light and during laser exposure at varying intensities. (c) The relationship between irradiance and photocurrent of the device. (d) Responsivity is a function of illumination intensity that ranges from 3.5 to 98 μW at a wavelength of 488 nm. (e) The I_{DS}–V_{BG} curve was obtained. (f) The R_λ of the $(BA)_2FAPb_2I_7$ photodetector is presented as a function of V_{BG}. Reprinted with permission.[109] Copyright 2021, Wiley-VCH GmbH.

Qiu *et al.* presented a low-temperature solution method for the synthesis of $(BA)_2(MA)_3Pb_4I_{13}$ 2D FET.[110] FETs were constructed by placing a SnO_2 buffer between the substrate and the single-crystal layer, along with the incorporation of NH_4Cl into the precursor. The oxide buffer in line the perovskite layer parallel to the surface, whereas the chloride salt enhanced crystalline order and concurrently passivated electronic traps *via* gentle doping. The interaction of these factors limited ion migration while enhancing effective charge transport. The completed transistors exhibited room-temperature mobilities almost 10^{-2} cm^2 V^{-1} s^{-1} and an ON/OFF ratio close to 10^4, demonstrating minimal hysteresis throughout the sweeping cycles.

Halide perovskites that include chiral organic ligand molecules exhibit sensitivity to both left- and right-handed circularly polarized light, which could facilitate selective detection of circularly polarized light. Hu *et al.* investigated the photoresponses in chiral ((*S*)-(−)-α-methyl benzylamine)$_2PbI_4$ and ((*R*)-(+)-α-methyl benzylamine)$_2PbI_4$, referred to as (*S*-MBA)$_2PbI_4$ and (*R*-MBA)$_2PbI_4$, respectively, using a thin-film FET configuration.[111] Fig. 8a–f illustrate the drain–source current profiles for (*S*- and *R*-MBA)$_2PbI_4$ transistors subjected to left- and right-circularly polarized light (LCP: left-handed circular polarized, RCP: righthanded circular polarized) of the same intensity, 6.3 mW cm^{-2}, recorded at temperatures of 300, 220, and 77 K with V_{GS} set to 0 V. It was clear that (*S*-MBA)$_2PbI_4$ transistors produced a stronger photocurrent when exposed to LCP compared to RCP, while (*R*-MBA)$_2PbI_4$ exhibited a higher photocurrent under RCP than LCP throughout the tested bias range, V_{DS} = −20 to 0 V, at temperatures of 300 K, 220 K, and 77 K, respectively, in the measurements conducted. This observation confirms that the left-handed chiral perovskite (*S*-MBA)$_2PbI_4$ exhibited a stronger response to LCP illumination compared to RCP. In contrast, the right-handed analog demonstrated the opposite behavior under identical conditions. Fig. 8g and h illustrated the variation of I_{DS}–V_{DS} curves for 20 wt% (*S*-MBA)$_2PbI_4$ and (*R*-MBA)$_2PbI_4$ transistors, functioning in photoconductor mode (V_{GS} = 0 V), as a function of temperature under 447 nm illumination, utilizing LCP or RCP beams with an intensity of 6.3 mW cm^{-2} across the temperatures of 300, 220, and 77 K. The output current, observed during the sweep of V_{DS} from −20 to 0 V, clearly displayed an initial linear section, which was subsequently followed by a noticeable saturation plateau. The I_{DS} responses from 20 wt% (*S*- and *R*-MBA)$_2PbI_4$ transistors, shown in Fig. 8g and h, exhibited a linear region for V_{DS} ranging from −3 to 0 V, followed by a saturation region extending to −20 V. Fig. 8g illustrates the I_{DS}–V_{DS} response of a 20 wt% (*S*-MBA)$_2PbI_4$ transistor when subjected to LCP illumination at a consistent light intensity of 6.3 mW cm^{-2}. At 300 K, the photocurrent measured 1.02 × 10^{-7} A, then decreased by approximately one order to 1.12 × 10^{-8} A at 150 K and ultimately fell to 7.41 × 10^{-10} A when cooled to the minimum temperature of 77 K, which was the recorded measurement. A similar thermal trend was observed for the 20 wt% (*R*-MBA)$_2PbI_4$ transistor when subjected to RCP illumination at 6.3 mW cm^{-2}, as illustrated in Fig. 8h during

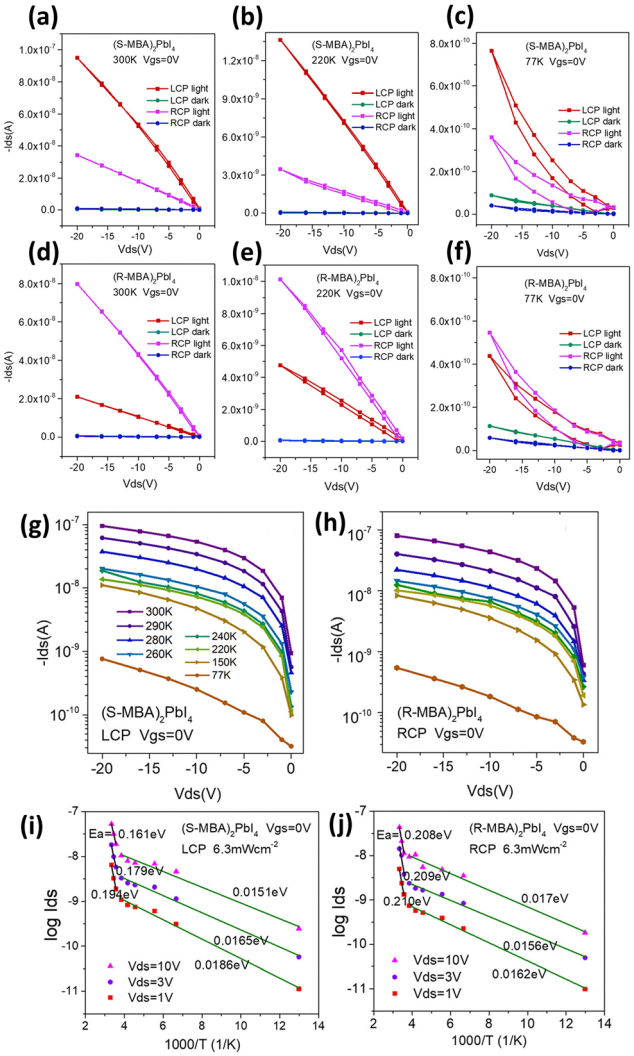

Fig. 8 The output current of a (*S*-MBA)$_2PbI_4$-based FET was measured under LCP and RCP illuminations, along with the corresponding outputs in dark conditions at (a) 300 K, (b) 220 K, and (c) 77 K, respectively. The output current under incident LCP and RCP illuminations with a light intensity of 6.3 mW cm^{-2} and the corresponding outputs in dark conditions at (d) 300 K, (e) 220 K, and (f) 77 K, respectively. Output curves of (g) a 20 wt% (*S*-MBA)$_2PbI_4$-based FET for temperatures spanning from 77 to 300 K under LCP illumination. (h) I_{DS}–V_{DS} characteristics of a 20 wt% (*R*-MBA)$_2PbI_4$ FET under RCP illumination. Logarithmic photocurrent for (i) a 20 wt% (*S*-MBA)$_2PbI_4$-based FET under LCP light illumination with and (j) a 20 wt% (*R*-MBA)$_2PbI_4$ FET in the presence of RCP light illumination. Reprinted with permission.[111] Copyright 2023, American Chemical Society.

the intensity testing phase. Current values of 8.43 × 10^{-8} A, 8.11 × 10^{-9} A, and 5.51 × 10^{-10} A were recorded at temperatures of 300 K, 150 K, and 77 K, respectively. To investigate the thermal influence in greater detail, logarithmic photocurrent was plotted against reciprocal temperature for 20 wt% (*S*-MBA)$_2PbI_4$ under LCP and 20 wt% (*R*-MBA)$_2PbI_4$ under RCP, each illuminated at 6.3 mW cm^{-2} while V_{DS} was fixed at 1, 3, or 10 V and V_{GS} maintained at 0 V, resulting in the thermal-activation graphs of Fig. 8i and j. Notably, both devices exhibited nearly identical I_{DS} evolutions *versus* 1/*T*, suggesting

similar carrier transport mechanisms irrespective of molecular handedness across the examined range of cooling and heating.

Also, Liao *et al.* synthesized four tin-iodide layered perovskite single crystals, 3-(aminomethyl)piperidinium tin iodide ($3AMPSnI_4$, 3A), 4-(aminomethyl)piperidinium tin iodide ($4AMPSnI_4$, 4A), 3-(aminomethyl)pyridinium tin iodide ($3AMPYSnI_4$, 3Y), and 4-(aminomethyl)pyridinium tin iodide ($4AMPYSnI_4$, 4Y), using a simple low-temperature solution-crystallization method.[112] Crystallographic inspection indicated that the derivatives featuring piperidinium cations with primary amino termini oriented uniformly (3A and 4Y) exhibited authentic Dion–Jacobson (DJ) architectures, resulting in net dipole moments due to the alignment of every $-NH_3^+$ group in the same direction between adjacent $[SnI_6]^{4-}$ slabs. In contrast, the RP analogs utilized two monoammonium spacers for each layer, effectively neutralizing the overall dipole. Notable symmetry differences were observed: 3A crystallized in a tetragonal system, while 4A, 3Y, and 4Y displayed orthorhombic metrics. Structural models from the side and top views in Fig. 9a and b illustrated that 3A, 4A, and 4Y exhibited eclipsed stacking, with the octahedra positioned directly above each other with a (0, 0) translation. The SEM revealed consistent plate-like morphologies in Fig. 9c and d. In contrast, 3Y exhibited a zig-zag arrangement with a (0.25, 0) shift, enabling simultaneous in-plane and out-of-plane Sn–I tilting, which resulted in needle-like crystals, as observed in the micrographs. The evaluation of transistors utilizing the 4A crystal was conducted subsequently. Fig. 9e illustrates the hole-transfer characteristics obtained at $V_{DS} = -40$ V, with V_{GS} being varied from 10 V to −15 V under ambient conditions. A minor hysteresis loop appeared but stayed constrained, likely due to the low density of grain boundaries inhibiting long-range ion migration. The threshold voltage, derived from the forward linear segment, was determined to be −2.5 V. The output curves presented in Fig. 9f confirm p-type modulation. The calculated maximum and average hole mobilities in the linear regime were found to be 0.57 $cm^2 V^{-1} s^{-1}$ and 0.45 $cm^2 V^{-1} s^{-1}$, respectively. The device maintained an ON/OFF ratio of approximately 4.2×10^2 and demonstrated commendable cycling durability, as shown in Fig. 9g.

Zhu *et al.* investigated that a practical interfacial-crystallization approach was developed for growing single-crystal perovskite at a liquid–liquid interface.[113] By controlling the solvent composition and supersaturation level at this junction, the transformation of Cs_2SnI_6 was achieved, transitioning from a 3D to a 2D structure. This process resulted in well-defined morphologies, including octahedra, pyramids, hexagons, and triangular nanosheets. In this study, two reagents, CsI and SnI_4, were dissolved in immiscible solvents, so it was certain that all subsequent chemical reactions took place precisely at their interface in Fig. 10a. The lower phase consisted of ethylene glycol (EG) mixed with hydriodic acid (HI) and saturated with CsI, while the upper phase contained hexane with SnI_4. The inability of these liquids to mix resulted in the formation of a planar boundary, which consequently limited the precipitation of Cs_2SnI_6 to that specific plane. HI demonstrated its crucial role; increasing its concentration led to a

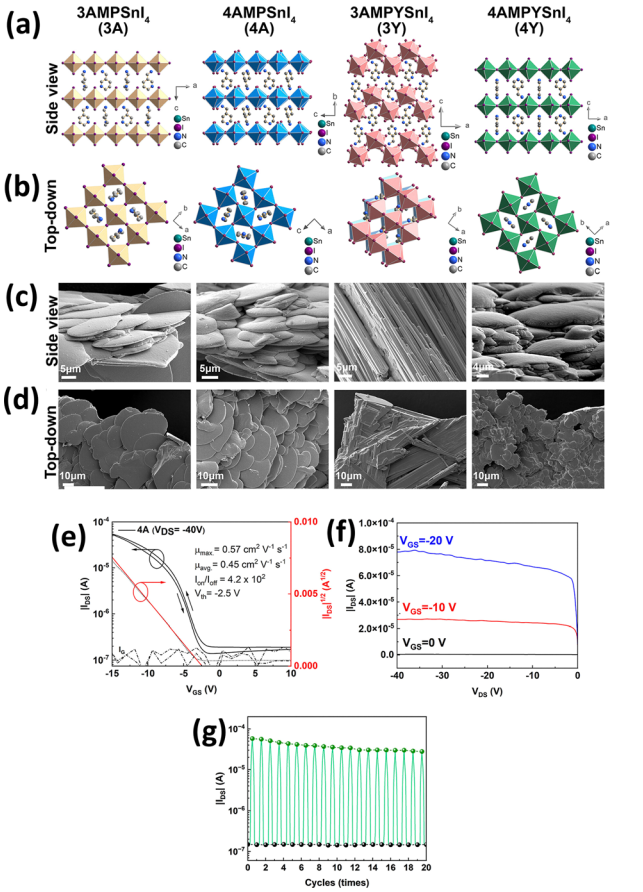

Fig. 9 (a) Side and (b) top-down views of the illustrated crystal structures for $3AMPSnI_4$ (3A), $4AMPSnI_4$ (4A), $3AMPYSnI_4$ (3Y), and $4AMPYSnI_4$ (4Y). Images (c) and (d) present tilted and top-down perspectives of the four single crystals as observed through scanning electron microscopy at room temperature. (e) Transfer curve, (f) current–voltage output curve, and (g) ON/OFF switching curves of the 4A FET device demonstrate commendable stability over 20 cycles. Reprinted with permission.[112] Copyright 2024, American Chemical Society.

significant decrease in the solubility of Cs_2SnI_6 within the EG matrix while simultaneously enhancing chemical supersaturation. In the same way, incorporating larger portions of the SnI_4 feed enriched the Sn^{4+}/I^- species near the frontier, thus further advancing the equilibrium toward solidification. As a result, by simultaneously adjusting the HI fraction and the SnI_4 quantity, the nucleation driving force can be altered, transitioning the growth mode and final morphology in Fig. 10a from octahedra to triangles. The resultant shapes initially appeared as truncated tetrahedra in Fig. 10b. Upon reaching 100 μL of the SnI_4 portion, defined pyramidal crystallites with a wide, flat hexagonal footplate emerged in Fig. 10c. Increasing the SnI_4 charge beyond 160 μL provided a sufficient amount of precursor, enabling lateral growth that exceeded vertical stacking and resulting in flat hexagonal platelets in Fig. 10d. With an HI : EG ratio of 1.5 : 1, the solubility decreased significantly, even a minor SnI_4 blend caused swift precipitation under conditions of strong kinetic nonequilibrium, resulting in the isolation of triangular sheets exceeding 40 μm laterally in Fig. 10e.

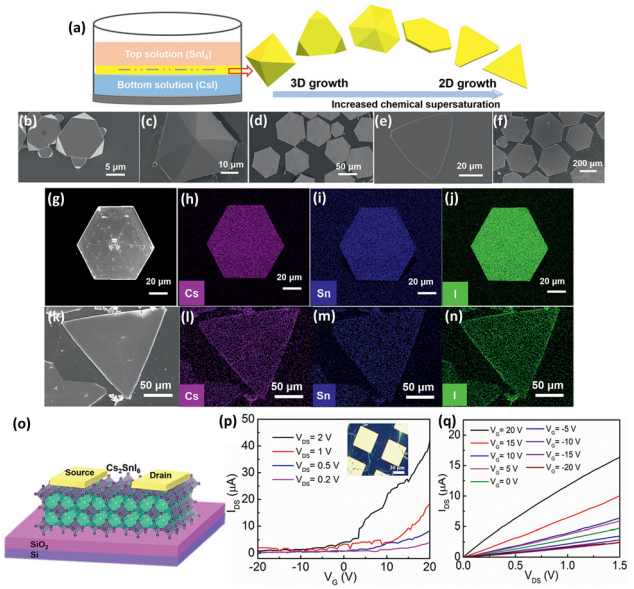

Fig. 10 (a) A schematic illustration depicting the growth of Cs_2SnI_6 crystals at the liquid–liquid interface. The geometries of precipitated crystals can be adjusted from three-dimensional to two-dimensional by enhancing the chemical supersaturation of Cs_2SnI_6 at the interface, resulting in significant nonequilibrium growth. SEM images illustrate the morphologies and geometries of various crystals, including (b) truncated tetrahedral, (c) pyramidal, (d) hexagonal, and (e) triangular-shaped Cs_2SnI_6 crystals featuring round tips. (f) A scanning electron microscopy image depicting large, flat hexagonal crystals exhibiting a lateral dimension exceeding 400 μm. (g) An SEM image depicting a hexagonal Cs_2SnI_6 crystal exhibiting growth steps that illustrate a layer-by-layer growth mechanism, accompanied by EDS elemental mapping for the elements: (h) Cs, (i) Sn, and (j) I. (k) A SEM image and (l)–(n) EDS mapping of a triangular Cs_2SnI_6 nanosheet demonstrate a consistent distribution of elements. (o) A schematic illustration of a back-gated Cs_2SnI_6 thin film FET device is presented. (p) The I_{DS}–V_{GS} characteristics of the fabricated Cs_2SnI_6 FET device were analyzed at different gate voltages, with the inset showcasing the optical image of the device that was created. (q) The I_{DS}–V_{DS} characteristics of the device were analyzed at various back-gate voltages, employing a step size of 5 V. Reprinted with permission.[113] Copyright 2020, Wiley-VCH GmbH.

The systematic expansion of crystal breadth was observed: at a concentration of 200 μL of SnI_4, the hexagonal plates exceeded 400 μm in size in Fig. 10f. With the highest HI content combined with ≥50 μL SnI_4, extensive ultrathin sheets formed, interconnected, and resulted in coherent films at the boundary. Fig. 10g–n displays SEM images that illustrate a typical hexagonal crystal with a massive triangular sheet. The energy-dispersive X-ray maps, Fig. 10h–j for the hexagon and Fig. 10l–n for the triangle, revealed uniform distributions of Cs, Sn, and I, confirming compositional consistency across each specimen. The electronic characteristics of the triangular nanosheets were investigated in bottom-gate FET in Fig. 10o. The I_{DS}–V_{GS} sweeps demonstrated a consistently increasing drain current as V_{GS} changed from negative to positive values in Fig. 10p, a characteristic indicative of n-type transport that supported previous Hall measurements. The current–voltage traces at various gate biases in Fig. 10q supported this assignment, demonstrating larger positive I_{DS} with progressively more positive gates. Based on the sheet dimensions and the transconductance obtained from Fig. 10p, the estimated electron mobility was found to be 35 $cm^2\ V^{-1}\ s^{-1}$. The fabricated devices exhibited an ON/OFF ratio of approximately 50 at V_{DS} = 2 V.

7. Conclusions

This review explores the latest advancements in single-crystal halide perovskite FETs and situates these materials within the broader context of developing low-power, high-throughput electronics. Table 1 summarizes representative 2D and 3D single-crystal halide perovskite FETs. The initial investigation focused on the crystallographic versatility of the ABX_3 lattice and its layered derivatives, emphasizing the relationship of structural dimensionality, spacer chemistry, and defect management in regulating carrier mobility and ionic motion. A thorough analysis of growth techniques revealed that inverse-temperature crystallization, solvent engineering, and epitaxial strategies currently produce bulk and thin-film crystals with significantly lower trap densities, resulting in more dependable model platforms compared to polycrystalline films. It demonstrated that minimizing vacancy concentrations and passivating interfaces allows perovskite channels to maintain strong gate modulation even in ambient conditions. The results show that ion migration always prevents steady-state operation at room temperature. This paper looks into the intricate relationships among dielectric selection, contact energetics, and environmental stress. An appropriate gate dielectric can inhibit interfacial ion drift while preserving high capacitance, while precisely aligned work functions in source and drain contacts reduce Schottky barriers and long-term degradation. Enhancements in threshold stability, reduced hysteresis, and increased ON/OFF ratios indicate that phonon scattering, rather than defects, currently prevails within practical bias windows.

In the future, the field will gain a better knowledge of mixed-dimensional structures and lattice strength, both of which have the potential to limit ion movement without sacrificing electronic coupling. The integration of lead-free alternatives is crucial for broader acceptance; however, their unique oxidation pathways necessitate customized passivation chemistries. Furthermore, vertical device geometries and dual-gate configurations provide significant opportunities for separating ionic and electronic responses, enabling advancements in complementary logic, neuromorphic circuits, and the integration of optoelectronics on flexible substrates.

Table 1 Comparison of various halide perovskite-based FETs

	Materials	Mobility ($cm^2\ V^{-1}\ s^{-1}$)	ON/OFF ratio	Ref.
3D	$MAPbI_3$	3×10^{-3}	50	103
	$MAPbBr_3$	23.39	2.64×10^4	104
	$CsPbBr_3$	7.3	10^6	107
2D	$(BA)_2(MA)_3Pb_4I_{13}$	10^{-2}	10^4	110
	$4AMPSnI_4$	0.57	4.2×10^2	112
	Cs_2SnI_6	35	50	113

Future efforts ought to focus on developing standardized protocols that resolve bias over time and create physics-based compact models, effectively distinguishing between ionic and electronic responses across various device architectures. Outstanding issues include the integration of single crystals at wafer scale, the ability to operate reliably under combined electrical, thermal, and optical stress, as well as the need for reproducible lead-free compositions that align with flexible low-temperature manufacturing processes.

Author contributions

Hyojung Kim: writing – original draft, funding acquisition.

Conflicts of interest

There are no conflicts to declare.

Data availability

No primary research results, software or code have been included and no new data were generated or analysed as part of this review.

Acknowledgements

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIT) (RS-2025-00554803).

Notes and references

1 H. Kim, G. Veerappan and J. H. Park, *Electrochim. Acta*, 2014, **137**, 164–168.
2 H. Kim, G. Veerappan, D. H. Wang and J. H. Park, *Electrochim. Acta*, 2016, **187**, 218–223.
3 H. Yuan, M. Hilal, Y. Ali, H. S. Abdo, Z. Cai, H. Kim, U. Ullah, H. Fayaz, W. Xie and J. I. Han, *Surf. Interfaces*, 2024, **54**, 105266.
4 M. Hilal, Y. Ali, Z. Cai, H. Kim, H. S. Abdo, I. A. Alnaser, Y. Hwang and J. I. Han, *Surf. Interfaces*, 2025, **60**, 106097.
5 Z. Song, M. Hilal, H. S. Abdo, Z. Cai, H. Kim and J. I. Han, *J. Ind. Eng. Chem.*, 2024, **144**, 691–699.
6 M. Hilal, Y. Ali, Z. Cai, H. Kim, H. S. Abdo, I. A. Alnaser and Y. Hwang, *Ceram. Int.*, 2025, **51**, 16246–16256.
7 H. Kim, I. H. Im, D. Hyun, M. Hilal, Z. Cai, S. J. Yang, Y.-S. Shim and C. W. Moon, *J. Korean Ceram. Soc.*, 2025, **62**, 397–411.
8 H. Yuan, M. Hilal, Y. Ali, H. M. U. Ayub, Z. Cai, H. Kim, W. Zhang, A. A. Khan, H. S. Abdo, I. A. Alnaser, Y. Hwang and J. I. Han, *Surf. Interfaces*, 2025, **58**, 105888.
9 J. Lee, H. Kim, M. Hilal and Z. Cai, *Solid State Sci.*, 2024, **156**, 107683.
10 J. Lee, H. Kim, M. Hilal and Z. Cai, *J. Electroceram.*, 2024, **52**, 283–296.
11 Y.-J. Son, S.-W. Kim, H.-M. Kim, H. Kim, B. Chu and D.-Y. Jeong, *Materials*, 2025, **18**, 1427.
12 G. Li, J. Hou, M. Hilal, H. Kim, Z. Chen, Y. Cui, J.-H. Kim and Z. Cai, *Sensors*, 2024, **24**, 6839.
13 J. Lee, H. Kim, M. Hilal and Z. Cai, *J. Mater. Sci.: Mater. Electron.*, 2024, **35**, 1421.
14 J. Hwang, J. H. Chung, H. J. Kim, S.-H. Park, Y.-H. Cho, S. Sohn, S.-J. Ro, H. Kim, K. Lee, D. Cho, J. H. Seo, Y.-S. Shim, J. Lee and W. Lee, *Sens. Actuators, B*, 2025, **442**, 138070.
15 Y. Cho, D. Kim, J. H. Seo, J. H. Chung, Z. Park, K. C. Kwon, J. Ko, T. W. Ha, J. Lee, G. Kim, S. Ro, H. Kim, C. Lee, K. Lee, Y. Shim and D. Cho, *Adv. Sci.*, 2025, **12**, 2501293.
16 M. Hilal, Y. Ali, Z. Cai, H. Kim, H. S. Abdo, I. A. Alnaser and Y. Hwang, *Sens. Actuators, A*, 2025, **388**, 116479.
17 A. Liu, H. Zhu, S. Bai, Y. Reo, M. Caironi, A. Petrozza, L. Dou and Y.-Y. Noh, *Nat. Electron.*, 2023, **6**, 559–571.
18 S. Shrestha, G. J. Matt, A. Osvet, D. Niesner, R. Hock and C. J. Brabec, *J. Phys. Chem. C*, 2018, **122**, 5935–5939.
19 F. Haque, N. T. T. Hoang, J. Ji and M. Mativenga, *IEEE Electron Device Lett.*, 2019, **40**, 1756–1759.
20 T. H. Chowdhury, Y. Reo, A. R. B. M. Yusoff and Y. Noh, *Adv. Sci.*, 2022, **9**, 2203749.
21 S. Wang, K. Bidinakis, C. Haese, F. H. Hasenburg, O. Yildiz, Z. Ling, S. Frisch, M. Kivala, R. Graf, P. W. M. Blom, S. A. L. Weber, W. Pisula and T. Marszalek, *Small*, 2023, **19**, 2207426.
22 I. You and Y.-Y. Noh, *Appl. Phys. Lett.*, 2021, **118**, 250501.
23 V. Podzorov and V. Bruevich, *Nat. Electron.*, 2024, **7**, 266–268.
24 B. Liu, M. Long, M.-Q. Cai and J. Yang, *J. Phys. D: Appl. Phys.*, 2018, **51**, 105101.
25 S. Lee, H. Kim, D. H. Kim, W. Bin Kim, J. M. Lee, J. Choi, H. Shin, G. S. Han, H. W. Jang and H. S. Jung, *ACS Appl. Mater. Interfaces*, 2020, **12**, 17039–17045.
26 H. Kim, J. S. Kim, J. Choi, Y.-H. Kim, J. M. Suh, M.-J. Choi, Y.-S. Shim, S. Y. Kim, T.-W. Lee and H. W. Jang, *ACS Appl. Mater. Interfaces*, 2024, **16**, 2457–2466.
27 H. Kim, J. S. Han, J. Choi, S. Y. Kim and H. W. Jang, *Small Methods*, 2018, **2**, 1700310.
28 H. Kim, K. A. Huynh, S. Y. Kim, Q. Van Le and H. W. Jang, *Phys. Status Solidi RRL*, 2020, **14**, 1900435.
29 H. Kim, J. S. Han, S. G. Kim, S. Y. Kim and H. W. Jang, *J. Mater. Chem. C*, 2019, **7**, 5226–5234.
30 H. Kim, D. Hyun, M. Hilal, Z. Cai and C. W. Moon, *Electronics*, 2024, **13**, 3572.
31 J. Y. Park, Y. H. Lee, H. Kim and L. Dou, *J. Appl. Phys.*, 2023, **134**, 060901.
32 S. G. Kim, J. S. Han, H. Kim, S. Y. Kim and H. W. Jang, *Adv. Mater. Technol.*, 2018, **3**, 1800457.
33 H. Kim, M.-J. Choi, J. M. Suh, J. S. Han, S. G. Kim, Q. Van Le, S. Y. Kim and H. W. Jang, *NPG Asia Mater.*, 2020, **12**, 21.
34 H. Kim, M. Choi, J. M. Suh, Y.-S. Shim, I. H. Im, D. Hyun, S. J. Yang, Z. Cai, M. Hilal, M. G. Lee, C. W. Moon, S. Y. Kim and H. W. Jang, *Mater. Sci. Semicond. Process.*, 2024, **182**, 108718.

35 D. Marongiu, M. Saba, F. Quochi, A. Mura and G. Bongiovanni, *J. Mater. Chem. C*, 2019, **7**, 12006–12018.
36 W. Tao, Y. Zhang and H. Zhu, *Acc. Chem. Res.*, 2022, **55**, 345–353.
37 K. R. Hansen, J. S. Colton and L. Whittaker-Brooks, *Adv. Opt. Mater.*, 2024, **12**, 2301659.
38 S.-H. Lin and J.-L. Kuo, *Phys. Chem. Chem. Phys.*, 2014, **16**, 20763–20771.
39 D. C. Hvazdouski, S. Baranava, E. A. Korznikova, A. A. Kistanov and V. R. Stempitsky, *2D Mater.*, 2024, **11**, 025022.
40 J. M. Hoffman, X. Che, S. Sidhik, X. Li, I. Hadar, J.-C. Blancon, H. Yamaguchi, M. Kepenekian, C. Katan, J. Even, C. C. Stoumpos, A. D. Mohite and M. G. Kanatzidis, *J. Am. Chem. Soc.*, 2019, **141**, 10661–10676.
41 S. Min and J. Cho, *Adv. Opt. Mater.*, 2024, **12**, 2302516.
42 Z.-Z. Zhang, T.-M. Guo, Z.-G. Li, F.-F. Gao, W. Li, F. Wei and X.-H. Bu, *Acta Mater.*, 2023, **245**, 118638.
43 H. L. B. Boström, J. Bruckmoser and A. L. Goodwin, *J. Am. Chem. Soc.*, 2019, **141**, 17978–17982.
44 S. Peng, Z. Yang, M. Sun, L. Yu and Y. Li, *Adv. Mater.*, 2023, **35**, 2304711.
45 Y. Liang, F. Li and R. Zheng, *Adv. Electron. Mater.*, 2020, **6**, 2000137.
46 Y. Zhang, M. Abdi-Jalebi, B. W. Larson and F. Zhang, *Adv. Mater.*, 2024, **36**, 2404517.
47 Y. Liu, S. Yuan, H. Zheng, M. Wu, S. Zhang, J. Lan, W. Li and J. Fan, *Adv. Energy Mater.*, 2023, **13**, 2300188.
48 J. S. Han, Q. Van Le, J. Choi, H. Kim, S. G. Kim, K. Hong, C. W. Moon, T. L. Kim, S. Y. Kim and H. W. Jang, *ACS Appl. Mater. Interfaces*, 2019, **11**, 8155–8163.
49 J. Butkus, P. Vashishtha, K. Chen, J. K. Gallaher, S. K. K. Prasad, D. Z. Metin, G. Laufersky, N. Gaston, J. E. Halpert and J. M. Hodgkiss, *Chem. Mater.*, 2017, **29**, 3644–3652.
50 S. G. Kim, Q. Van Le, J. S. Han, H. Kim, M. Choi, S. A. Lee, T. L. Kim, S. B. Kim, S. Y. Kim and H. W. Jang, *Adv. Funct. Mater.*, 2019, **29**, 1906686.
51 H. M. Jang, J. Park, S. Kim and T.-W. Lee, *J. Phys.: Condens. Matter*, 2021, **33**, 355702.
52 J. S. Han, Q. Van Le, H. Kim, Y. J. Lee, D. E. Lee, I. H. Im, M. K. Lee, S. J. Kim, J. Kim, K. J. Kwak, M. Choi, S. A. Lee, K. Hong, S. Y. Kim and H. W. Jang, *Small*, 2020, **16**, 2003225.
53 J. S. Han, Q. Van Le, J. Choi, K. Hong, C. W. Moon, T. L. Kim, H. Kim, S. Y. Kim and H. W. Jang, *Adv. Funct. Mater.*, 2018, **28**, 1705783.
54 Y. Ma, Y. Wang, Y. Fang, Y. Jiang, Z. Dai and J. Miao, *Adv. Opt. Mater.*, 2024, **12**, 2401367.
55 T. Hossain, H. R. Atapattu, H. Pruett, M. T. Rahman, K. R. Pedersen, A. J. Huckaba, S. R. Parkin and K. R. Graham, *Chem. Mater.*, 2024, **36**, 11004–11014.
56 W. Gao, C. Chen, C. Ran, H. Zheng, H. Dong, Y. Xia, Y. Chen and W. Huang, *Adv. Funct. Mater.*, 2020, **30**, 2000794.
57 J. Xu, J. Ma, Y. Gu, Y. Li, Y. Li, H. Shen, Z. Zhang and Y. Ma, *Cryst. Res. Technol.*, 2023, **58**, 2200128.
58 P. Andričević, P. Frajtag, V. P. Lamirand, A. Pautz, M. Kollár, B. Náfrádi, A. Sienkiewicz, T. Garma, L. Forró and E. Horváth, *Adv. Sci.*, 2021, **8**, 2001882.
59 F. X. Xie, H. Su, J. Mao, K. S. Wong and W. C. H. Choy, *J. Phys. Chem. C*, 2016, **120**, 21248–21253.
60 K. R. Dudipala, T. Le, W. Nie and R. L. Z. Hoye, *Adv. Mater.*, 2024, **36**, 2304523.
61 S. Watanabe, T. Hayashida, M. Iwai, Y. Inomata, M. Kunitake and T. Kida, *ACS Omega*, 2023, **8**, 2455–2461.
62 M. Yang, Z. Nie, X. Li, R. Wang, Y. Zhao and H. Wang, *J. Mater. Chem. C*, 2023, **11**, 5908–5967.
63 Y. Chen, M. He, J. Peng, Y. Sun and Z. Liang, *Adv. Sci.*, 2016, **3**, 1500392.
64 F. Huang, F. Fang, Y. Zheng, Q. You, H. Li, S. Fang, X. Cong, K. Jiang, Y. Wang, C. Han, W. Chen and Y. Shi, *Nano Res.*, 2023, **16**, 1304–1312.
65 M. Yin, H. Yao, H. Qiu, C. Wu, M. Zhang and F. Hao, *Adv. Funct. Mater.*, 2024, **34**, 2404792.
66 W. Jiang, H. Di, H. Sun, C. Zhao, F. Liao and Y. Zhao, *J. Cryst. Growth*, 2020, **550**, 125880.
67 F. Chen, C. Xu, Q. Xu, Y. Zhu, Z. Zhu, W. Liu, X. Dong, F. Qin and Z. Shi, *Cryst. Growth Des.*, 2018, **18**, 3132–3137.
68 S. Wang, Z. Ling, P. W. M. Blom, T. Marszalek and W. Pisula, *Adv. Funct. Mater.*, 2025, 2501217.
69 Y. Cho, H. R. Jung and W. Jo, *Nanoscale*, 2022, **14**, 9248–9277.
70 J. Peng, C. Q. Xia, Y. Xu, R. Li, L. Cui, J. K. Clegg, L. M. Herz, M. B. Johnston and Q. Lin, *Nat. Commun.*, 2021, **12**, 1531.
71 Z. Yuan, J. Zhou, Y. Zhang, X. Ma, J. Wang, J. Dong, F. Lu, D. Han, B. Kuang and N. Wang, *J. Phys.: Condens. Matter*, 2022, **34**, 144009.
72 F. Yu, Y. Song, L. Wang, Y. Yang, J. Wang, X. Shen, B. Jin, H. Song, Y. Fang and Q. Dong, *Small*, 2025, **21**, 2407109.
73 J. Zhang, Z. Li, P. Wang, M. Wang, Z. Qi, Y. Yin, H. Ma, J. Liu, R. Wang, W. Tian, R. Cai, S. Jin, X. Jiang and Y. Shi, *ACS Appl. Mater. Interfaces*, 2024, **16**, 476–484.
74 J.-J. Cao, Y.-H. Lou, K.-L. Wang and Z.-K. Wang, *J. Mater. Chem. C*, 2022, **10**, 7423–7436.
75 L. Ke, S. Luo, X. Ren and Y. Yuan, *J. Phys. D: Appl. Phys.*, 2021, **54**, 163001.
76 W. Qin, K. Zheng, H. Liu and J. Chu, *J. Mater. Sci.*, 2022, **57**, 5374–5383.
77 D. Ding, B. Zhou, X. Li, J. Duan, K. Wu, B. Hou, H. Fan, H. Liu and L. Jiang, *J. Mater. Chem. A*, 2025, **13**, 961–970.
78 C. Yadav, M. Agrawal, A. Agarwal and Y. S. Chauhan, *IEEE Trans. Nanotechnol.*, 2017, **16**, 347–354.
79 B. Singh, D. Gola, K. Singh, E. Goel, S. Kumar and S. Jit, *IEEE Trans. Electron Devices*, 2016, **63**, 2299–2305.
80 D.-W. Park, S. Mikael, T.-H. Chang, S. Gong and Z. Ma, *Appl. Phys. Lett.*, 2015, **106**, 102106.
81 P. Darmawan, T. Minari, Y. Xu, S. Li, H. Song, M. Chan and K. Tsukagoshi, *Adv. Funct. Mater.*, 2012, **22**, 4577–4583.
82 K.-S. Shin, J.-H. Lee, S.-M. Han, I.-H. Song and M.-K. Han, *J. Non-Cryst. Solids*, 2006, **352**, 1708–1710.

83 C. S. Ho, Y. C. Lo, Y. H. Chang and J. J. Liou, *Solid State Electron.*, 2006, **50**, 1774–1779.
84 P. Mittal, B. Kumar, Y. S. Negi, B. K. Kaushik and R. K. Singh, *Microelectronics J.*, 2012, **43**, 985–994.
85 M. D. Jacunski, M. S. Shur and M. Hack, *IEEE Trans. Electron Devices*, 1996, **43**, 1433–1440.
86 D. C. Hong and Y. Taur, *IEEE Trans. Electron Devices*, 2021, **68**, 3734–3739.
87 N. Makris, M. Bucher, L. Chevas, F. Jazaeri and J.-M. Sallese, *IEEE Trans. Electron Devices*, 2020, **67**, 4658–4661.
88 S. G. Shirazi and S. Mirzakuchaki, *Appl. Phys. A: Mater. Sci. Process.*, 2013, **113**, 447–457.
89 W. K. Henson, N. Yang, S. Kubicek, E. M. Vogel, J. J. Wortman, K. De Meyer and A. Naem, *IEEE Trans. Electron Devices*, 2000, **47**, 1393–1400.
90 P. C. Chao, P. M. Smith, S. Wanuga, W. H. Perkins and E. D. Wolf, *IEEE Electron Device Lett.*, 1983, **4**, 326–328.
91 P. Patel and G. Kumar, in 2024 5th International Conference for Emerging Technology (INCET), IEEE, 2024, pp. 1–8.
92 L. Yang, H. Li, H. Xiu, M. Deng, Q. Tian, Q. Zhang and X. Xin, *Carbon*, 2023, **215**, 118396.
93 T.-M. Pan, C.-H. Yang and S.-T. Pang, *Mater. Sci. Semicond. Process.*, 2023, **164**, 107639.
94 P. Huo, B. Galiana and I. Rey-Stolle, *Semicond. Sci. Technol.*, 2017, **32**, 045006.
95 T.-M. Pan, C.-H. Yang, J.-L. Her and S.-T. Pang, *J. Alloys Compd.*, 2023, **960**, 170857.
96 J. He, F. Liu, J. Zhang, J. Feng, J. Hu, S. Yang and M. Chan, *IEEE Trans. Electron Devices*, 2007, **54**, 1203–1209.
97 C.-H. Kim and C. D. Frisbie, *J. Phys. Chem. C*, 2014, **118**, 21160–21169.
98 F. Tan, Y. Xiong, J. Yu, Y. Wang, Y. Li, Y. Wei, J. Sun, X. Xie, Q. Sun and Z. L. Wang, *Nano Energy*, 2021, **90**, 106617.
99 F. Palumbo, C. Wen, S. Lombardo, S. Pazos, F. Aguirre, M. Eizenberg, F. Hui and M. Lanza, *Adv. Funct. Mater.*, 2020, **30**, 1900657.
100 B. Chan, C. Soh, K. E. Siew, H. S. Kheong, L. W. Jer, I. Saad and N. Bolong, in 2021 IEEE 19th Student Conference on Research and Development (SCOReD), IEEE, 2021, pp. 130–134.
101 X.-J. She, C. Chen, G. Divitini, B. Zhao, Y. Li, J. Wang, J. F. Orri, L. Cui, W. Xu, J. Peng, S. Wang, A. Sadhanala and H. Sirringhaus, *Nat. Electron.*, 2020, **3**, 694–703.
102 S. P. Senanayak, M. Abdi-Jalebi, V. S. Kamboj, R. Carey, R. Shivanna, T. Tian, G. Schweicher, J. Wang, N. Giesbrecht, D. Di Nuzzo, H. E. Beere, P. Docampo, D. A. Ritchie, D. Fairen-Jimenez, R. H. Friend and H. Sirringhaus, *Sci. Adv.*, 2020, **6**, eaaz4948.
103 Y. Zhou, N. Tiwale, Y. Yin, A. Subramanian, M. H. Rafailovich and C.-Y. Nam, *Appl. Phys. Lett.*, 2021, **119**, 183303.
104 Y. Zou, Y. Shi, B. Wang, M. Liu, J. An, N. Zhang, L. Qi, W. Yu, D. Li and S. Li, *ACS Photonics*, 2023, **10**, 2280–2289.
105 T. Yang, C. Jin, J. Qu, A. A. Darvish, R. Sabatini, X. Zhang, H. Chen, S. P. Ringer, G. Lakhwani, F. Li, J. Cairney, X. Liu and R. Zheng, *ACS Appl. Mater. Interfaces*, 2021, **13**, 37840–37848.
106 V. Bruevich, L. Kasaei, S. Rangan, H. Hijazi, Z. Zhang, T. Emge, E. Y. Andrei, R. A. Bartynski, L. C. Feldman and V. Podzorov, *Adv. Mater.*, 2022, **34**, 2205055.
107 J. Zhou, L. Xie, X. Song, Z. Wang, C. Huo, Y. Xiong, Z. Cheng, Y. Wang, S. Zhang, X. Chen and H. Zeng, *J. Mater. Chem. C*, 2020, **8**, 12632–12637.
108 F. Khorramshahi and A. Takshi, *Electronics*, 2020, **9**, 1852.
109 R. K. Ulaganathan, R. C. Murugesan, C. Lin, A. Subramanian, W. Chen, Y. Chang, A. Rozhin and R. Sankar, *Adv. Funct. Mater.*, 2022, **32**, 2112277.
110 X. Qiu, Y. Liu, J. Xia, J. Guo, P.-A. Chen, H. Wei, J. Guo, X. Shi, C. Chen, Z. Zeng, H. Chen, L. Jiang, L. Liao and Y. Hu, *Cell Rep. Phys. Sci.*, 2023, **4**, 101217.
111 S. Hu, B. Tang, S. V. Kershaw and A. L. Rogach, *ACS Appl. Mater. Interfaces*, 2023, **15**, 27307–27315.
112 C. Liao, S. Bernardi, C. G. Bailey, I. H. Chao, S.-Y. Chien, G. Wang, Y.-H. Sun, S. Tang, J. Zheng, J. Yi, M.-H. Yu, S. P. Russo, H.-W. Yen, D. R. McCamey, B. J. Kennedy, A. Widmer-Cooper, C.-C. Chueh and A. W. Y. Ho-Baillie, *ACS Nano*, 2024, **18**, 14176–14186.
113 W. Zhu, J. Shen, M. Li, K. Yang, W. Bu, Y. Sun, J. Shi and J. Lian, *Small*, 2021, **17**, 2006279.