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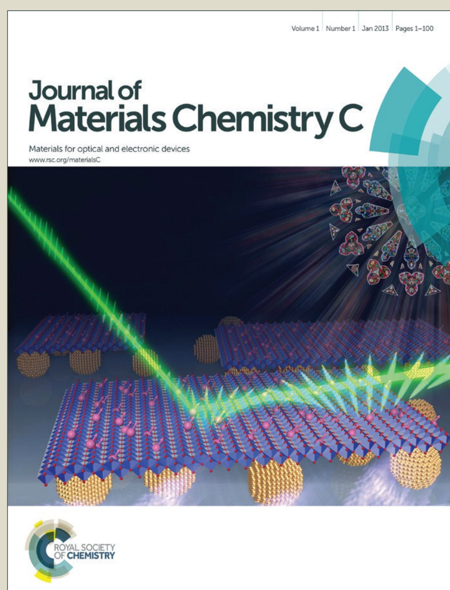

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Facial synthesis of KCu_7S_4 nanobelts for nonvolatile memory device application

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Abstract: Tetragonal KCu_7S_4 nanobelts (NBs) with width of 200-600 nm and length of up to hundreds of micrometers were facially synthesized *via* a solution-based method. Electrical analysis reveals that the as-fabricated NB exhibits typical *p*-type semiconducting characteristics with an exceptionally high carrier mobility of ~870 $cm^2 V^{-1} s^{-1}$, which may be attributed to the quasi-1D conduction path along the *c* axis in the structure of KCu_7S_4. Further study of a device based on Cu/KCu_7S_4 NB/Au Schottky junction shows a stable memory behavior with a set voltage of about 0.6 V, a current ON/OFF ratio of about 10^4, and a retention time > 10^4 s. Such resistive switching characteristics, according to our analysis are due to the interfacial oxide layers that can efficiently trap the electrons by the oxygen vacancies. This study will offer opportunities for the development of high-performance memory device with new geometry.

Key Words: Memory devices, semiconductor nanostructures, interfacial oxide layer, set voltage, retention time.

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1. Introduction

Thiocuprates, ternary compounds of a mono- or two-valent electropositive element (such as alkali metals (Na–Cs), $[NH_4]^+$, Ca, Tl (I), and Ba) with copper and sulphur, were first synthesized in 1862[1] and had attracted much research interest over the past 30 years. Since copper in this kind of compounds can adopt different coordinations, there is a rich structural chemistry, which merits intensive experimental and theoretical studies of transport phenomena of low-dimensional solids.[2]

K-Cu-S system, for example, have been intensively investigated due to their abundant phases (KCuS,[3] KCu_4S_3,[4, 5] $K_3Cu_8S_6$,[6, 7] KCu_3S_2,[8] KCu_7S_4,[9, 10] *et al.*) and their crystallographic structures as well as the unique physical and chemical properties. Among them, $KCu_{7-x}S_4$ (the nonstoichiometry range $0.00 \leqslant x \leqslant 0.34$)[11] is known to be constructed by two parallel Cu_4S_4 columns which lie on the mirror planes perpendicular to the *c* axis and are interconnected by tetrahedral Cu^+ cation chains, forming pseudo-one-dimensional channels in which the K^+ cations reside.[12] Low temperature phase transitions and resistivity anomalies have been observed in the phases, which were interpreted by vacancy ordering of the partially occupied tetrahedral Cu^+ cation chains in the structure by the single crystal studies.[13, 14] Meanwhile, the presence of the vacancies of Cu atoms as well as the inherent conducting pathway along the *c* axis gives rise to the relatively high conductivity, which facilitates the use of KCu_7S_4 series as the pseudocapacitor material.[15] Recently, a composite-hydroxide mediated (CHM) approach has emerged to be a one-step, convenient, low-cost, environment friendly and possibly mass-production route for the synthesis of a series of functional

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materials at nanoscale.[16] For example, Liu *et al.* reported one-pot synthesis of KCu_3S_2 microbelts *via* chemical reaction in the composited hydroxides solution (NaOH/KOH = 51.5:48.5) at 230 °C.[17] What is more, KCu_7S_4 nanowires had also been obtained from the KOH solution at 150 °C.[15] In spite of these tremendous progresses in synthesis, relatively few research work has been carried out to study the electronic devices application.[15] Herein, we report on large-scale synthesis of KCu_7S_4 nanobelts (NBs) with widths of 200-600 nm and lengths of up to hundreds of micrometers by a solution reaction at 80 ^{0}C, which is much lower than previous study. Electrical study finds that the as-prepared NBs exhibit typical *p*-type semiconducting characteristic with a high hole mobility of 870 cm^2/V s. Further device analysis study reveals that the KCu_7S_4/Cu Schottky junction exhibit a reproducible memory behaviour with a set voltage of 0.4-1.0 V, a current ON/OFF ratio of about 10^4, and a retention time >10^4 s. This memory characteristic is associated with the oxygen vacancies in the interfacial oxide layer which can act as efficient trapping centers to trap electrons.

Experimental Section

Materials synthesis: All the reagents (analytical-grade purity) were purchased from Shanghai Chemical Reagents Co. and were used without any further purification. In a typical synthesis of KCu_7S_4 nanobelts, KOH (3.52 g) was dissolved into 10 mL distilled water to form a homogeneous solution (~ 6 mol L^{-1}) with the equivalent concentration of OH^- ions to the mixture of composite hydroxide in the composite-hydroxide mediated (CHM) approach.[18] Then, 1 mmol $CuCl_2$, 4 mmol $Na_2S \cdot 9H_2O$ and 1 mL hydrazine hydrate were added into the vessel sequentially. After thorough stirring, the vessel was sealed and kept at 80 °C in water bath for 1 h. The taupe sponge-like products were finally collected by centrifugation and

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washed with distilled water and absolute ethanol several times and dried in a vacuum at 60 ^{0}C for 4 h for further characterization.

Structural analysis and device characterization: The morphologies and microstructures of the as-synthesized products were characterized by X-ray diffraction (XRD, Rigaku D/MAX-γB, Cu Kα radiation, λ=1.54178Å), transmission electron microscopy (TEM, Hitachi H800), high-resolution transmission electron microscopy (HRTEM, JEOL JEM-2100F), field emission scanning electron microscopy (FESEM, SIRION 200 FEG) and energy-dispersive X-ray spectroscopy (EDS, Oxford INCA, attached to SEM). The UV-vis absorption spectrum was performed on a UV-vis spectrometer (CARY 5000). X-ray photoelectron (XPS) spectra were recorded on a Thermo ESCALAB250 X-ray photoelectron spectrometer using monochromatized Al K*α* X-ray as the excitation source.

To assess the electrical properties of the KCu_7S_4 NBs, bottom-gate field-effect transistors (FETs) based on individual NB were constructed. Briefly, the as-synthesized KCu_7S_4 NBs were dispersed on a SiO_2 (300 nm)/n^+-Si substrate. Then photolithography, electron beam deposition and a subsequent lift-off process were utilized to define the Au (50 nm) electrodes on the KCu_7S_4 NBs. During device analysis, the heavily doped Si substrate acted as the global bottom gate in the nanoFETs. Cu/KCu_7S_4/Au memory devices were also constructed for the further research of the electrical switch behavior by fabricating a Cu (50 nm) electrode beside the adjacent Au (50 nm) electrode through an additional photolithography process. All the electrical measurements were carried out at room temperature with a semiconductor characterization system (Keithley 4200-SCS).

Results and Discussion

Figure 1a shows a typical XRD pattern of the as-synthesized products. All the diffraction peaks can be readily indexed to body-centered tetragonal KCu_7S_4 phase (JCPDS card No. 83-0357). No evident impurity peaks from Cu_2S and Cu_2O or other binary copper chalcogenides are observed, indicating that the products are of single phase and high purity. It is also noted that

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the intensity of (110) peak is much higher than that reported in standard JCPDS card, which implies a dominate crystal plane in the products. Figure 1b and c present a typical SEM and low-resolution TEM images of the as-synthesized KCu_7S_4 NBs, showing a general morphology of NBs with width of 200-600 nm and length of up to hundreds of micrometers. Notably, the EDS spectrum (inset of Figure 1b) reveals that the sample consists of K, Cu and S elements, with an atomic ratio of K: Cu: S = 1:7.04:4.3, indicative of a remarkable cation-deficiency in comparison with the stoichiometry of KCu_7S_4. Further HRTEM image taken from the edge of a single KCu_7S_4 NB (Figure 1d) discloses a well-defined 2D lattice fringes. The inter-planar spacings of 1.94 and 1.81 Å in the image correspond to the (002) and (440) lattice planes of tetragonal KCu_7S_4, respectively. Therefore, we can deduce that as-synthesized NBs grow along the direction [001] and are terminated with crystallographic planes (110). Such a preferential growth direction is in good agreement with the fast Fourier transform (FFT) pattern (see the inset of Figure 1d). Further XPS survey spectrum in Figure 1e shows that the NBs are chemically composed of three elements, i.e. K, Cu, and S. Considering the vague correlation between the binding energy of Cu and the valence state, the modified Auger parameter ($\alpha^{/}$), defined as the sum of the kinetic energy of the Auger signal and the binding energy of the photoelectron line is chosen to estimate the chemical state of Cu. Through the numerical sum of the Cu $2p_{3/2}$ line and the Cu LMM line (Figure 1e), the Auger parameter is calculated to be 1848.8 eV, suggesting the majority of the KCu_7S_4 are composed of mono-valence state of copper, i.e., Cu (I).[19] Meanwhile, two indistinctive shake-up peaks can be observed in the Cu2p spectrum, which implies the existence of a trace amount of CuO in the surface of the product.[20]

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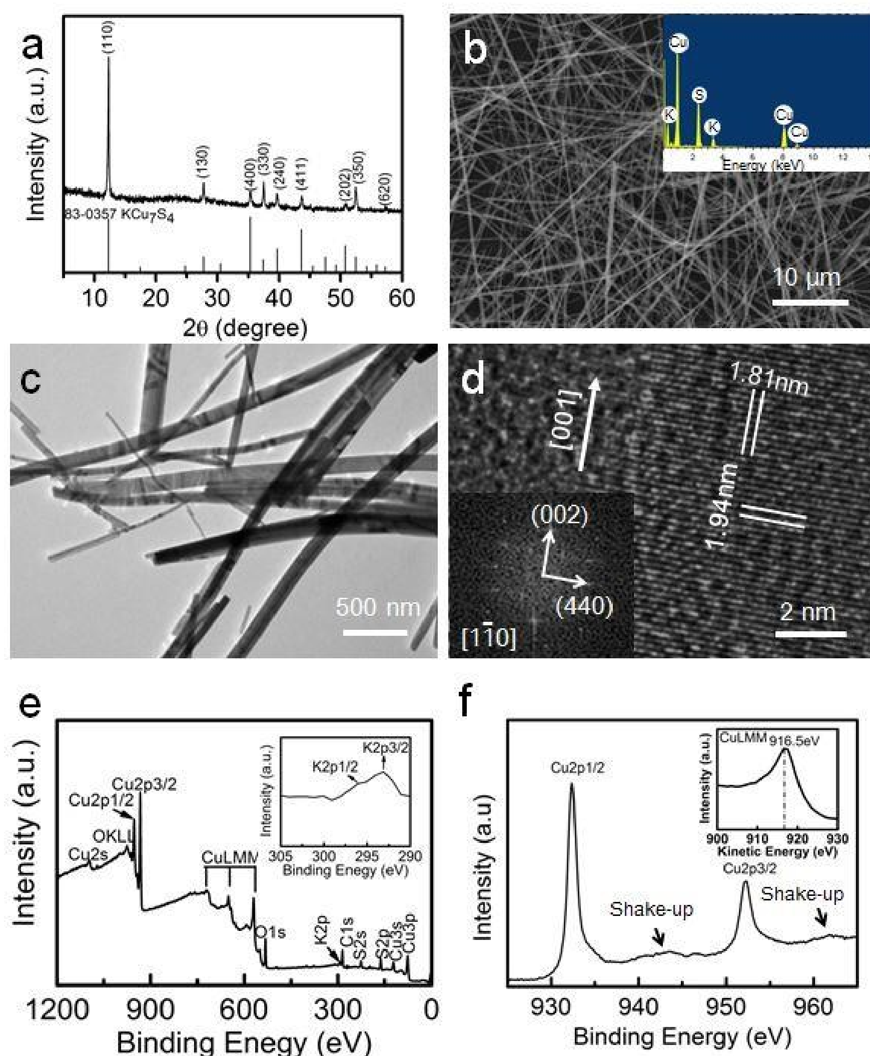

Figure 1 (a) XRD pattern, (b) FESEM image, (c) TEM image and (d) HRTEM image of as-synthesized products. Inset in (b) shows the corresponding EDS spectrum, and inset in (d) shows the corresponding SAED pattern. XPS spectra: (e) survey and (f) Cu2p spectrum. Insets show K2p spectrum and Cu LMM Auger spectrum, respectively.

It is worth noting that the formation of the KCu_7S_4 NBs is not only determined by the concentration of the alkali solution, but also by the Cu/S molar ratio. **Figure 2**a compares the XRD patterns of products obtained by various conditions. We can see clearly that high concentration of OH^- ions is favorable for the growth of KCu_7S_4 NBs. Even though the 3.52 g KOH of precursor was replaced with 3 g mixture of NaOH and KOH (Na/K ratio of 51.5:48.5), the morphology of the final product is nearly the same (Figure 2b). As the amount of KOH was

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decreased from 3.52 to 1.71 g, the resultant product will be mainly composed of microbelts with diameters of up to several micrometers (Figure 2c). Nevertheless, when the concentration was decreased to 0.3 g, a new phase ($Cu_{7.2}S_4$) with irregular morphology will be formed (Figure 2d). Further control experiment reveals that besides alkali concentration, the morphology and phase of the nanostructures were determined by the Cu/S molar ratios as well. Figure 2e & f show the products synthesized from varied Cu/S ratios. It is seen that short hexagonal microrods and well-defined NBs were obtained from the Cu/S ratio of 1/2 (shown in Figure 2e) and 1/5 (shown in Figure 2f), respectively. However, no remarkable difference can be observed between the Cu/S ratio of 1/5 and 1/4 (shown in Figure 1b). Therefore, we deduce that excess S with the Cu/S ratio in the range of 1/5-1/4 is favorable to the formation of the well-defined KCu_7S_4 NBs.

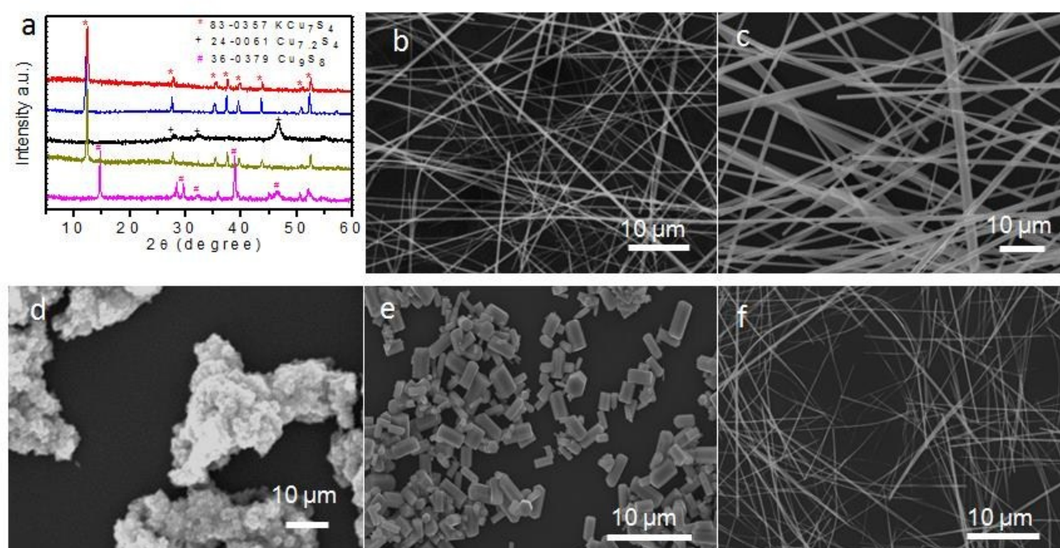

Figure 2 (a) XRD patterns and SEM images of the products obtained with (b) 3 g mixture of NaOH and KOH with Na/K ratio of 51.5:48.5, (c) 1.71g KOH and (d) 0.3 g KOH, and with different Cu/S molar ratios: (e) Cu:S = 1:2, (f) Cu:S = 1:5, respectively. The black, blue, red, brass, and magenta curves in (a) correspond to the product in (b), (c), (d), (e) and (f), respectively.

Bottom-gate field-effect transistors (FETs) based on the as-synthesized KCu_7S_4 NBs were then fabricated in order to further study their electrical property and conductivity. **Figure 3**a

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shows the schematic illustration of the individual KCu_7S_4 NB nano-FET. In this study, Au metal was selected as the electrode material in that it can form good contact to the KCu_7S_4 NB with very low contact resistance (Figure 3b). The resistivity of as-synthesized KCu_7S_4 NB is deduced to be in the range 0.2-1.2 mΩ·cm (see Figure 3c), with an average value of 0.6 mΩ·cm, which is slightly smaller than the resistivity for the stoichiometric $KCu_{7.00}S_4$ crystals (10 mΩ·cm), but larger than the resistivity for the nonstoichiometric phases $KCu_{7-x}S_4$ ($x \neq 0$, 0.1 mΩ·cm).[12] Further temperature-dependent resistance analysis in Figure 3d finds that the resistance decreased with the increase of the temperature in the range of 10~300 K, suggesting the semiconducting behavior of the KCu_7S_4 NBs.

Figure 3e shows the transport properties of the KCu_7S_4 NBs. The source-drain current (I_{ds}) *versus* source-drain voltage (V_{ds}) curves were measured under varied gate voltage (V_g) from -10 to +10 V with a step of 5 V. The decrease of conductance with increasing V_g confirms the *p*-type characteristic of the KCu_7S_4 NB. This electrical property can be ascribed to the intrinsic cation-deficient structure, that is, the 75% occupancy of the 1D tetrahedral Cu^+ cation chains to form the chemically reasonable formulation $KCu_3(Cu_4S_4)$ ($\equiv KCu_7S_4$).[12] Previously, a number of bottom-gate nanowire field effect transistor a number of tors (NWFETs) have been constructed to demonstrate the field-effect mobility of semiconductor nanowires (NWs).[21, 22] In this study, the hole mobility (μ_h) of the *p*-type KCu_7S_4 NB can be estimated by the following equation:

$$g_m = \partial I_{ds}/\partial V_g = (Z/L)\mu_h C_0 V_{ds}$$

where $g_m = \partial I_{ds}/\partial V_g$ represents the channel transconductance of the nano-MOSFET and is deduced from the slope of the $I_{ds} - V_g$ curve in the linear region (inset in Figure 3e) and Z/L is

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the width-to-length ratio of the NB channel. The capacitance per unit area is given by $C_0=\varepsilon_0 \varepsilon_{SiO_2}/h$, where ε_0 is the vacuum dielectric constant, ε_{SiO_2} is the dielectric constant of SiO_2 and h is the thickness of the SiO_2 gate dielectric layer.[23, 24] Based on the above equation, the hole mobility is calculated to be about 870 $cm^2\ V^{-1}s^{-1}$. Furthermore, the hole concentration (n_h) is deduced to be about $1.4\times10^{16}\ cm^{-3}$ through the equation $n_h=\sigma/q\mu_h$, where σ is the conductivity of the NBs and q is the elementary charge. The hole mobility is one order of magnitude higher than the reported value of β-Cu_2S with the comparable carrier concentration,[25] which may be attributed to the quasi-1D conduction path in the structure of KCu_7S_4.

The band gap of the semiconductors can be estimated by optical spectrum analysis. The UV-*vis*-NIR absorption spectrum of the as-synthesized KCu_7S_4 NBs (Figure 3f) presents a near-band-edge (NBE) absorption peak at 413 nm and a stronger near-infrared (NIR) absorption peak at 1226 nm. The inset in Figure 3f shows the corresponding $(\alpha hv)^2 - hv$ curve. As illustrated by the Kubelka-Munk function, the optical band gap of the as-synthesized KCu_7S_4 NBs can be deduced to be about 1.65 eV by extrapolating the linear region of the plot to intersect with the X-axis.[26] According to Alivisatos's study,[27] the strong absorption in NIR range corresponds to the localized surface plasma resonances (LSPR) due to the relatively high carrier (holes) concentration in the as-synthesized products, which may be useful for the application in the field of NIR photodetectors.

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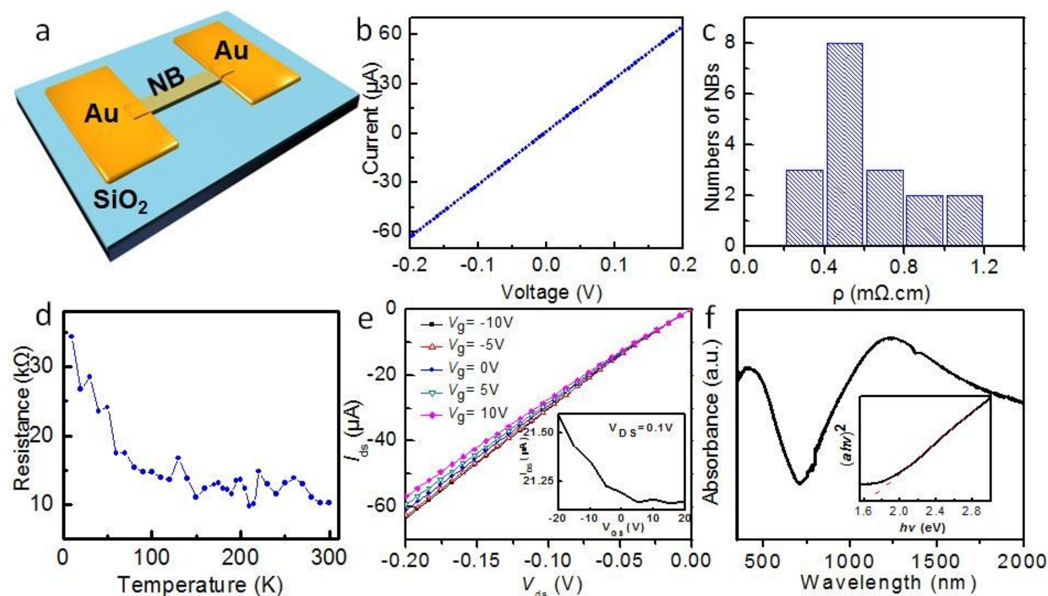

Figure 3 (a) Schematic illustration of the bottom-gate FET based on a single KCu_7S_4 NB. (b) A typical *I-V* curve of a single KCu_7S_4 NB in dark. (c) The distribution of resistivity values for 18 devices. (d) Temperature-dependent resistance of a single KCu_7S_4 NB. (e) I_{ds}–V_{ds} curves measured with V_g increasing from -10 V to 10 V with a step of 5 V, the inset shows the corresponding I_{ds}-V_g curve at V_{ds} = 0.1 V. (f) UV-*vis* absorption spectrum of KCu_7S_4 NB, the inset shows the corresponding $(\alpha h\nu)^2 - h\nu$ plot.

Previously, a number of chalcogenides (e.g. Ag_2S,[28] and $Cu_{2-x}Se$[29]) as well as copper-containing chalcogenides (such as Cu–doped SiO_2[30] and Cu–doped MoO_3[31]) have been employed to assemble metal–insulator–metal (MIM) memory devices.[32] Enlightened by these work, Au/KCu_7S_4 NB/Cu Schottky junction was constructed to explore the capability of the KCu_7S_4 NB for memory device application. **Figure 4**a depicts the current (*I*) – voltage (*V*) curves for the as-fabricated nano-device measured by a dc voltage sweeping from -0.4 V → 0 V → 0.8 V → 0V → -0.4 V (the bias was applied to the Au electrode and the Cu electrode was grounded) with a compliance current of 0.1 mA. It is obvious that the nanodevice displays well-defined current rectifying characteristic with a rectification ratio of up to 10^4. Considering the KCu_7S_4 NB/Au is a good *Ohmic* contact, the observed rectifying behavior can be exclusively ascribed to the KCu_7S_4 NB/Cu contact. In addition, a significant hysteresis loop

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can be observed in the forward voltage regime. That is, the device would be switched suddenly from the high resistance state (HRS or OFF state) to the low resistance state (LRS or ON state) at a set voltage (V_{set}) of ~ 0.5 V when the voltage swept from -0.4 V to 0.8 V. It would retain the ON state until the voltage swept back from 0.8 V to -0.4 V. Specifically, the OFF state occurred at the reset voltage (V_{reset}) of ~ 0.2 V. According to the *I-V* curve in a semi-logarithmic plot (Figure 4b), the conductance ratio of the ON/OFF states is larger than 10^4 at 0.4 V. The high coincidence of the initial cycle and the twenty subsequent cycles (shown in Figure 4c) as well as the relatively narrow V_{set} distribution of 18 devices (0.4 – 1.0 V, shown in Figure 4d) suggests the high uniformity and excellent reproducibility of the memory devices.

Figure 4e shows the retention characteristics of the ON and OFF states of the memory device measured in ambient air at room temperature at a read voltage of 0.4 V. It can be seen that the conductance ratio of 10^4 (~ 10^{-4} to 10^{-8}) can be stably retained for more than 1×10^4 s. To further disclose reproducibility of the devices, a pulsed voltage of ± 0.8 V was applied to repeatedly switch the device between ON and OFF states, after which, a smaller voltage 0.4 V was applied to read the resistance. As we can see from Figure 4f, the device can be reversibly switched between the ON and OFF states without obvious performance degradation. This stable retention and the reproducible switching behavior will enable the present KCu_7S_4 NB/Cu Schottky junction to be good building blocks for fabrication of high-performance memory devices.

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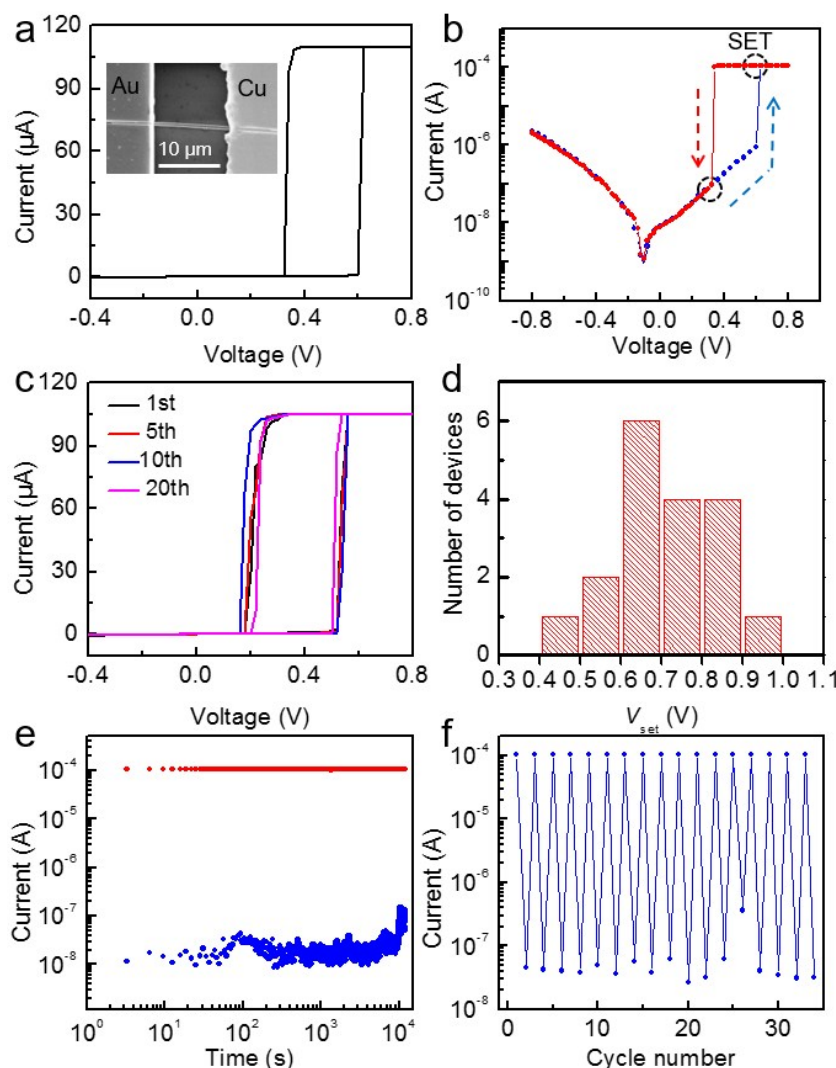

Figure 4 Typical *I-V* curves of the KCu_7S_4/Cu Schottky junction in (a) a linear scale and (b) a semi-logarithmic plot with a compliance current of 0.1 mA. The arrows indicate the voltage sweeping direction. Inset in (a) shows the typical SEM image of the device. (c) *I-V* curves of the device measured for twenty times in sequence. (d) Histogram of the set voltage distribution of 18 devices. (e) The retention performance of the device under a read voltage of 0.4 V. (f) The switching endurance for the first 30 cycles by applying a +0.8 V pulse for writing and a -0.8 V pulse for erasing.

A well-defined metal conducting filament model was previously proposed to unveil the resistive switching mechanism of nonvolatile memory device made of copper ionic materials. In this model, the resistive switching between "ON" and "OFF" states is related to the creation and annihilation of ultrathin Cu filament within copper chalcogenides at different bias voltages.[23] Although the as-synthesized KCu_7S_4 NBs contain a large quantity of copper ions in crystal structure, and the KCu_7S_4 NB based device indeed displays obvious memory

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behavior. However, such a memory device cannot be explained by the conducting filament theory in that the Cu^+ ions are largely confined within the 1D tetrahedral Cu^+ cation chains. As a result, a Cu^+ ion can move only by hopping into an adjacent vacancy site if available.[33] In addition, the Au/KCu_7S_4 NB *Ohmic* junction cannot account for the memory behavior as well as no detectable hysteresis loop appears in the backward voltage regime or when Au electrodes are used on both ends (**Figure 5**). To unveil the underlying mechanism behind this memory device, two more devices (Al/KCu_7S_4 NB and Si/KCu_7S_4 NB) were fabricated. **Figure 6** shows the schematic illustration of device structures and the *I-V* characteristics, from which, one can see that both devices exhibit obvious hysteresis loop with V_{set} of 7.2 and 5.8 V, respectively. Such a memory behavior, according to previous study, can be ascribed to the interfacial layer in which the oxygen vacancies in the unintentionally formed oxide film (AlO_x and SiO_2, respectively) were believed to serve as efficient trapping centers for electrons.[34, 35, 36] In light of this, we think the observed hysteresis loop in Cu/KCu_7S_4 NB may also originate from the unintentional interfacial oxide layer which is poorly crystalline and are commonly present on the surface of nanostructures fabricated by a low-temperature solution-based approach.[37]

For such a memory device, when a forward bias is applied across the KCu_7S_4 NB/Cu Schottky junction, electrons that drift from Cu electrode to KCu_7S_4 NB will be trapped by the interfacial layer where the oxygen vacancies in it will act as the trapping center for electrons. As a result, the junction weakens as the forward bias is increased or held for longer duration. This weakening effect is manifested by the abrupt turn-on of the forward *I-V* curve.[38] In this case, the memory device will be turned to an “ON” state (LRS) (**Figure 7**a), which corresponds to writing data into the device. When the forward bias is reduced (backward scan from positive

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to negative voltage), the trapped electrons will be gradually released and the weakened junction will reinstall gradually, resulting a hysteresis loop in the forward voltage regime. The device will be therefore turned to "OFF" state (HRS) (Figure 7b), corresponding to erasing data from the device.

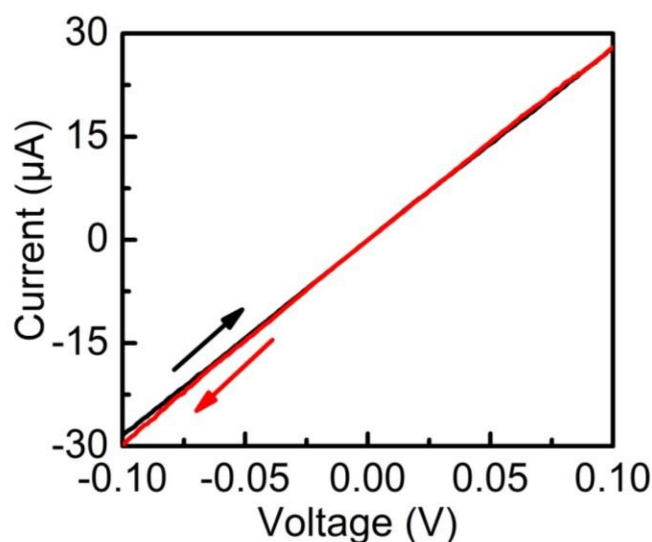

Figure 5 Typical *I-V* curve of a single KCu_7S_4 NB with Au electrodes at both ends under a dual sweep. The arrows indicate the voltage sweeping direction.

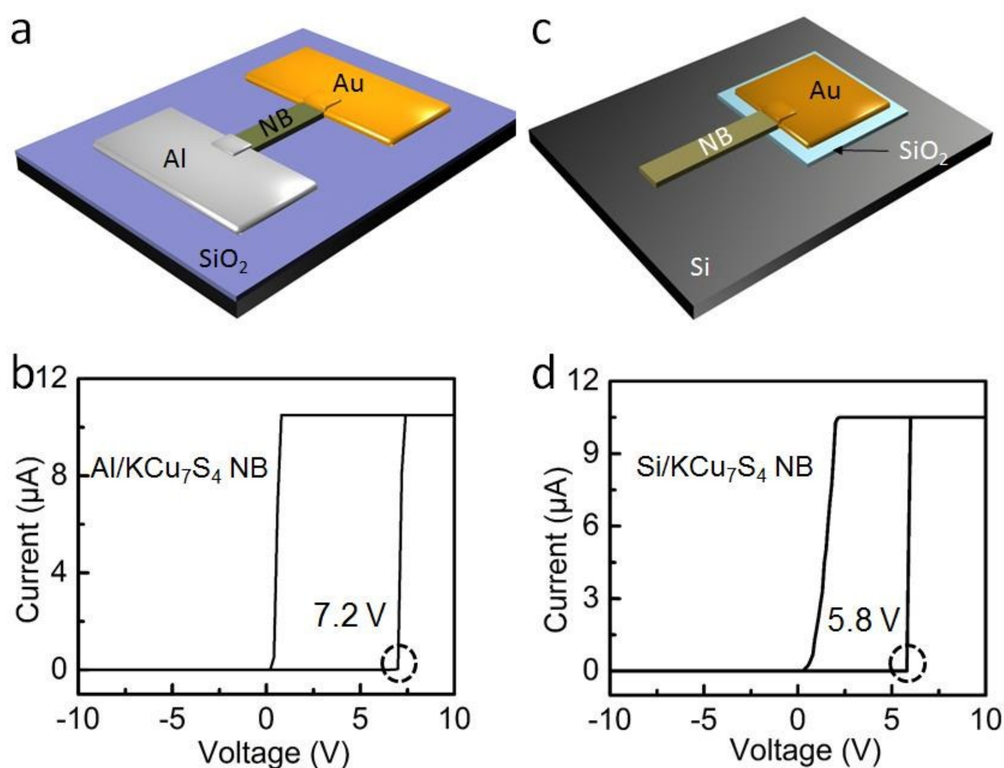

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Figure 6 (a) Schematic illustration of an Au/KCu_7S_4/Al heterojunction device, (b) the corresponding *I-V* curve of the device. (c) Schematic illustration of an Au/KCu_7S_4/Si heterojunction device, (d) the corresponding *I-V* curve of the device.

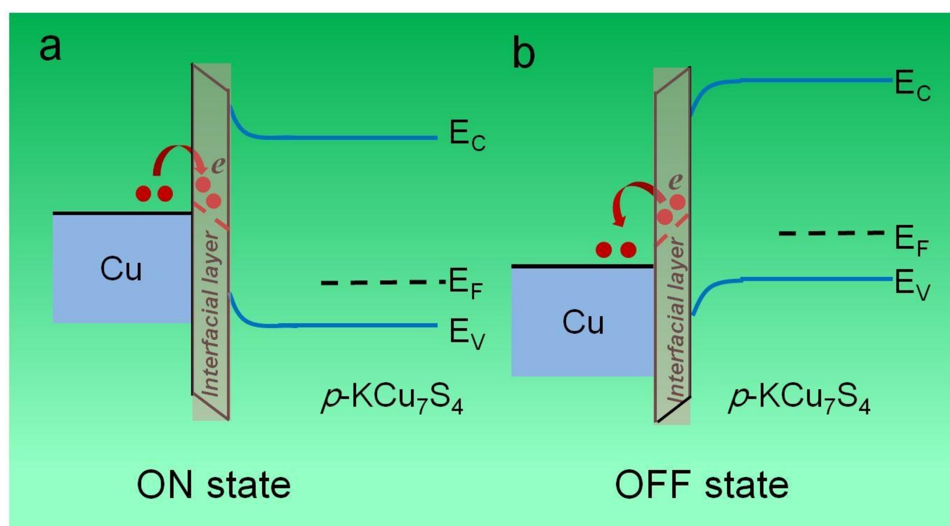

Figure 7 (a) Schematic energy band diagram for the KCu_7S_4 NB /Cu Schottky junction in the ON state when a forward bias is applied to the Au electrode. The electrons are trapped in the interface state. (b) Schematic energy band diagram for the device in the OFF state when a reverse bias is applied to the Au electrode. The trapped electrons are released to the Cu electrode.

Table 1 compares the key parameters of the present and other interfacial layer-induced memory devices. It can be seen that the retention time and on/off ratio of the present KCu_7S_4/Cu memory device is poorer than other devices, including *p*-CdTe/Al, and *p*-ZnS/*n*-Si. However, it is undeniable that our device has a low set voltage of 0.4-1 V, which is much smaller than other devices with similar geometries. Such a relatively small set voltage may be attributed to the higher conductivity of the Cu-based interfacial oxide layer and the limited trapping capability compared with the insulating oxide layer (e.g. AlO_x and SiO_2) in other devices.

Table 1. Key parameters comparison of the present and other devices with similar geometry.

Memory media	Operation mechanism	V_{set}	I_{on}/I_{off}	Retention time	Ref
KCu_7S_4/Cu	Interfacial layer (CuO_x)	0.4-1.0 V	~ 10^4	>10^4 s	This work

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p-CdTe/Al	Interfacial layer (AlO_x)	6-8 V	~ 10^6	3×10^4 s	[34]
p-ZnS/*n*-Si	Interfacial layer (SiO_2)	2.7-3.3 V	~ 10^6	~10^5 s	[35]
Ti/CuO_x/Pt	Interfacial oxygen migration	~ 0.8V	> 100	--	[37]
Cu_2S/ZnO	Mobility of Cu^+	0.1-0.4V	~ 10^4	--	[38]

Conclusions

In summary, tetragonal KCu_7S_4 NBs with width of 200-600 nm and length of up to hundreds of micrometers were synthesized through a low-temperature solution approach. Electrical characterization reveals that the as-synthesized KCu_7S_4 NBs are *p*-type semiconductors with a high hole mobility of about 870 cm^2 V^{-1} s^{-1}, which may be attributed to the quasi-1D conduction path along the *c* axis in the structure of KCu_7S_4. Further study found that the KCu_7S_4/Cu Schottky junction shows a reproducible memory characteristic with a set voltage of 0.4-1.0 V, a current ON/OFF ratio of about 10^4, and a retention time large than 10^4 s, which is comparable to other memory devices with similar configuration. This study will offer the opportunity for promising applications in high-performance and low-consumption nonvolatile memory devices.

Acknowledgments

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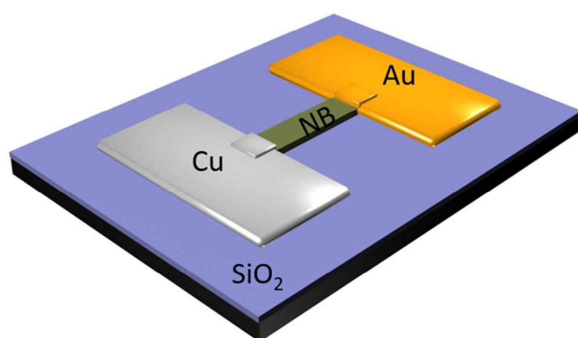
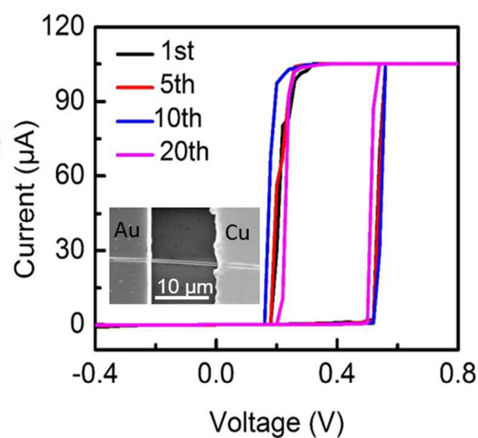
Graphical abstract

A nonvolatile memory nano-device was fabricated from KCu_7S_4 nanobelts which were synthesized by a low-temperature solution approach. Electrical study reveals that the KCu_7S_4/Cu Schottky junction devices display typical resistive switching characteristics with a low set voltage of 0.4-1 V, and a current ON/OFF ratio of about 10^4, and a retention time > 10^4 s.





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