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## Forming and compliance-free operation of low-energy, fast-switching $\text{HfO}_x\text{S}_y/\text{HfS}_2$ memristors†

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We demonstrate low energy, forming and compliance-free operation of a resistive memory obtained by the partial oxidation of a two-dimensional layered van-der-Waals semiconductor: hafnium disulfide ( $\text{HfS}_2$ ). Semiconductor–oxide heterostructures are achieved by low temperature ( $<300^\circ\text{C}$ ) thermal oxidation of  $\text{HfS}_2$  under dry conditions, carefully controlling process parameters. The resulting  $\text{HfO}_x\text{S}_y/\text{HfS}_2$  heterostructures are integrated between metal contacts, forming vertical crossbar devices. Forming-free, compliance-free resistive switching between non-volatile states is demonstrated by applying voltage pulses and measuring the current response in time. We show non-volatile memory operation with an  $R_{\text{ON}}/R_{\text{OFF}}$  of 102, programmable by 80 ns WRITE and ERASE operations. Multiple stable resistance states are achieved by modulating pulse width and amplitude, down to 60 ns,  $<20$  pJ operation. This demonstrates the capability of these devices for low-energy, fast-switching and multi-state programming. Resistance states were retained without fail at  $150^\circ\text{C}$  over  $10^4$  s, showcasing the potential of these devices for long retention times and resilience to ageing. Low-energy resistive switching measurements were repeated under vacuum (8.6 mbar) showing unchanged characteristics and no dependence of the device on surrounding oxygen or water vapour. Using a technology computer-aided design (TCAD) tool, we explore the role of the semiconductor layer in tuning the device conductance and driving gradual resistive switching in 2D  $\text{HfO}_x$ -based devices.

### New concepts

We employ a low-temperature, dry oxidation method to partially convert an  $\text{HfS}_2$  crystal to a vertical  $\text{HfO}_x\text{S}_y/\text{HfS}_2$  structure. As opposed to most other works on oxidation-conversion of 2D semiconductors, our process results in a thin, highly crystalline oxide–semiconductor heterostructure with almost perfect interfaces. Crossbar-arrays of amorphous oxide-based memristors typically require peripheral circuitry to enable electroforming (a one-time process required to initialise the devices) and current compliance circuitry (to limit high currents which may damage the devices). Both of these requirements hinder energy consumption, computation time and integration density in machine learning and neuromorphic applications. Devices which exhibit forming-free and compliance-free operation have been investigated previously; however, they typically exhibit resistive switching with a low ON/OFF ratio and/or require fabrication processes which are incompatible with CMOS. By using thermally-grown  $\text{HfO}_x\text{S}_y/\text{HfS}_2$  structures, we demonstrate electroforming-free and compliance-free, non-volatile resistive switching while maintaining a good ON/OFF ratio and a CMOS-compatible thermal budget. Our devices also show multiple resistive states, as well as stability at high temperatures and under vacuum. Using TCAD simulations, we demonstrate that the  $\text{HfS}_2$  semiconducting layer enables the engineering of ON currents. We also show that the mechanism responsible for the forming-free and compliance-free resistive switching in the device is non-filamentary, unlike most oxide-based memristors.

## Introduction

The growing demand for data-driven computation in artificial intelligence (AI) and machine learning (ML) applications has skyrocketed energy consumption from modern data centres, with estimates showing that global yearly usage from this sector surpasses 200 TW-hours per year. This figure is predicted to rise by an order of magnitude by 2030<sup>1</sup> highlighting the growing need to address this problem.<sup>2</sup> One fundamental issue lies in the von Neumann architecture used for computation, which physically separates processing and memory units. The shuttling of data back and forth between such processing and memory units inevitably wastes energy and increases computation time. Neuromorphic computing aims to address this by taking inspiration from the human brain—a biological

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“computer” capable of performing complex tasks with far higher efficiency. For example, Google DeepMind’s AlphaGo model requires the use of 1920 CPUs and 280 GPUs and consumes  $\sim 1$  MW power to play the boardgame Go (inference) against a human player. Comparatively, the human brain uses only  $\sim 20$  W for the same task.<sup>3,4</sup> One feature of the brain directly responsible for this discrepancy is the co-location of processing and memory in an extensive network of neurons and synapses. In combination with other factors, this means that handling noisy and unstructured data is a relatively unremarkable task for the human brain, enabling us to quickly, reliably and efficiently tackle complex problems. Even when handled by the best artificial neural networks (ANN) running on modern hardware, most ML and AI implementations require extensive and costly training, consume large amounts of power and require frequent retraining.<sup>5</sup> Therefore, it is clear that for computing tasks which benefit from quick and efficient processing of noisy input data, brain-like (neuromorphic) computation is necessary.<sup>6</sup>

To implement neuromorphic computations, we can take inspiration from the brain and develop systems which allow computations in memory. A common approach is to use crossbar arrays of densely-packed non-volatile memory (NVM) devices in deep neural networks (DNN) or spiking neural networks (SNN).<sup>7</sup> Usually, the NVM devices forming the building blocks of crossbar arrays are memristors. Memristors are two-terminal, non-linear devices with inherent memory and represent a leading candidate for hardware implementations of neuromorphic computing.<sup>8</sup> They have the ability to modulate their resistance between distinct states by the application of electrical stress, such as ramped or pulsed voltages. Crucially, they retain their programmed resistance even when the electrical stress is removed.<sup>9</sup>

Non-volatile resistive switching in solid-state devices based on titanium oxide thin films has been observed as early as 1960,<sup>10</sup> with the memristor first being formally described in 1971 by Leon Chua.<sup>9</sup> More recent interest in ReRAM memristive technology was sparked in 2008 when devices based on thin titanium oxide films were once again investigated, this time directly addressing Chua’s memristor framework,<sup>11</sup> and later when memristors were integrated in silicon suboxide films.<sup>12</sup> Since then, the field has flourished, with improvements in our understanding of the switching mechanisms of ReRAM devices,<sup>13,14</sup> the performance of each individual element,<sup>15–17</sup> scaling<sup>18–20</sup> and different material systems. One particular material that we will investigate is hafnium oxide ( $\text{HfO}_x$ ), sometimes referred to as hafnia. Hafnium oxide is part of a class of materials called high- $k$  dielectrics. High- $k$  dielectrics are so named as they possess a high dielectric constant compared to  $\text{SiO}_2$ , which allows the use of thicker layers in metal oxide semiconductor (MOS) capacitors to suppress tunnelling while maintaining large capacitance.<sup>21</sup> In memristive applications  $\text{HfO}_x$ -based devices fabricated by sputtering or atomic layer deposition (ALD) have already demonstrated low-energy switching, a high degree of scalability, signal processing, image compression and convolutional filtering,<sup>22</sup> good endurance<sup>23</sup> and synaptic applications<sup>24,25</sup> although there has

been a collective desire to increase programming linearity in synaptic applications and reduce the individual memristor power consumption.<sup>26</sup> One potential avenue of investigation for fabricating low-power memristors is to look at 2D layered materials (2DLMs).

Since the ground-breaking experiment where single layers of graphene were isolated and their electron transport was investigated,<sup>27</sup> several more 2DLMs have been discovered with thousands more predicted to exist.<sup>28</sup> They often have unique properties which highlight a key interest in their research. In particular, 2DLMs present the opportunity to fabricate devices with atomic precision of thicknesses down to a single atomic layer, with chemically abrupt surfaces and no dangling bonds.<sup>17,29–33</sup> This allows devices with a wide range of properties and applications to be realised, combining different materials with varying properties with ease.<sup>33</sup> Wafer-scale growth of desired 2DLMs for memristors by chemical vapour deposition (CVD) has been developed,<sup>19</sup> with pilot lines already established. For example, memristors fabricated from wafer-scale CVD hexagonal boron nitride (hBN) have shown both a high ON/OFF ratio of  $10^{11}$  and energy consumption as low as 8.8 zJ, demonstrating the potential of this technology.<sup>29,34</sup> However, sample-to-sample variation and poor control of defect densities present in the films make them as-yet unsuitable for at-scale fabrication of memristors.<sup>35</sup> Another scalable fabrication technique that has been demonstrated with 2D materials of particular interest is the template growth of ultrathin oxides from semiconducting crystals. Starting from a near-perfect crystalline 2DLM, native oxides can be formed by partially oxidising semiconducting crystals with almost perfect interfaces, using plasma oxidation,<sup>36–38</sup> thermal oxidation<sup>39</sup> or photo-oxidation.<sup>40</sup> Native oxides obtained by plasma oxidation of a starting 2D crystal have shown promising memristive behaviour in work done on  $\text{GaS}$ <sup>36</sup> and  $\text{HfSe}_2$ <sup>37</sup> memristors. Recently,  $\text{GaS}_x\text{O}_y/\text{GaS}$  memristors with an ultrathin oxide and a clean interface have been demonstrated, showing low energy  $\sim 0.22$  nJ operation.<sup>36</sup> Similarly, plasma oxidised  $\text{HfO}_x\text{Se}_y/\text{HfSe}_2$  memristors have also been fabricated, demonstrating operation at low current compliance (100 pA) and low energy (0.1 fJ) in filamentary resistance switching.<sup>37</sup>

Despite the excellent performance being demonstrated in many memristors, devices which can be operated without the requirement for compliance or electroforming are even more desirable to reduce the power consumption, operation time and integration area cost of utilising memristors as synaptic weights in neuromorphic chips, improving efficiency.<sup>41</sup> The peripheral circuitry and transistor-memristor (1T1M) architectures required to integrate most ReRAM memristors into neuromorphic and ML chips provide a high barrier to their adoption.<sup>41,42</sup> A few fabrication methods have shown promise in this regard. Methods which engineer a large proportion of oxygen vacancies in the pristine device such as  $\text{H}_2$  annealing or using a Ti electrode gettering layer have been largely successful in promoting forming-free behaviour in  $\text{ZnO}$ <sup>42</sup> and  $\text{Ta}_2\text{O}_5$  memristors,<sup>43</sup> respectively. However, the highly defective oxide switching layers inducing forming-free resistive switching also necessitate the application of current compliance to prevent



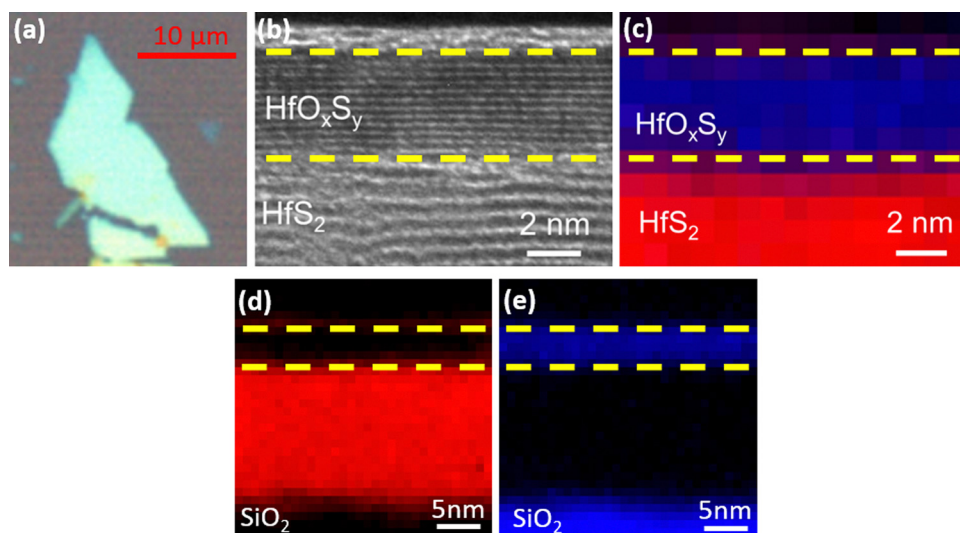
high currents from damaging the device.<sup>42,43</sup>  $\text{SnO}_x$  ReRAM devices have been shown to exhibit both forming and compliance-free resistive switching. The forming-free behaviour is thought to be due to the ultra-thin oxide used<sup>41</sup> and the compliance-free nature of this device is thought to be a result of the  $\text{TiO}_{2-x}$  interfacial layer acting as a series resistor, limiting currents and driving gradual resistive switching. However, devices which exhibit forming and compliance-free or gradual switching properties typically show a low  $R_{\text{ON}}/R_{\text{OFF}}$ ,<sup>41,44</sup> or employ fabrication techniques incompatible with CMOS.<sup>45,46</sup>

This presents a technological challenge: to fabricate devices which can combine strong non-volatile memory characteristics such as resistive switching at low energy and stable retention (found in many abrupt switching devices), while allowing for nearly continuous multi-level switching, high integration density and simplified operation without electroforming or compliance (which can be found in many gradual switching devices.) In this work, we address this by investigating the use of  $\text{HfO}_x\text{S}_y/\text{HfS}_2$  structures where a thin  $\text{HfO}_x\text{S}_y$  oxide is obtained by partial oxidation of 2D  $\text{HfS}_2$  crystals for resistive memories. The oxidation of  $\text{HfS}_2$  flakes has already been demonstrated by a wet oxidation (thermal oxidation in ambient) method<sup>39</sup> and by a plasma partial oxidation method, demonstrating the application of such crossbar structures in flash memory.<sup>38</sup> Instead, here we investigate a controlled dry oxidation method to produce  $\text{HfO}_x\text{S}_y/\text{HfS}_2$  heterostructures to be used in memristive devices. We show that our devices behave as non-volatile memory devices without requiring an electroforming initialisation step or current compliance for their operation. The memristors show fast and low-energy operation, consuming as little as  $\sim 20$  pJ per switching cycle with 60 ns programming pulses. Moreover, we also demonstrate good  $R_{\text{ON}}/R_{\text{OFF}}$  and stable state retention of multiple states over  $10^4$  s at  $150^\circ\text{C}$ .

## Material preparation and characterisation

$\text{HfS}_2$  flakes were deposited onto oxidized silicon wafers by mechanical exfoliation. The flakes were then oxidised using a low-temperature 110-minute dry thermal oxidation method, carefully controlling pressure, temperature, oxygen flow rate and time. The low temperature ( $<300^\circ\text{C}$ ) oxidation process allows us to conduct this step even after transfer onto metal contacts and is well below the CMOS compatibility limit of  $<450^\circ\text{C}$ .<sup>47</sup>

To gain insight into the structure of the oxide, we investigated a partially oxidised  $\text{HfS}_2$  flake (Fig. 1a) using cross-sectional transmission electron microscopy (TEM, Fig. 1b). The atomic arrangement in the sample appears to be ordered in both the semiconductor and oxide regions, supporting the idea of a crystalline or large-domain polycrystalline oxide being formed, which is quite different from other oxides achieved by converting (predominantly by plasma and ambient/wet thermal) 2DLMs to their native oxides.<sup>37–39,48–50</sup> The sample was oxidised under dry conditions but perhaps crucially oxidised at low temperature and cooled in an oxygen-free environment, as this has been seen to produce crystalline oxides in other oxidation-conversion work involving transition metal dichalcogenides (TMDs).<sup>51</sup> The oxide formed with the parameters detailed in the Methods section is 4 nm thick; however, this is a process dependent property. The electron energy loss spectroscopy (EELS) maps (Fig. 1c) show that there is a clear separation of semiconductor (Fig. 1d) and oxide (Fig. 1e) regions with a good interface, however in the top region of Fig. 1c and d, a sulfide layer can be observed. The origin of this region is not known, however it could be related to the displacement of sulphur species during oxidation. Furthermore, a small amount of sulphur is present in the oxide layer (Fig. 1d), hence



**Fig. 1** (a) Optical microscopy image of  $\text{HfO}_x\text{S}_y/\text{HfS}_2$  flakes before being transferred to lamella for transmission electron microscopy (TEM). (b) Cross-sectional TEM image of partially oxidised flake shows crystallinity of the resulting oxide layer and (c) electron energy-loss spectroscopy (EELS) mapping of (d) sulfur (red) and (e) oxygen (blue) demonstrates a clear separation of the  $\text{HfO}_x\text{S}_y$  and  $\text{HfS}_2$  regions.



the designation  $\text{HfO}_x\text{S}_y$ . The process-dependent oxide thicknesses and characteristics were also studied with spectroscopic imaging ellipsometry (SIE) in good agreement with the TEM data (Fig. S1, ESI†).

## Electrical measurements

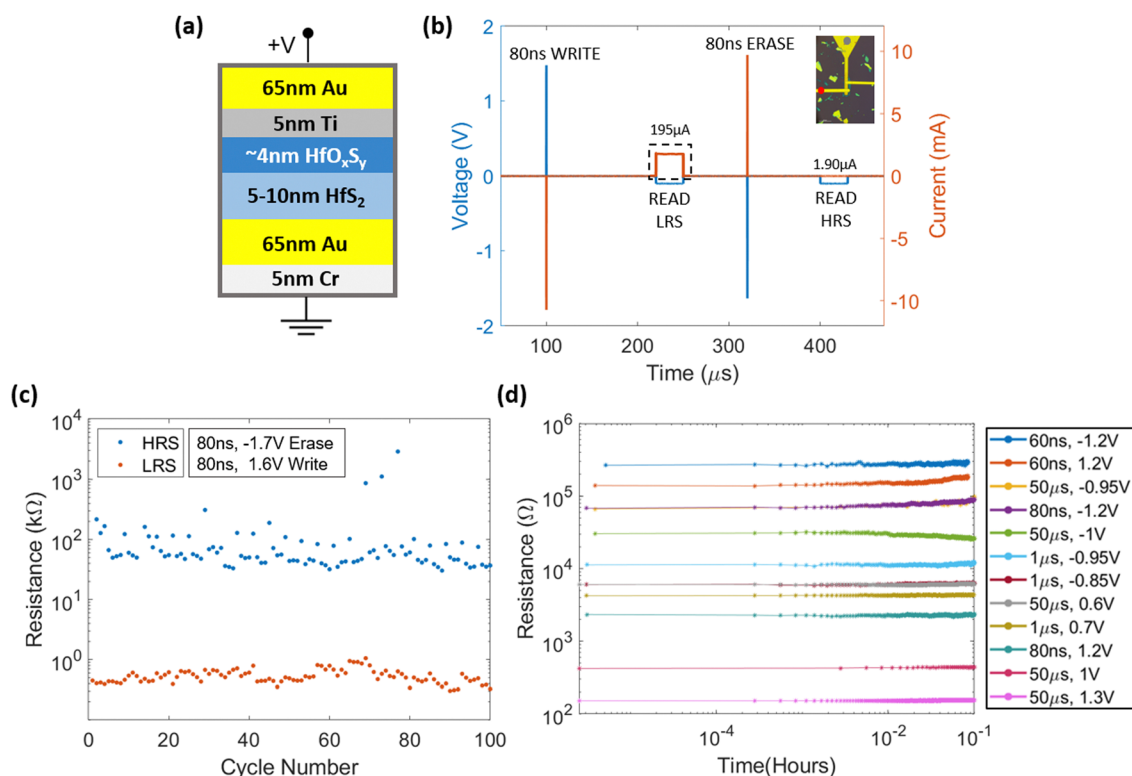
### Pulsed switching

$\text{HfO}_x\text{S}_y/\text{HfS}_2$  memristive devices were fabricated using the oxidation method briefly described previously (and in detail in the Methods section), resulting in the structure shown in Fig. 2a. To examine the performance characteristics of our devices which determine their capability for integration in ML and neuromorphic applications, we applied voltage pulses and measured the current response in time. The voltage was applied to the top electrode while keeping the bottom electrode grounded. The device was SET from a high resistance state (HRS) to a low resistance state (LRS) during the WRITE operation, which was programmed as a pulse with a 20 ns rise and fall time, held at 1.6 V for 80 ns (Fig. 2b). The ERASE operation allowed the device to RESET its resistance from LRS back to HRS and was applied just as the WRITE operation, but at  $-1.7$  V instead. READ operations were performed at  $-0.1$  V over a significantly longer time (30  $\mu\text{s}$ ) and all pulses were spaced  $\sim 75$   $\mu\text{s}$  apart to avoid any spurious contribution to the current originating from charge

and discharge from parasitic capacitances. The device exhibited reproducible resistive switching over the 100 cycles tested (Fig. 2c), switching between  $0.51$   $\text{k}\Omega$  and  $52.5$   $\text{k}\Omega$  resistance states for LRS and HRS, respectively.

Importantly, no IV sweep characterisation or electroforming was conducted to initialise these devices prior to their initial pulsed testing to avoid any effect resulting from previous testing that might modify their switching behaviour. In fact, resistive switching has been achieved in these devices without electroforming or current compliance, which is unusual for  $\text{HfO}_x$ -based devices and provides a significant advantage for their integration in circuits.<sup>41,42,52</sup> Although many memristive devices show excellent performance and scalability, they require peripheral circuitry for electroforming, and integration into transistor-memristor (1T1M) architectures to limit high currents that would otherwise permanently damage the device. These factors not only hinder integration density and complicate peripheral control circuitry, but they also increase computation time and increase energy costs, reducing the applicability for many memristive devices into neuromorphic or dedicated ML chips.<sup>41,42</sup> Dedicated circuitry for electroforming and current compliance would not be required to operate our thermally oxidised  $\text{HfO}_x\text{S}_y/\text{HfS}_2$  memristors, highlighting one of the key merits of these devices.

By integrating the current over the pulse programmed WRITE and ERASE times and multiplying by the programmed



**Fig. 2** (a) Schematic of typical devices fabricated using the dry oxidation method. (b) Pulsed voltage test applied to the device with an associated current response showing non-volatile WRITE and ERASE operations (READ currents expanded for visibility). Energy = 1.3 nJ for WRITE and ERASE. (c) 100 cycle state distribution of LRS and HRS with 80 ns, 1.6 V WRITE pulses and 80 ns,  $-1.7$  V ERASE pulses, resulting in a  $R_{\text{ON}}/R_{\text{OFF}}$  of 102. (d) Multiple stable resistance states are achievable by varying pulse width and amplitude.



voltage, respectively, the WRITE and ERASE energies for each operation can be estimated to be  $\sim 1.3$  nJ. A good  $R_{\text{ON}}/R_{\text{OFF}}$  of 102 and resistive switching with minimal state conductance drift was observed (Fig. 2c). This demonstrates that this device can be used for stable, low energy resistive switching with a good  $R_{\text{ON}}/R_{\text{OFF}}$ . 60 ns pulse width WRITE and ERASE operations have also been investigated (see the ESI,† Fig. S3e). With 60 ns switching, we observe even lower WRITE and ERASE energies of 16.5 pJ and 17 pJ, respectively, for the few cycles investigated. Such fast pulses are at the absolute maximum temporal resolution of the parameter analyzer and remote sensing unit setup (Keysight B1500A + waveform generator fast measurement unit–WGFMU) and for cross-point devices on  $\text{SiO}_2/\text{Si}$  substrates which can exhibit significant capacitive effects. Therefore, all pulse widths employed were verified with an oscilloscope connected to a remote sensing unit at the voltage input terminal of the memristor (Fig. S3a–d, ESI†).

Fig. 2d shows a variety of resistance states achievable by programming a single device with different pulse widths and voltages, and the retention characteristics of these states. Notably, the range of resistance states accessible in the device spans 3 orders of magnitude, which is significant for circuit applications of multi-level memristive devices. Using this variable conductance behaviour in pulse-width or amplitude modulation pulsing schemes,<sup>46</sup> further experiments should be conducted to demonstrate potentiation and depression with linear and high-granularity weight update, taking advantage of the wide range of stable resistance states available.

### Device stability

For integration in modern machine learning hardware, a non-volatile memory device should not only show the ability to switch repeatedly between multiple distinct resistance states, but it should also show good retention of programmed resistance states and no dependence on external factors (other than applied voltage pulses) for its operation. To test the state retention of our devices, we programmed several distinct resistance states in a fresh device (different from the one shown

in Section 2.1 and not previously subjected to any voltage stress), using 80 ns,  $\sim \pm 0.9$ –1.7 V pulses and observed the resistance drift at an elevated temperature in a moderate vacuum (Fig. 3a). Resistance states were read at 0.1 V every second over  $10^4$  s. The LRS and HRS states at 150 °C observed in the device range from  $\sim 20$  k $\Omega$  to 0.15 k $\Omega$  regime, respectively. Crucially, all the states investigated were stable at each temperature throughout the  $10^4$  s testing period, despite the relatively aggressive testing conditions. Testing the retention of the device at temperatures higher than room temperature accelerates the ageing processes inside the device which typically leads to failed state retention. Therefore, the stable retention at elevated temperatures demonstrates the potential for long retention of multiple resistance states in these devices.

To exclude the influence of water vapour or oxygen in the surrounding air from the device operation, we measured the devices in an 8.6 mbar vacuum environment (Fig. 3b), applying similar programming pulses to before (80 ns, 1.5 V WRITE and  $-1.9$  V ERASE). The operation of the device is unaffected by the vacuum environment, demonstrating that it is not dependent on any external factors such as oxygen or moisture. This is an important demonstration of the feasibility for integration of  $\text{HfO}_x\text{S}_y/\text{HfS}_2$  devices with existing technological practices, such as the use of passivation layers in CMOS applications. Passivation layers bury the device in a dielectric material which is used to protect and stabilise them. Therefore, memristors integrated in neuromorphic chips or crossbar arrays would have to operate independently of their surroundings, in an oxygen-free environment, which we demonstrate here.

Overall, investigating devices by pulsed voltage is critical from a technological perspective: to demonstrate their capability for integration in ML and neuromorphic applications. Our  $\text{HfO}_x\text{S}_y/\text{HfS}_2$  memristors switch independently of atmospheric oxygen and moisture, at low energy, responding to fast voltage pulses while providing good  $R_{\text{ON}}/R_{\text{OFF}}$ . They demonstrate tuneable conductance within a wide range of values and strong resilience to temperature and ageing over time. Crucially, we are able to operate these devices without an electroforming initialisation

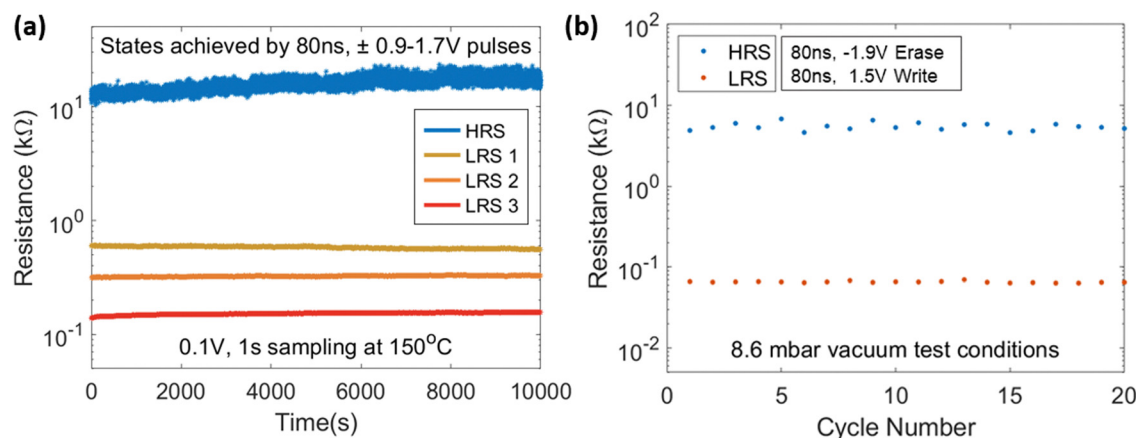


Fig. 3 (a) Non-volatile states achieved by 80 ns pulse programming are retained over  $10^4$  s at 150 °C. (b) Pulsed voltage resistance switching unaffected by operating device in an 8.6 mbar vacuum environment.

step or requiring any complex current compliance circuitry. This unique combination of desirable performance characteristics highlights the need for further investigation into wafer-scale and simulation-based implementations of such devices in neural networks for explicit machine learning or neuromorphic tasks. However, to design a scalable technological node which can harness these desirable characteristics, it is therefore equally important to understand the likely complex underlying mechanisms responsible for resistive switching in these devices.

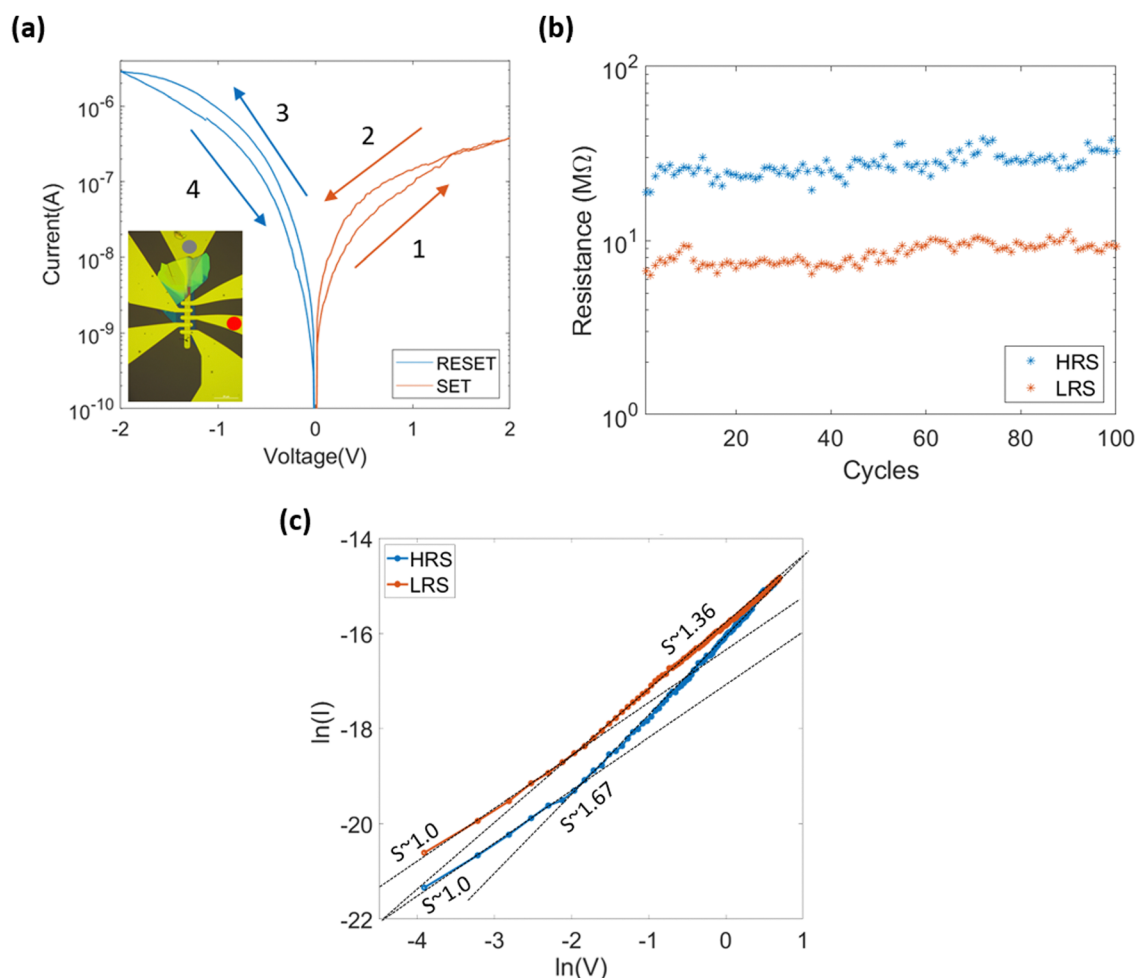
### Voltage ramps

While pulsed voltage resistance switching demonstrates the performance and efficiency of the device in a realistic application, the mechanisms behind the resistive switching in the device are better studied by ramping the voltage applied to the top contact of the device and inspecting the current output. This is particularly important for our devices as they employ an uncommon structure and morphology for a vertical memristive device. To do so, we tested a different device which was not previously exposed to any voltage stress. The device, shown in

the inset of figure Fig. 4a, is nominally identical to the one used for pulsed switching, with the only difference being the thickness of the semiconductor. The device was characterised using IV sweeps (Fig. 4a) and the representative IV characteristics shown in Fig. 4a were produced without requiring an initial electroforming step or current compliance just as before and with the device initially in its HRS. The HRS and LRS evolution over 100 SET/RESET cycles are presented (Fig. 4b).

The device operates at low SET and RESET currents, reading 26 nA at  $-0.2$  V ( $\sim 7.7$  M $\Omega$ ) in LRS compared to 7.4 nA at  $-0.2$  V ( $\sim 27$  M $\Omega$ ) in HRS (Fig. 4b). The higher resistance of these devices compared to those in Fig. 2 is likely due to differences in device thickness and sample-to-sample variation. For the same oxidation parameters but higher initial HfS<sub>2</sub> thicknesses, the remaining thickness of un-oxidised HfS<sub>2</sub> in the device will be greater. This, in turn, reduces peak currents in the device (Fig. S6, ESI†) presenting a method for tuning the conductance and energy consumption of the device.

The stark difference in  $R_{\text{ON}}/R_{\text{OFF}}$  in the more technologically relevant fast pulsed operation scheme (Fig. 2 – higher  $R_{\text{ON}}/R_{\text{OFF}}$ )



**Fig. 4** (a) Forming and compliance-free, gradual resistance switching of the device shown in the inset. From (b), consistent resistive switching endurance can be observed, with the resistance gradually increasing over cycles. (c) The lack of an abrupt filament formation prevents a runaway region from appearing in the  $\ln I$  IV plot of a representative SET cycle from which we can assume transport characteristics.

compared to the ramped voltage scheme used here to investigate transport in the device (Fig. 4) can be explained by the effect of Joule heating. Factors which are known to limit peak LRS conductance and hinder stability during switching such as Joule heating typically dominate over longer timescales.<sup>53</sup> This may explain the lower  $R_{\text{ON}}/R_{\text{OFF}}$  of the device in Fig. 4, investigated with long-timescale IV sweeps, despite the higher voltages used in this instance. We have observed very similar  $R_{\text{ON}}/R_{\text{OFF}}$  and IV sweep characteristics even in more conductive devices. Near the SET voltage of  $\sim 1.45$  V in Fig. 4a, a small rise in conductance can be observed, but this is suppressed in IV sweep operation, likely contributed to by Joule heating and other conductance-limiting mechanisms in the device. Hence, maintaining fast switching timescales  $\sim 80$  ns in pulsed operation allows for a larger conductance modulation than with voltage ramps (Fig. 4) resulting in a higher  $R_{\text{ON}}/R_{\text{OFF}}$ .<sup>53</sup>

In order to identify the dominating transport mechanisms, we analyse the natural logarithm of  $V$  and  $I$  for a representative SET voltage sweep, shown in Fig. 4c. The characteristics of these IV sweeps are representative of the resistance switching observed in all the devices we have fabricated with this method. The HRS and LRS portions of the SET curve are represented by blue and orange lines, respectively. In contrast to other similar devices,<sup>37</sup> there is no abrupt and dramatic increase in conductance at the SET voltage, as described previously. This implies a conductance-mediated switching behaviour where, rather than breakdown effects such as electrode-bridging conductive filaments being formed,<sup>20</sup> resistive switching is primarily caused by the overall field-induced redistribution of movable defects (such as oxygen vacancies) in the device.<sup>54</sup> The electrical transport in the device seems to initially follow trap-controlled space charge limited conduction (SCLC), where there is an ohmic regime at a low voltage such that  $\ln(I) \sim \ln(V)$ , then a region where the proportionality increases to  $\sim 1.67$  emerges closer to the relationship described by Child's law. However after this step, there is no dramatic runaway current region, yet the device still switches to an LRS. Most  $\text{HfO}_x$ -based devices show Schottky emission in the high field HRS region,<sup>37,55</sup> however this is not the case in our devices. As opposed to the more commonly used (*e.g.* as a gate dielectric) amorphous  $\text{HfO}_x$  with low defect densities,<sup>42,56</sup> from TEM we have observed a crystalline oxide with sulfur defects present (Fig. 1) and out-of-plane defect pathways (Fig. S2, ESI†). Other 2D material based memristive devices have shown the ability to produce low current and forming-free devices such as ours, due to pre-existing defect pathways along domain walls in (poly)crystalline oxide.<sup>45</sup> Due to the applied field, the conductivity of this pathway could be mediated by oxygen ion or vacancy diffusion<sup>57</sup> as described in the conductance-mediated picture.<sup>54</sup> As the applied positive voltage from the top electrode causes the oxide region to become more sub-stoichiometric due to oxygen ion migration into the Ti electrode,<sup>58</sup> the resistance of the oxide region can be modulated without completely breaking it down or forming a continuous metallic filament.<sup>54,57</sup>

In the LRS the electrical transport is also rather complex showing an initial relationship of  $\ln(I) \sim 1.36 \ln(V)$  at high field,

then an ohmic region at low field. This may be due to the semiconductor-oxide nature of our device, providing two additional junctions, one of which may be rectifying. These are not normally present in memristive devices, and the out-of-plane transport through the  $\text{HfS}_2$  further complicates the picture.

## TCAD simulation

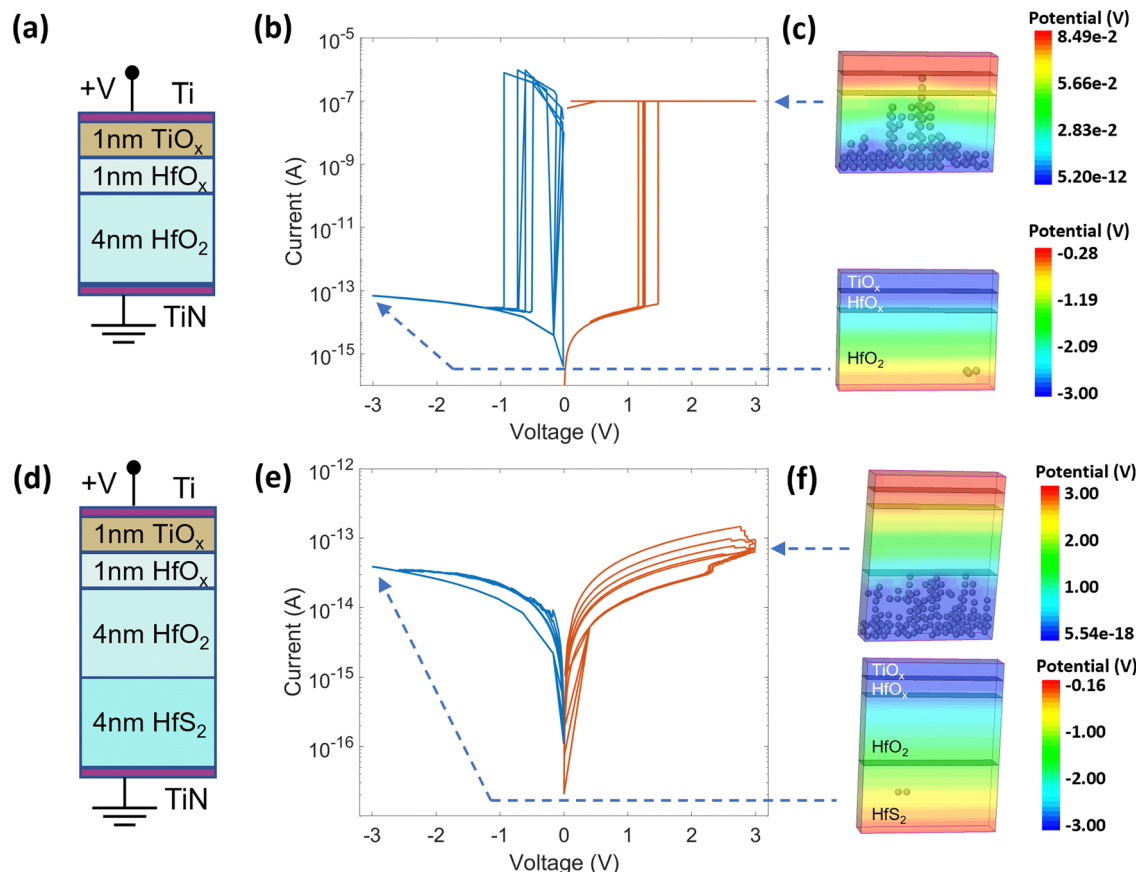
To further understand the transport and role of the semiconductor layer in our devices, we simulated resistive switching using a technology computer aided design (TCAD) software: Sentaurus (Synopsys, 2022). We compare a vertical memristor structure with a switching layer consisting of only  $\text{HfO}_x/\text{HfO}_2$  to one consisting of  $\text{HfO}_x/\text{HfO}_2/\text{HfS}_2$ , similar to our devices.

The dynamics of three particles were simulated in our modelled devices under applied field in kinetic Monte-Carlo (KMC) simulations: mobile oxygen ions ( $\text{O}^{2-}$ ), mobile oxygen vacancies ( $\text{V}_{\text{O}}^{2+}$ ) and immobile, uncharged oxygen vacancies ( $\text{V}_{\text{O}}$ , composing the filament). Allowing for field-driven Frenkel pair ( $\text{O}^{2-}$  ion and  $\text{V}_{\text{O}}^{2+}$  oxygen vacancy) generation and recombination, we simulated resistive switching by ramping voltage in a quasistatic manner, dwelling at each voltage step for a certain period of time, recording the defect generation, particle movement in the device and the resulting conduction or leakage current (solving Poisson's equation) from the top to the bottom electrode. Spatially-dependent as opposed to spatially-agnostic vacancy generation was simulated by reducing the activation energy for Frenkel pair generation in the presence of pre-existing defects, guided by existing literature.<sup>59,60</sup> Subsequently, filaments were generated as an energy-driven and spatially-dependent transition from free-moving, charged  $\text{V}_{\text{O}}^{2+}$  particles into immobile, uncharged  $\text{V}_{\text{O}}$  particles which can carry a conduction current. Trap-assisted tunnelling processes which would make the simulation more realistic<sup>60</sup> were omitted due to their heavy simulation time cost.

We simulated device structures as shown in Fig. 5a, using a design similar to that of existing  $\text{HfO}_x/\text{HfO}_2$  memristors but with a lateral size of  $8 \text{ nm} \times 1.5 \text{ nm}$  to focus on the dynamics of a single filament and reduce simulation time. A Ti top electrode was modelled as an idealised contact of no thickness, on top of a 1 nm thick  $\text{TiO}_x$  layer interfacing with an equally thin  $\text{HfO}_x$  layer. The latter two regions were included due to the well-known gettering effect of Ti electrodes on oxides.<sup>58,61</sup> The  $\text{TiO}_x$  region therefore permitted in-and-out diffusion of  $\text{O}^{2-}$  ions into the electrode under an applied field to simulate this effect. Frenkel pair generation in  $\text{HfO}_2$  based devices with Ti top electrodes has been shown to occur preferentially in the sub-stoichiometric  $\text{HfO}_x$  region,<sup>62</sup> so we simulate Frenkel pair generation only in the  $\text{HfO}_x$  region, with the  $\text{HfO}_2$  bulk allowing  $\text{V}_{\text{O}}^{2+}$  diffusion and filament growth/recession under applied field. The bottom contact was a TiN idealised contact.

In Fig. 5b we show representative resistive switching cycles for a  $\text{Ti}/\text{TiO}_x/\text{HfO}_x/\text{HfO}_2/\text{TiN}$  device. The device was cycled 5 times to demonstrate the general switching characteristics while saving simulation time. The device exhibits abrupt





**Fig. 5** Finite-element simulation of HfO<sub>2</sub> memristors without and with HfS<sub>2</sub> (a) Thicknesses of each layer in the HfO<sub>x</sub>/HfO<sub>2</sub> memristors without HfS<sub>2</sub> (width = 1.5 nm, length = 8 nm). (b) Simulated IV sweeps of a device excluding HfS<sub>2</sub> exhibiting abrupt switching with filament formation and dissolution shown in (c) for peak SET and RESET voltages, respectively. Electrostatic potential across the device also shows modulation of potential due to the presence of the filament in the device. Spheres in the electrostatic potential plots represent immobile vacancies (V<sub>O</sub>) comprising the filaments. (d) Structure of simulated devices including the HfS<sub>2</sub> region. (e) Simulated IV sweeps of a device using the semiconductor–oxide structure from (d) showing gradual resistive switching, with immobile vacancy concentration (represented by spheres) shown in the HfS<sub>2</sub> region in (f) for the peak SET and RESET voltages. A much smaller modulation of the potential due to vacancy aggregation in (f) can be seen compared to the electrode bridging filament in (c).

resistive switching and requires a current compliance to prevent complete dielectric breakdown, as is common in most HfO<sub>x</sub>-based memristive devices. The particles shown in Fig. 5c are immobile vacancies (V<sub>O</sub>) comprising the conductive filament, and the voltage was applied to the top electrode. Note that for both Fig. 5c and f, oxygen ions and mobile vacancies are not visualised for ease of interpretation.

With the inclusion of a HfS<sub>2</sub> region (Fig. 5d), we observe compliance free, gradual resistive switching (Fig. 5e) with tuneable device conductance (Fig. S6, ESI†) as in our experimental devices. The HfS<sub>2</sub> region was simulated by starting with a template Si file and adjusting the band gap (1.23 eV) and work function (5.71 eV) parameters due to limited available material parameters for few-layer HfS<sub>2</sub>.<sup>63–66</sup> Enabling charged vacancy diffusion and filament growth/recession mechanisms in the HfS<sub>2</sub> region was critical for the replication of resistive switching similar to our experimental devices (Fig. S4, ESI†). A similar effect where charged oxygen vacancies migrated through HfO<sub>2</sub> and across the HfO<sub>2</sub>/SiO<sub>2</sub> interface has been investigated.<sup>67</sup> The vacancy was shown to stabilise in its neutral charge state upon entering the SiO<sub>2</sub> layer, just as we have modelled for the HfO<sub>2</sub>/

HfS<sub>2</sub> interface here. In our experimental devices, it is likely that vacancies may have migrated through out-of-plane defects present in the pristine device (Fig. S2, ESI†) which could explain the forming-free behaviour.

Notably, simply increasing the thickness of the HfO<sub>2</sub> layer as shown in Fig. 5a to match the HfO<sub>2</sub>/HfS<sub>2</sub> thickness shown in Fig. 5d did not lead to any significant hysteretic behaviour in the sub-switching regime and the device still showed abrupt resistive switching otherwise. Therefore, the HfS<sub>2</sub> layer could play a vital role in limiting currents and preventing abrupt resistive switching, removing the need for current compliance. Greatly reduced peak current magnitudes can be observed in the simulated HfO<sub>2</sub>/HfS<sub>2</sub> device compared to our fabricated devices, however this has been shown to be due to the small cross-sectional simulation area chosen (Fig. S5, ESI†). By extrapolating to the lateral area of our experimental devices, we predict similar currents in the order of nA at 1.0 V. Furthermore, we observe that the peak conductance of the device decreases with increasing HfS<sub>2</sub> thickness (Fig. S6, ESI†), demonstrating the ability to tune the peak conductance and energy consumption of these devices based on their structure. The current observed is



strongly related to the number of  $V_O$  generated in the  $HfS_2$  region in the simulation (Fig. 5f). This suggests a conductance-mediated switching mechanism as the behaviour exhibited by the device is more akin to resistance switching without complete filament formation<sup>14,54,57</sup> rather than the more abrupt and conventional filamentary bridging of the top and bottom electrodes through an amorphous hafnia switching layer. Video files showcasing the generation and diffusion of vacancies contributing to resistive switching in these devices can be accessed in the ESI† (Movies S1 and S2) with a brief description of each movie in ESI† Section S5. The simulation accuracy and current magnitudes can be improved further by the inclusion of trap-assisted tunnelling processes such as elastic and inelastic trap to band and band to trap tunnelling of electrons, treating the  $V_O^{2+}$  particles as electron traps which transition to  $V_O$  particles upon electron capture.<sup>60</sup>

## Conclusions

We have shown that oxide–semiconductor structures obtained by dry oxidation of  $HfS_2$  at low temperature ( $<300\text{ }^\circ\text{C}$ ) can be used to realize forming-free and compliance-free resistive memories. By using voltage pulses, we demonstrate that non-volatile resistive switching with a  $R_{ON}/R_{OFF} \approx 10^2$  can be achieved with low energy, 80 ns pulses. We also show that the devices can exhibit resistive switching with less than 20 pJ pulses, highlighting their potential for low energy operation which is critical for ML and neuromorphic applications. Stable retention of resistance states at  $150\text{ }^\circ\text{C}$  has been observed, demonstrating the potential of these devices for long retention times and resilience to ageing. With the aid of IV sweeps and TCAD simulations, we investigate the transport in these devices and show that the semiconductor layer plays a key role in preventing oxide breakdown, enabling compliance-free operation and tuneable conductance/power consumption. Further work is required to determine and decouple the exact switching and transport mechanisms in the device, for example by investigating the effect of area on LRS conductance in experimental devices. However, our work has shown that both the semiconductor–oxide structure and the precise control of oxide crystallinity have a significant impact on the performance and behaviour exhibited by 2DLM-based memristors, paving the way for simplified circuits for neuromorphic computing.

## Methods

### $HfS_2$ production and oxidation

$HfS_2$  flakes were prepared by mechanical exfoliation of a  $HfS_2$  crystal (HQGraphene) onto 285 nm  $SiO_2$  on Si in an inert ( $N_2$ ) glovebox environment. The flakes were then examined using an optical microscope and transfer system within the glovebox. Oxidation was then performed in a Moorfield Minilab 026 system integrated within the same inert environment glovebox. The flakes were heated in vacuum to a set point of  $280\text{ }^\circ\text{C}$  when oxidation commenced for 110 minutes at 0.1 mbar in a dry  $O_2$

environment with a flow rate of 38 SCCM. The samples were then allowed to cool in vacuum.

### Ellipsometry measurements

Ellipsometry measurements are performed using an EP4 Spectroscopic Imaging Ellipsometer (SIE, Park Systems GmbH, Göttingen), equipped with a laser-stabilized Xenon arc lamp and a three-grating monochromator as a spectroscopic light source. This allows for an available spectral range between 360 nm to 1000 nm, and a  $\sim 5$  nm bandwidth of the output line. A polarization state generator (PSG), comprised of a linear polarizer and a quarter-wave plate (compensator), controls the state of polarization of the incident beam. The reflected light is collected through an analyzer and a  $50\times$  objective to a  $1392 \times 1040$  pixel CCD camera, allowing for a lateral resolution down to  $1\text{ }\mu\text{m}$ . All measurements are performed in the P-A-nulling mode, at an incidence angle of  $50^\circ$  with respect to the surface normal.

### TEM lamellar fabrication and characterisation

The cross-sectional lamellae were prepared using a DualBeam FIB-SEM system (Carl Zeiss Auriga), equipped with a platinum (Pt) deposition cartridge and a nanomanipulator (Kleindiek Nanotechnik). To minimize the ion beam damage, the sample was first protected by a  $\sim 100$  nm platinum layer by electron beam deposition (2 kV). After that, several micrometer-thick platinum layers were deposited using a gallium ion beam. After rough milling by 30 kV ion beam, a  $\sim 2\text{ }\mu\text{m}$  thick plate was lifted out and attached to the edge of a copper finger, following thinning processes using a 15 kV ion beam to minimize the ion beam damage and the final lamella was less than 100 nm thick. After thinning, the lamella was transferred to the TEM column for observation as soon as possible to minimise potential further oxidation. Transmission electron microscopy (TEM) and scanning TEM (STEM) were performed using uncorrected FEI Titan 80–300 with a Schottky field emission S-FEG source operated at 300 kV. Electron energy-loss spectroscopy (EELS) maps were carried out with a Gatan Quantum spectrometer with an energy dispersion of 0.5 eV per channel.

### Device fabrication

Bottom electrodes were fabricated by a direct-write lithography method, evaporating 5 nm of chrome as an adhesion layer, and then 65 nm of gold by electron beam evaporation. Lift-off was performed in Dimethyl sulfoxide (DMSO) at  $65\text{ }^\circ\text{C}$  for 10 minutes. Flakes of  $HfS_2$  used in devices were transferred by a polycarbonate (PC) stamp, which was melted onto the bottom electrodes at  $180\text{ }^\circ\text{C}$ . The residual PC was dissolved in chloroform and the device was cleaned with acetone and IPA cleaning. Subsequently, the flakes were partially oxidized following the protocol described above. Finally, direct-write lithography was used to pattern the top electrode and 5 nm of titanium then 65 nm of gold was deposited by electron beam (e-beam) evaporation, with the lift-off performed the same as before.

### Device characterisation

Devices were measured on a FormFactor (formerly Cascade) MPS150 probe station, connected to a Keysight B1500A



Parameter Analyzer with remote sensing units and a waveform generator/fast measurement unit (WGFMU) with a temporal resolution of 10 ns. Oscilloscope measurements were performed with a 1 GHz Keysight P9243A oscilloscope. Measurements above room temperature and in vacuum were conducted with a 6-probe Nextron MPS-PTH chamber equipped with a Peltier stage and connected to a dry pump.

### Sentaurus TCAD simulations

Simulations were performed in Synopsys Sentaurus TCAD. Device structures were designed in SDE, with a mesh size of 0.5 nm and no doping. A template Silicon parameter file was used to represent HfS<sub>2</sub> in the device structure. Ti and TiN electrodes were simulated as idealised contacts. In SDevice, Kinetic Monte Carlo (KMC) simulations were used to show the time evolution of oxygen vacancies and oxygen ion generation, diffusion, and filament growth/recession dynamics dependent on applied voltage to the simulated structures. SVisual TCL command files were used to produce particle plots, IV characteristics and animations included in ESI†.

### Data availability

Data for this article, including scripts used to plot figures in the main text and ESI† are available in the UCL research data repository, at <https://doi.org/10.5522/04/27186993.v1>.

### Conflicts of interest

The authors declare that they have no competing interests.

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