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Ultrahigh stress response and storage properties in a single CdS nanobelt-based flexible device for an erasable nonvolatile stress sensing and memory effect

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Here, we demonstrate that a single CdS nanobelt with numerous stacking faults, synthesized by a thermal evaporation method, can show a giant stress-response to compressive and tensile strains with an ultrahigh gauge factor of $\sim 10^4$ and ultrafast millisecond response and recovery speed. After the strains were removed, more importantly, the stress can trigger a high resistance state (HRS), indicative of a nonvolatile stress sensing and memory effect. Moreover, the stress-induced HRS can return to the initial low resistance state (LRS) after a relatively large bias was subsequently applied, indicative of a bias-erasing effect. In nanostructures, numerous stacking faults, serving as trap centres, can capture and store charges. Therefore, the bulk structural defects play a crucial role in superior stress sensing accompanied by an erasable nonvolatile memory effect. Compressive strain can trigger the height of the trap barrier to decrease, whereas tensile strain can trigger it to increase. Therefore, the conductance of the CdS nanobelt regularly increases with an increase in compressive strain. In contrast, it decreases with an increase in tensile strain, showing the strain dependence of conductance. After compressive or tensile strains were removed, in addition, the total number of electrons localized in traps is also reduced, and correspondingly the conductance decreases, showing a nonvolatile stress-writing HRS memory effect. Subsequently, the charges can be injected into traps at a relatively large bias, resulting in the recovery of the LRS, namely an erasable effect. Regarding superior stress-switching accompanied by stress-writing and bias-erasing memory, a multi-defect CdS nanostructure has tremendous potential in nonvolatile stress sensing and memory applications.

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1. Introduction

Flexible conductive stress–strain materials can produce large deformation under stress and meanwhile maintain a certain degree of electrical conductivity. Therefore, they can be widely applied in sensors, foldable display screens, wearable electronic devices, electronic skin, and artificial organs.[1–6] In particular, nanostructured materials show superior mechanical properties, and therefore they can be integrated into flexible devices that can be subjected to large strain.[7] Moreover, a giant piezoresistance (GPZR) effect, which is more than two orders of magnitude greater than the known bulk effect, can be produced in nanostructures.[8] Accordingly, they have gained considerable attention in stress sensors based on semiconductor nanostructures due to an ultrahigh response to stress.[9–32] So far, some mechanisms, such as the variation of carrier mobility, effective carrier mass, electron concentration change trap activation energy and trap barrier depth,[8,22–27] the transition from an insulator to a metal,[28] the shift of the surface Fermi-level,[27,28] and the relaxation of non-stress-related surface charges,[29,30] have been proposed to explain the phenomena. Whereas, at the nanoscale, their physicochemical processes are still controversial. For one-dimensional (1D) nanostructures, interestingly, it is extremely advantageous to construct two-terminal devices, and moreover the origin of their physical mechanism can be well identified due to configuration simplicity.[31,32] Consequently, individual 1D nanostructures have attracted extensive attention in the construction of nanodevices as building blocks.

CdS is a group II–VI semiconductor with a direct bandgap energy of 2.42 eV. Due to a proper bandgap width in the visible light range and excellent physicochemical properties,[33–35]

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currently, considerable attention has been focussed on CdS in optics, such as photocatalysis,[36] solar cells,[37,38] and photodetectors.[39–41] Although it has been applied in electronics as well, such as field-effect transistors,[42] switches,[43] and logic circuits,[44] it is still urgently required to improve and expand its application in electronics. For CdS, in general, it exists in two lattice structures of face-centered cubic (fcc) zinc blende and hexagonal closed-packing (hcp) wurtzite. In particular, it is easy for staking faults to generate reciprocally in the two lattices, resulting in the formation of twin planes and heterostructures,[45–47] which significantly affect the electronic transport properties of nanostructures and lead to the formation electronic mini-bands, and therefore will be beneficial not only for bandgap engineering but also for direct intersubband and optical transitions.[48,49] When the external environment varies, these superstructures will strongly impact the electronic transport. Therefore they can show superior sensing capability, and even form a special memory function.[40] For n-type nanostructures, dangling bonds, arising from the breakage of lattice periodicity on their surfaces, can trigger acceptor-type surface states, resulting in upward band bending and the formation of a carrier-depletion layer in the vicinity of surfaces, and correspondingly a surface barrier-related diode, which is independent of metal work function and semiconductor electron affinity, is constructed.[50–52] More importantly, numerous bulk defects, such as atom interstitial and vacancy composition defects, and stacking fault structure defects, exist within the nanostructures, resulting in the formation of traps at different levels.[31,32,53] The filling and emptying of traps can not only form a volatile sensing function, but also produce more meaningful nonvolatile memory characteristics. To meet the ever-increasing demand in device function, it is imperative to explore and extend the novel properties of nanostructures, and then design a new electronic component. Especially for nanostructure-based flexible devices with superior mechanical performance, if their conductance can show a giant response to external stress, and moreover the variation can effectively be memorized, this will further extend their applications in nonvolatile stress-sensor and memory devices.

Here, a single CdS nanobelt with numerous stacking faults was utilized to fabricate a two-terminal flexible device on a Kapton substrate. These bulk defect-related traps can capture and store charges. By loading different strains, it is expected that the height of the trap barrier could be modulated, which in turn adjusts the conductance of the CdS nanobelt, resulting in a superior stress sensing effect. Meanwhile, a high resistance state (HRS) is expected to form by the mechanical excitation of trapped charges induced by strain as well, and moreover the strain-induced HRS can be well maintained at a low operation bias and room temperature after being mechanically excited, forming a stress-writing nonvolatile memory effect. Subsequently, the HRS device can return to the low resistance state (LRS) by loading a relatively large bias, and correspondingly a bias-erasing effect is realized. Thus, not only will superior stress switching be constructed on the basis of the CdS nanobelt, but also a stress-writing and bias-erasing nonvolatile stress sensor and memory effect will successfully be realized.

2. Experimental

2.1. Synthesis of CdS nanobelts

CdS nanobelts, used in this experiment, were synthesized by a high temperature thermal evaporation method.[40] First, high purity CdS powders were put into a small clean ceramic boat. Subsequently, the ceramic boat is placed in the middle of a tubular furnace. In order to fully exhaust the air in the ceramic tube, 90%N_2 + 10%H_2 mixture gas was introduced for 30 min before heating, and thereafter the tube furnace was heated to 1200 °C and held for 1 h. After reaction, the tubular furnace was naturally cooled to room temperature under the protection of a mixed atmosphere. Finally, the yellow products, namely CdS nanobelts, were found on the inner wall of the ceramic tube.

2.2. Characterization

In order to analyse the composition, morphology and structure, the as-synthesized samples were measured by X-ray diffraction (XRD; RIGAKU D/max-3b), field emission environmental scanning electron microscopy (FESEM, FEI Quanta 200F), and high-resolution transmission electron microscopy (HRTEM, JEOL JEM-2010).

2.3. Fabrication and electrical measurement of the device

For the preparation of a flexible device, a relatively long individual CdS nanobelt was transferred onto a Kapton substrate using an optical microscope and then Ag electrodes were fabricated at the two ends using semi-dried silver paste. And then, post-annealing was required to minimize the contact resistance under a 90%N_2 + 10%H_2 atmosphere at 400 °C for 10 min. Finally, the devices were packed using polydimethylsiloxane (PDMS). Different strains were realized using a linear motor. The electrical measurements were conducted using a synthesized function generator (Stanford Research System Model DS345) and a low-noise current pre-amplifier (Stanford Research System Model SR570).

3. Results and discussion

3.1. Morphology and structural characterization of the as-synthesized CdS nanobelt

To better understand the possible origin of stress impact on the conductance of the CdS nanobelts, the morphology and structure of the as-synthesized samples were investigated in detail. Fig. 1a shows the XRD pattern. All the diffraction peaks can be indexed to hexagonal wurtzite CdS. In the detectable range of resolution, no other impurity peaks were found in the XRD pattern, indicating that the CdS nanobelts prepared by a thermal evaporation method have high purity. To further distinguish the morphology of the CdS samples, they were characterized by FESEM, as shown in Fig. 1c and d. It can be seen that the samples represent mainly a belt-like zigzag shape with widths ranging from tens to hundreds of nanometers and lengths ranging from tens to hundreds of microns, and moreover their surface is smooth and tidy. Their microstructure was characterised by HRTEM. As seen from the lattice fringe image and its corresponding fast Fourier transform (FFT) pattern, as shown in Fig. 1e and f, the growth of the CdS nanobelt is along the [0001] direction, and moreover numerous stacking faults

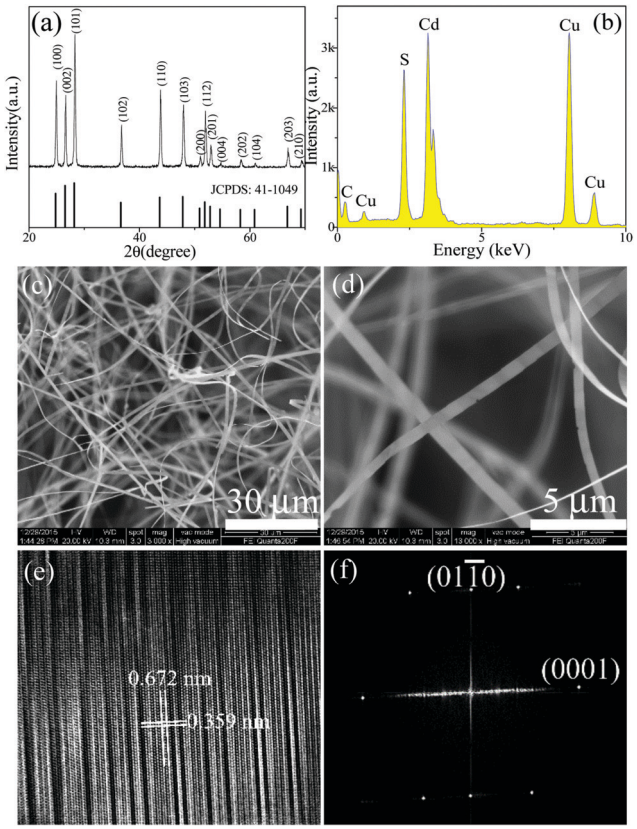

Fig. 1 Structural and morphology characterization of as-synthesized CdS products. (a) XRD pattern, revealing the formation of hexagonal wurtzite CdS (JCPDS: 41-1049); (b) EDS spectrum, indicating that the sample is composed of Cd and S; (c) and (d) FESEM images, showing belt-like zigzag shape; (e) and (f) HRTEM image and its corresponding FFT pattern, revealing the presence of numerous stacking faults in (0001) planes.

exist in the {0001} planes. Their composition was further analysed using an X-ray energy dispersive spectrometer (EDS), as shown in Fig. 1b. The appearance of Cu and C elements originates from the copper grid and the carbon-coated polymer supporting film, respectively. Hence, the nanobelts are only composed of Cd and S.

3.2. Strain dependence of electronic transport in a single CdS nanobelt-based device

Firstly, the stress sensing properties of a single CdS nanobelt under static compressive stress were tested at 1 V triangle wave voltage with a scanning frequency of 0.1 Hz, and 0%, −0.13%, −0.26%, −0.39% and −0.52% strains were loaded, respectively. The corresponding schematic diagram of fabrication and measurement of the device is shown in Fig. 2a. As seen from the *I*–*V* characteristics in Fig. 2b, the conductance of the device increases with an increase in compressive strain. Fig. 2c shows the series multiple cyclic current response plot under different strains. Similarly, it can demonstrate that the conductance increases with an increase in compressive strain. Especially for a compressive strain higher than −0.39%, the sensitivity of the device to compressive strain is more apparent. The current value has increased by approximately two orders of magnitude compared without loading compressive stress, and moreover the current

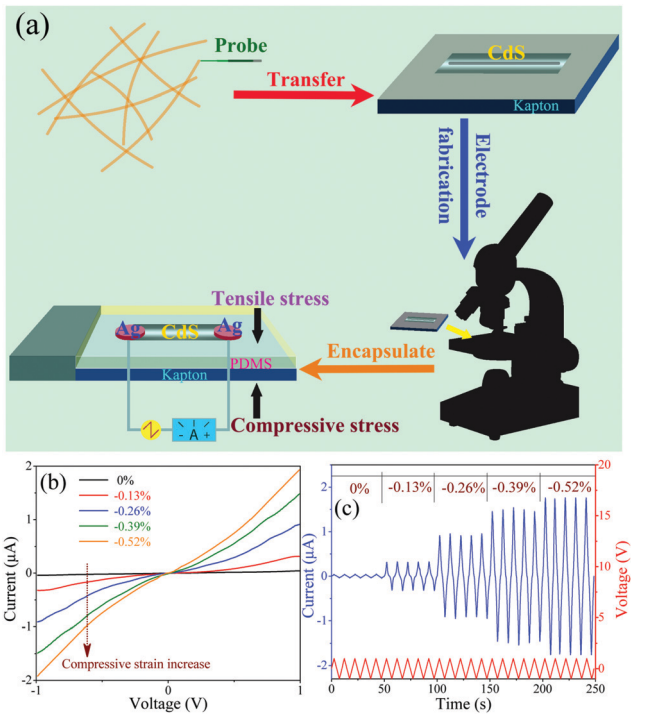

Fig. 2 Under different static compressive strains, the conductance response of a single CdS nanobelt-based device at 1 V bias. (a) Schematic diagram of the device fabrication for the measurement of a strain sensor and memory; (b) *I*–*V* curves; (c) multiple cyclic *I*–*T* response curves, showing a stable variable feature.

variation is up to microampere, indicating that the conductance of CdS nanowires imcreases significantly under static compressive strain, namely an advantageous stress switching performance.

Under different static tensile strains, subsequently, the stress response characteristics of the single CdS nanobelt were also examined under the same conditions, as shown in Fig. 3. It can be seen that the conductance of the device decreases with increasing tensile strain. This is just contrary to the applied static compressive strain. As seen from Fig. 3b, the current of the device decreases rapidly with an increase in tensile strain. When the strain of the device reaches about +0.52%, its current is almost zero, and the device is close to a nonconductive state. It can be seen that the CdS nanobelt is also overwhelmingly sensitive to static tensile strain. Therefore, the superior

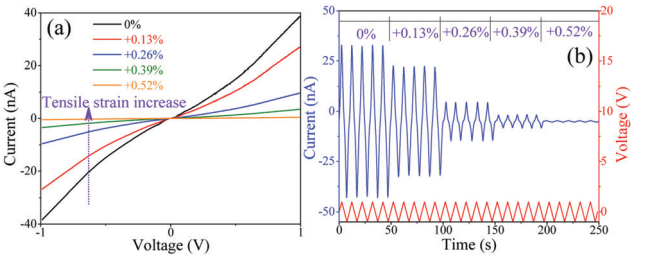

Fig. 3 Under different static tensile strains, the conductance response of a single CdS nanobelt-based device at 1 V bias. (a) *I*–*V* curves; (b) multiple cyclic *I*–*T* response curves.

piezoresistive switching effect can be used as a promising strategy in stress sensors.

For the *I–V* characteristics under different strains, it can be found that they are all non-linear, indicating that it is impossible for their electronic transport to originate from Ohmic contact. To explore the feasible mechanism, their *I–V* curves are respectively fitted with different electronic transport models, such as Schottky emission $\ln(I) \propto V^{1/2}$, space charge limited current (SCLC) $I \propto V^2$, Poole–Frenkel (P–F) emission $\ln(I/V) \propto V^{1/2}$, and Fowler Nordeim (F–N) tunnelling $\ln(I/V^2) \propto 1/V$.[54–59] After fitting, it can be found that $\ln(I/V) \propto V^{1/2}$ has a relatively outstanding linear relationship compared to $I \propto V^2$ for the 0 ± 1 V positive bias part under different strains, as shown in Fig. 4. This result manifests that the electronic transport of the CdS nanobelt mainly arises from the Poole–Frenkel emission mechanism under strain, that is, the piezoresponse mainly originates from the hopping of electrons localized in the bulk traps of CdS nanostructures rather than the interface barrier between the nanobelt and two Ag electrodes. According to the principle of the P–F emission mechanism, the current through the CdS nanobelt can be expressed as follows:[59]

$$J = qN_C\mu E \exp\left[\frac{-q\left(\phi - \sqrt{qE/\pi\varepsilon_0\varepsilon_r}\right)}{kT}\right] \quad (1)$$

where J is the current density, q is the charge electric quantity, N_C is the conduction band state density, μ is the electron mobility, E is the electric field strength, ε_0 is the dielectric constant in free space, ε_r is the dynamic dielectric constant, K is the Boltzmann constant, T is the absolute temperature, and ϕ is the barrier height the trapped electrons need to pass out, that is, the trap ionization energy or capture energy level, which is related to Coulomb potential. As seen in Fig. 4, in addition, the slope of the fitted curves has basically the same value of about 2.5 under different compressive and tensile strains, indicating that it is almost independent of the applied strains. The electrical measurements were all performed at room temperature, and therefore the mobility remains unchanged, which in turn makes the dynamic dielectric constant ε_r invariant as well. Although the slope of the device can almost maintain the same value under different strains, the fitted curves upshift with increasing compressive strain, and contrarily downshift with increasing tensile strain. This result firmly demonstrates that strain only triggers the variation of barrier height ϕ, which decreases with compressive strain and conversely increases with tensile strain. As a consequence, it is easier for the electrons to hop from traps into the conduction band under larger compressive strain; in contrast, it becomes more arduous under larger tensile strain.

3.3. Stress-response to dynamic cyclic strains

I–V characteristics, measured under different static strains, show that CdS nanobelts have excellent stress response properties. The piezoresistive effect was further measured under different dynamic cyclic compressive and tensile strains at a fixed bias of 1 V, respectively, as shown in Fig. 5 and 6. At 1 V fixed DC voltage, the strains were periodically loaded at an interval of 20 s. It can clearly be seen that the current increases under loading compressive strain and then decreases after the removal of compressive strain. In contrast, it decreases under being loaded with tensile strain and increases after the tensile strain is removed. The current switching ratio of LRS/HRS increases with an increase in both compressive and tensile strains. The gauge factor (GF) can be calculated according to the following formula:

$$\mathrm{GF} = \frac{\Delta R/R}{\varepsilon} \quad (2)$$

where ΔR is the resistance difference between the HRS and LRS, R is the resistance of LRS, and ε is the strain. Under compressive

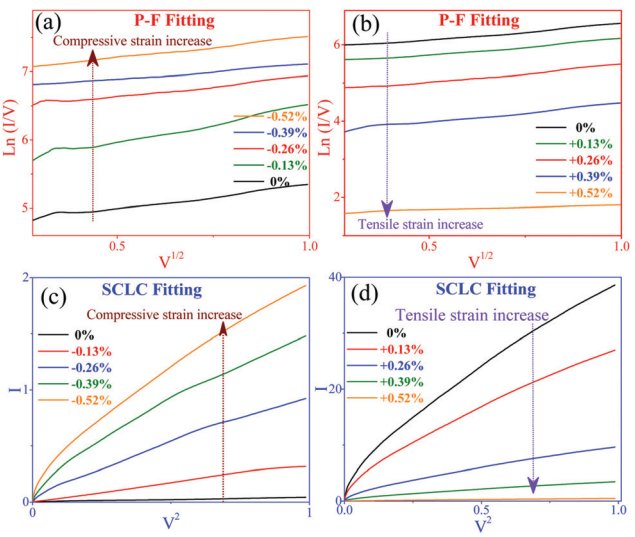

Fig. 4 Under different static strains, the fitted plots of *I–V* curves at a forward bias part. (a) and (b) $V^{1/2}$–ln(*I*/*V*) P–F fitting under compressive and tensile strains, respectively; (c) and (d) V^2–*I* SCLC fitting under compressive and tensile strains, respectively.

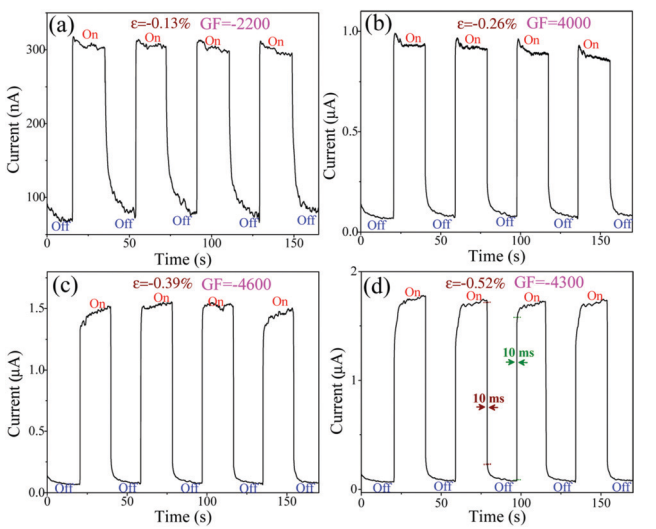

Fig. 5 Under different dynamic cyclic compressive strains, the on/off response of a single CdS nanobelt-based device at a fixed bias of 1 V. (a) −0.13%; (b) −0.26%; (c) −0.39%; (d) −0.52%.

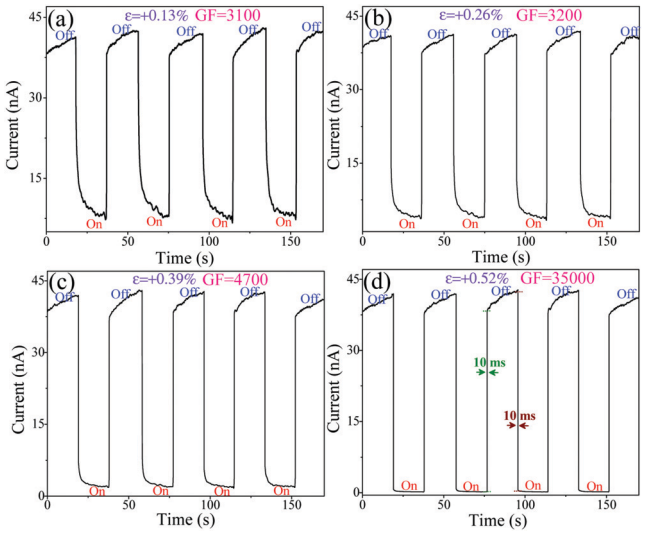

Fig. 6 Under different dynamic cyclic tensile strains, the on/off response of a single CdS nanobelt-based device at a fixed bias of 1 V. (a) +0.13%; (b) +0.26%; (c) +0.39%; (d) +0.52%.

and tensile strains lower than 0.13%, both their GFs are relatively low, and moreover the device shows a relatively slow recovery from the LRS to HRS. Under a low strain, therefore, the current shows a persistent variation with time; however it can easily reach a relatively stable state under a larger strain. Under the tensile and compressive strains of ±0.52%, the response and decay time is all lower than about 10 ms, indicative of a quick response to stress and bias. With increasing strains, moreover, GF can reach about 4.0×10^3. Under a higher tensile strain of 0.52%, GF shows a tremendous increase and exceeds 3.0×10^4 due to a larger resistance value at the HRS. This indicates that the conductance of a single CdS nanobelt has an ultrahigh sensitivity and responsivity to external stress. In addition, the periodic dynamic tests show that the current can maintain a relatively stable state, suggestive of outstanding repeatability.

In order to investigate the variations and characteristics of the strain dependence of the conductance response in a single CdS nanobelt in detail, dynamic cyclic compressive and tensile strains of ±0.39% were periodically loaded to the device at 1 V triangle wavelength voltage with a frequency of 0.05 Hz, as shown in Fig. 7 and 8, respectively. The loading and releasing time of strain is 8 and 2 s, respectively. As seen from Fig. 7, the current of the device increases with loading a compressive strain of −0.39%; that is, the conductivity increases and the resistance decreases, and contrarily the conductivity decreases and the resistance increases after the strain is released. Moreover, the response and recovery of current is very rapid upon loading and withdrawing strains. In addition, the GF value can reach about 1.7×10^4, indicative of an ultrahigh sensitivity and responsivity. As seen from Fig. 7a–c, the current variations are all nonlinear with the bias. It can further be seen that the *I*–*V* curve cannot reach its original state after completely removing the compressive strain, and moreover its conductance shows a certain degree of decrease, suggestive of a memory effect.

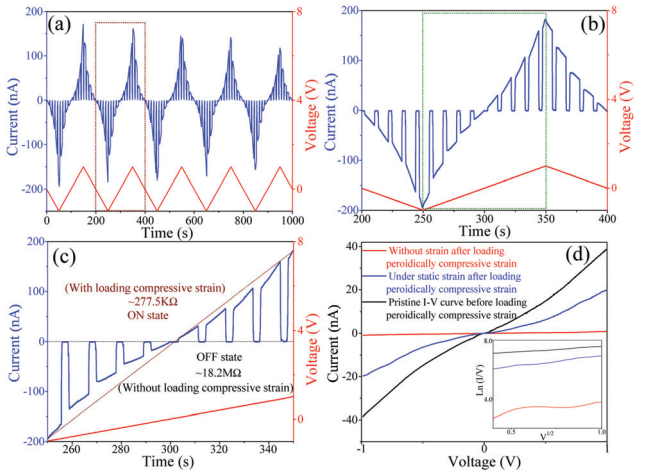

Fig. 7 Current response to a compressive strain of about −0.39% at 1 V bias. (a) At a consecutive triangle wave voltage (red curve) with an amplitude of 1.0 V and a frequency of 0.05 Hz, current (blue curve) response to a periodic dynamic compressive strain with 8 s loading and 2 s releasing; (b) one *I*–*V* response cycle to the periodic dynamic compressive strain corresponding to the wine dotted frame in (a); (c) the magnified view to the wine dotted frame in (b); (d) *I*–*V* curves before being loaded with a periodic strain (black), under being loaded with a static compressive strain (blue) and without being loaded with any strain (red) after a periodical compressive strain was applied, and the inset shows the fitting plot according to the PF emission mechanism for the forward-biased part.

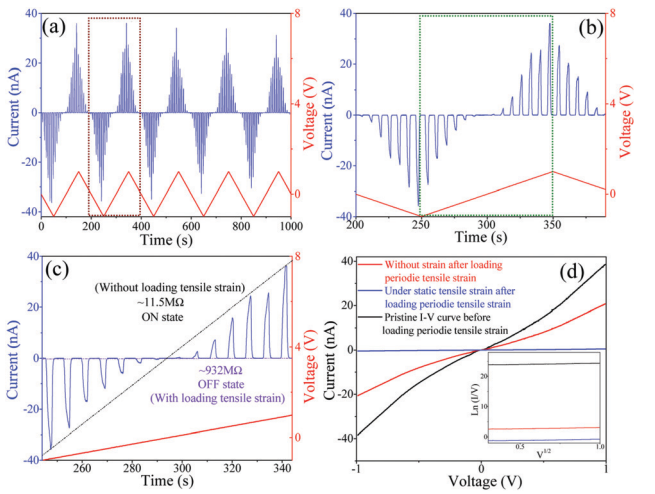

Fig. 8 Current response to a tensile strain of about +0.39% at 1 V bias. (a) At a consecutive triangle wave voltage (red curve) with an amplitude of 1.0 V and a frequency of 0.05 Hz, current (blue curve) response to a periodic dynamic tensile strain with 8 s loading and 2 s releasing; (b) one *I*–*V* response cycle to the periodic dynamic tensile strain corresponding to the wine dotted frame in (a); (c) the magnified view of the wine dotted frame in (b); (d) *I*–*V* curves before being loaded with a periodic strain (black), under being loaded with a static tensile strain (blue) and without being loaded with any strain (red) after a periodical tensile strain was applied, and the inset shows the corresponding plot according to PF emission fitting for the forward-biased part.

Under the same conditions, similarly, the piezoresistive performance of the device under a dynamic cyclic tensile strain of +0.39% was also measured at 1 V triangle wavelength bias,

as shown in Fig. 8. It can be seen that the device current decreases or it even shows a non-conductive state when tensile stress is loaded; that is, its conductivity decreases and correspondingly its resistance increases. In contrast, its current increases after the removal of strain, indicating that its resistance decreases. The response and recovery of the device is relatively rapid as well, and the GF value can reach about 2×10^4. Before loading dynamic strain, and under and without static tensile strain after dynamic tensile strain was applied, similarly, the *I–V* characteristics of the device were measured as well, as shown in Fig. 8d. After completely removing the tensile strain, the *I–V* curve cannot return to its initial state before loading tensile strain. Although the conductance of the device is lower under loading static tensile strain than that without static tensile stress, both of them are lower than that before loading dynamic tensile stress, indicative of the formation of a nonvolatile memory effect.

In the course of loading and removing strains, the single CdS nanobelt-based device can show a significant current variation of microamperes, an ultrahigh GF of $\sim 10^4$, and a fast response and recovery time of milliseconds. Moreover, the resistance variation law is consistent with loading static strain, showing an excellent stress dependence of switching performance. After external compressive and tensile strains were completely withdrawn, more importantly, the conductance of the device cannot be recovered completely to its initial LRS state before being loaded with strain, demonstrating a nonvolatile stress memory effect, which can be used to store the stress information and provide a theoretical basis for the development of the memory field. Accordingly, an individual CdS nanobelt not only shows surprising instantaneous stress sensing performance, but also has tremendous potential in nonvolatile stress sensing applications. Therefore, it has a great application prospect to be fabricated into an integrated device of volatile and nonvolatile stress sensors.

3.4. Nonvolatile stress sensing and memory properties

From the above analysis, an individual CdS nanobelt can not only show a rapid response to external stress variation, but also show a certain degree of memory effect after a strain is applied, indicating vast potential applications in nonvolatile stress-writing sensor and memory devices since they cannot return to the original LRS after the loaded compressive and tensile strains were completely removed. More interestingly, further experiments demonstrate that the strain-triggered HRS can return to its original LRS by applying a relatively large bias, and hence the stored stress information can effectively be erased. The compressive and tensile stress-writing and bias-erasing nonvolatile sensors and memory can be obtained. The corresponding writing and erasing properties are investigated in detail, as shown in Fig. 9 and 10.

As seen from Fig. 9, the memory cell can show an apparent compressive stress-triggered storage effect at 1 V operation voltage, and then the stored stress information can be erased by applying a relatively large voltage of 10 V. Although the current of the device increases under loading a compressive strain of −0.52%, it decreases to about 2 times after the compressive strain is

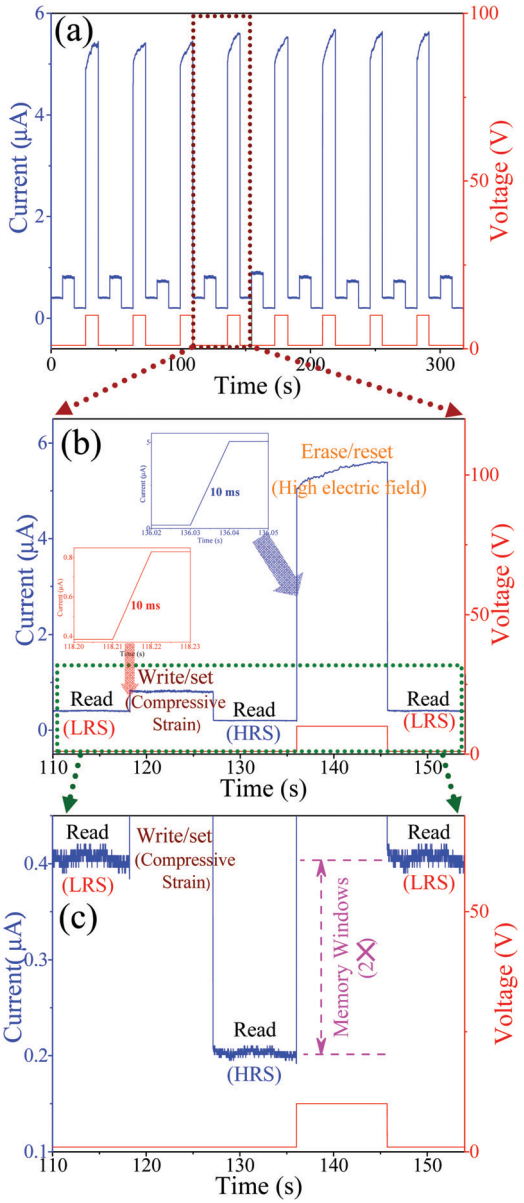

Fig. 9 Write/erase/read access of a single memory cell written by compressive strain and erased by a relatively large voltage of 10 V. Blue curves correspond to the current response, and red curves correspond to the as-loaded bias voltage. (a) Multiple cycles of write/read/erase; (b) an enlarged view of one cycle in the wine dotted frame in (a), showing that a strain of −0.52% can trigger an HRS and a large voltage of 10 V can induce the device to return to the LRS at a low read voltage of 1.0 V. The red and blue insets show the response time of the device upon being subjected to strain and a large bias, respectively, and the data sampling interval is 10 ms; (c) a magnified view of the green dotted frame in (b), showing the presence of an obvious memory window of 2× between the HRS and LRS.

completely removed compared with that of the initial LRS state, showing an HRS memory effect. Fig. 9a shows 8 consecutive writing/erasing/reading processes. It can be seen that the stability and reversibility are both extremely promising. Moreover, the response time is about 10 ms for both stress-writing and bias-erasing. In addition, the applied bias voltage and strain are independent of the polarity of the two-terminal device, indicating

that it is impossible for the erasable stress memory effect to originate from piezoelectricity.

Meanwhile, the stress memory performance of a single CdS nanobelt was also measured by tensile strain writing, as shown in Fig. 10. Under being subjected to a tensile strain of +0.52%, the current of the device decreases, which is just opposite to compressive strain. Although the current can show a certain extent of recovery after the tensile strain is completely removed, it cannot return to its initial LRS value, showing the same HRS memory effect as compressive strain. After applying a relatively large voltage of 10 V, the current of the device can completely return to its initial LRS, indicative of a similar erasable effect. The current variation exceeds 10 times before and after loading the tensile strain, suggestive of a relatively large memory window. Although the compressive and tensile strains can both give rise to the HRS memory effect, the tensile strain can trigger a larger memory window than the compressive strain at the same strain value. As seen from Fig. 10a, 8 consecutive writing/erasing/reading processes clearly show that the device can also exhibit a high degree of stability and repeatability for tensile stress-writing and large bias-erasing.

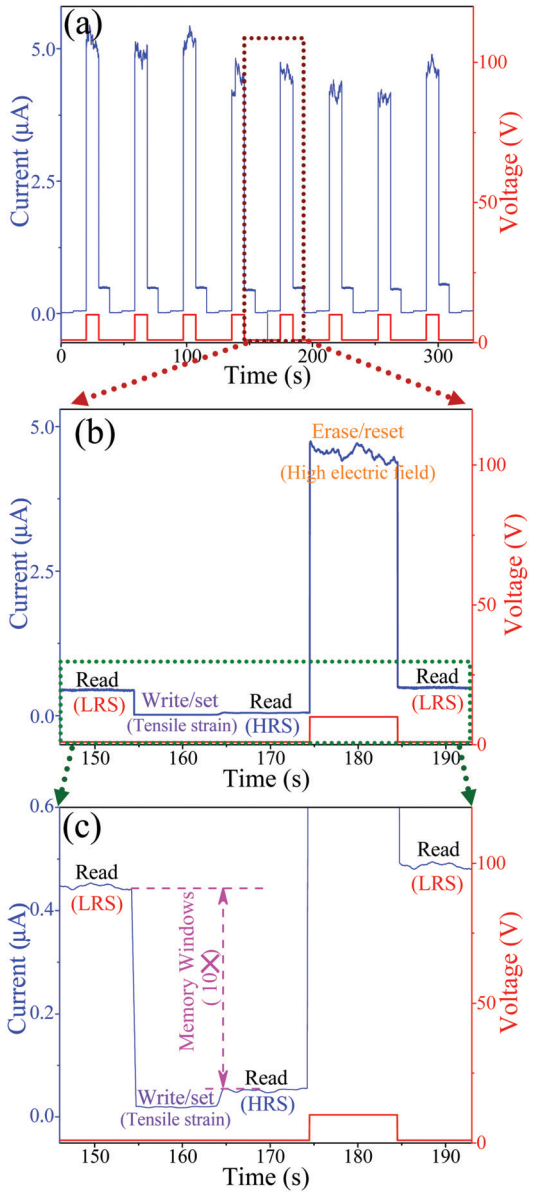

Fig. 10 Memory properties of a stress memory cell written by a tensile train of +0.52% and erased by a voltage of 10 V. Blue curves correspond to the current response, and red curves correspond to the as-loaded bias voltage. (a) Multiple cycles of write/read/erase/read, showing stability and repeatability; (b) enlarged view of one cycle in the wine dotted frame in (a), revealing that an HRS can be formed aftera tensile strain was applied and then LRS can be recovered after a large voltage of 10 V was applied at a low read voltage of 1.0 V; (c) a highly magnified view of the green dotted frame in (b), showing the presence of an excellent memory window of 10× between the HRS and LRS.

In addition, to further explore the stability and durability of the LRS and HRS in single CdS nanobelt-based stress memory, the variation of current with time was measured after applying strain and a large bias, respectively, as shown in Fig. 11. It can be seen that the current changes of the large bias-induced LRS and the compressive and tensile strain-induced HRS are both insignificant after 3000 seconds at 1 V reading voltage. This indicates that the stability and retention of nonvolatile properties are very good, and the stored HRS stress information and erased LRS data can both be maintained for a long time.

In order to further clarify the erasing mechanism of stored stress information in CdS nanobelts at a large bias, the HRS device triggered by a strain was continuously swept by 10 V triangular wave voltage, as shown in Fig. 12. It can be seen that the device can show a nonvolatile HRS at a low bias after a strain was applied. With the increase of external bias, nevertheless, the output current of the device jumps suddenly from the HRS to the LRS at about −6.5 V, accompanied by a large hysteresis loop. Therefore, the reset/erase process takes place at about 6.5 V voltage. Then, the device can remain in the LRS when the bias turns in the opposite direction. Moreover, it can invariably remain in the LRS under the subsequent second and third scanning cycle, which indicates that the HRS device can completely reach the LRS once it is applied with a large voltage above 6.5 V. After the stress information is written at zero or a relatively low bias voltage, consequently, it can effectively be deleted by loading a relatively large bias voltage higher than 6.5 V.

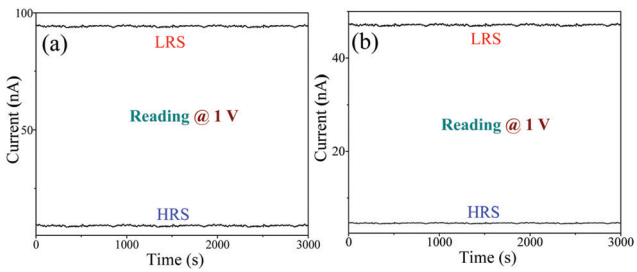

Fig. 11 Durability of stored data at both the bias-induced LRS and strain-induced HRS at 1 V reading voltage, revealing a nonvolatile memory behaviour. (a) The HRS written by loading −0.52% compressive strain and the LRS obtained by applying 10 V voltage; (b) the HRS written by loading 0.52% tensile strain and the LRS obtained by applying 10 V voltage.

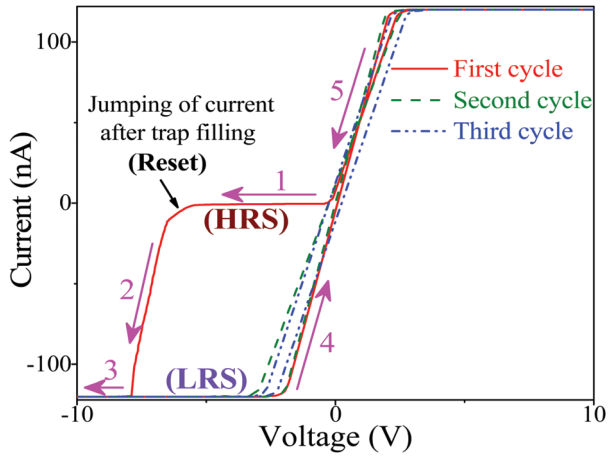

Fig. 12 Under applying a relatively large bias of 10 V, three consecutive cyclic *I–V* characteristics for a strain-induced HRS device, showing that the HRS device can become an LRS device after being first loaded with a bias above 6.5 V.

3.5. Trap-related stress-writing and bias-erasing mechanism

The work function of Ag is 4.26 eV, which is smaller than the CdS electron affinity of 4.5 eV, and hence an ohmic contact could form at the interface of two Ag electrodes and the CdS nanobelt. Due to the synthesis of CdS nanobelts at a relatively high temperature of 1200 °C, however, nonstoichiometric ratio can result in the presence of S vacancies and Cd interstitials in their lattices. Simultaneously, numerous stacking faults, verified by HRTEM observation, exist in their lattices as well. Moreover, these defect levels are relatively deep, and accordingly they can serve as trap centers for capturing and storing charges. For the nanostructures with a very large specific surface area and typical n-type properties, the breaking of lattice periodicity leads to the presence of a number of dangling bonds on their surfaces, and correspondingly a surface depletion region is formed and a surface barrier is built as well. Under different strains, however, all the *I–V* curves can well be fitted by a P–F emission mechanism. Therefore, the height of the trap barrier should surpass that of the surface barrier, and the electron transport of a single CdS nanobelt-based two-terminal device is mainly predominated by the barrier height of traps under strains rather than that of CdS NB and Ag electrode interfaces. Its conductance will strongly be dependent on the filling levels of traps.

CdS with a hexagonal wurtzite structure is a noncentrosymmetrical crystal. Although flexoelectric and piezoelectric effects could generate positive charges under tensile strain and conversely generate negative charges under compressive strain, they are dynamic effects. As seen from the *I–T* curves loading dynamic strains, their currents do not show two opposite variations at the moment of loading and withdrawing stress, and moreover the current variation states always remain as long as the strain is maintained. In addition, their *I–V* curves can well be fitted by the P–F mechanism under different strains, as shown in Fig. 4. Moreover, the height of the trap barrier decreases with an increase in static compressive strain, and contrarily it increases with an increase in static compressive strain. These results demonstrate that only the height of the trap barrier varies under strain. As seen from Fig. 7d, 8d, 9 and 10, in addition, the height of the trap barrier can both decrease after loading compressive and tensile strains. Therefore, both the compressive and tensile strains induce the filling levels to decrease by the excitation of mechanical energy, resulting in an HRS. The corresponding diagrammatic sketches of trap barrier height variation and trapped electron excitation are shown in Fig. 13b and c. At zero or a relatively low bias voltage, the electrical field-induced height (V) of the energy band tilt is lower than that of the trapped barrier (ϕ), and therefore the charges cannot effectively be injected into traps from the negative electrode. The emptied state of traps can well be maintained, showing a nonvolatile HRS memory effect. Under a larger bias, however, the electrical field-induced height of the energy band tilt is larger than that of the trapped barrier, and consequently it is exceedingly beneficial for charges to be injected into traps from the negative electrode. As shown in Fig. 12, there is a sudden increase of current, and then the device transforms from the HRS into the LRS after only being loaded with a relatively large unidirectional bias, which can verify firmly the presence of a filling effect. When the traps are filled up, electrons can readily hop from one trap to another, and accordingly the conductance increases and the device transforms from the HRS to the LRS. The corresponding diagrammatic sketch of trap filling is shown in Fig. 13d.

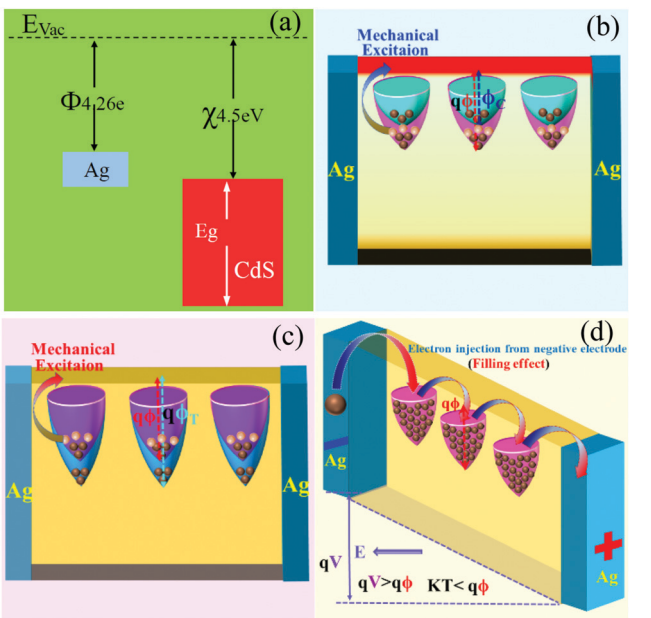

Fig. 13 Diagrammatic sketches of stress sensing and memory properties of a single CdS nanobelt-based two-terminal device. (a) Energy band diagram before contacting Ag with CdS; (b) under compressive strain, traps change, showing that the trap barrier height decreases and meanwhile some of the trapped electrons are excited mechanically; (c) under tensile strain, traps change, showing that the trap barrier height increases and meanwhile some of the trapped electrons are also excited mechanically; (d) under a relatively large electric field, the emptied traps are filled by electrons from the negative electrode, resulting in a recovery of the HRS to the LRS.

4. Conclusions

In summary, a flexible device, based on a single CdS nanobelt with numerous stacking faults, can show a giant conductance response to compressive and tensile strains with an excellent sensitivity, responsivity, and response and recovery speed. The conductivity increases with an increase in compressive strain, and conversely decreases with an increase in tensile strain. The GF value can reach about 10^4, and the response and decay time is low at about 10 ms. After compressive and tensile strains were applied, importantly, the device can both show a certain extent of resistance increase, and moreover the strain-induced HRS can well be maintained for a long time, exhibiting a nonvolatile stress-writing memory function. More interestingly, the HRS device can return to the initial LRS after subsequently applying a relatively large bias, showing a bias-erasing effect. The memory window can reach about 10 times triggered by a tensile strain of +0.52%. Therefore, the CdS nanobelts not only show an ultrahigh stress sensing performance, but also an excellent erasable nonvolatile stress sensing and memory performance. In nanostructures, the numerous stacking faults, served as trap centres, can capture and store charges. The height of the trap barrier surpasses that of the surface barrier, and accordingly the filling levels of traps play a dominant role in superior stress sensors accompanied by a certain extent of the erasable nonvolatile stress memory effect. Compressive strain can trigger the height of the trap barrier to decrease, and contrarily tensile strain can trigger it to increase. Therefore, the conductance of the CdS nanobelt is accurately controlled by loading different strains. After applying compressive and tensile strains, the total number of electrons in traps decreases due to mechanical excitation, resulting in a decrease in the conductance. Moreover, it can well be retained at a relatively low operation bias and room temperature, showing a nonvolatile stress-writing HRS memory effect. Subsequently, the charges can be injected into traps at a relatively large bias, resulting inthe recovery of the original LRS, namely an erasable memory effect. Regarding the superior stress-switching performance accompanied by nonvolatile stress-writing and bias-erasing memory, the multi-defect CdS nanostructure has tremendous potential in nonvolatile stress sensing and memory applications.

Conflicts of interest

There are no conflicts to declare.

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