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Strain-induced ordered Ge(Si) hut wires on patterned Si (001) substrates

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Ge/Si nanowires are predicted to be a promising platform for spin and even topological qubits. While for large-scale integration of these devices, nanowires with fully controlled positions and arrangements are a prerequisite. Here, we have reported ordered Ge hut wires by multilayer heteroepitaxy on patterned Si (001) substrates. Self-assembled GeSi hut wire arrays are orderly grown inside patterned trenches with post growth surface flatness. Such embedded GeSi wires induce tensile strain on the Si surface, which results in preferential nucleation of Ge nanostructures. Ordered Ge nano-dashes, disconnected wires and continuous wires are obtained correspondingly by tuning the growth conditions. These site-controlled Ge nanowires on a flattened surface lead to the ease of fabrication and large-scale integration of nanowire quantum devices.

Introduction

Semiconductor quantum dots (QDs)[1] as a solid-state approach towards universal quantum computers[2] have attracted widespread attention. Early studies of quantum information such as spin state measurement[3] and coherent manipulation of qubits in neighbouring QDs[4] were mainly implemented on GaAs heterostructures. However, hyperfine interactions between electrons and nuclear spins in group III–V materials severely deteriorate their spin coherence.[5] Group IV semiconductors naturally contain a high-level of zero nuclear spin isotopes and can be further isotopically purified to suppress nuclear spins.[6] Silicon electron spin qubits can therefore bring a remarkable improvement in coherence time[7,8] and operation fidelities.[9] In recent years, germanium nanowires (NWs) have become a promising candidate for obtaining spin based[10] or even topological[11,12] quantum information due to their high mobility,[13] strong and tunable spin–orbit interaction (SOI),[14–16] capability of isotopic purification and CMOS compatibility. Thanks to these properties, ultrafast electrical manipulation of hole spin qubits with the Rabi frequency exceeding 540 MHz[17] and hard superconducting gaps up to magnetic fields of 250 mT[18] have been demonstrated in Ge NWs.

The scalability of the NW-based quantum devices, however, is still a major challenge. It is a prerequisite to obtain NWs with controlled positions and geometries for NW-based device applications. Conventional vapor–liquid–solid (VLS) methods are able to form uniform NWs and NW-networks.[19,20] However, these NWs typically grow out of the substrate plane and require to be transferred to a second substrate for device fabrication, which is an obstacle for scalability. The incorporation of a metal catalyst in VLS growth is another challenge for quantum devices, as it leads to decreased carrier mobility, parasitic channels and charge noises.[21,22] The direct growth of in-plane Ge NWs and NW-networks has been demonstrated *via* selective area growth[23] recently, but the crystalline imperfections such as dislocations and stacking faults still remain unsolved. By combining top-down fabrication and bottom-up self-assembly methods, site-controlled Ge hut wires (HWs) with perfect crystal quality have been previously demonstrated along the edges of pre-patterned trenches.[16] But these trenches generally create certain challenges for subsequent device fabrication. Tremendous efforts have been made to grow wires inside the shallow trenches; however, only GeSi HWs with low Ge concentrations were obtained.[24]

Strain-driven formation of nanoscale islands on lattice-mismatched layers in hetero-epitaxy offers an effective way to obtain coherent islands[25–29] and nanowires.[30] Liu *et al.* found that[27] the strain field induced by embedded strained islands in multilayer heteroepitaxial films leads to the formation of island columns with common size; their 2D model can be

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generally applied for the formation of multi-layer nanowires; however, due to the large lattice mismatch between Si and Ge, it is kinetically difficult to form long Ge wires.[31,32] Here, we demonstrate uniform Ge HW arrays on a flattened surface by multi-layer growth of strained Ge(Si) layers separated with Si spacer layers on top of site-controlled GeSi HWs. We first fabricate shallow trenches to obtain GeSi HWs with fully controlled positions followed by a surface flattening process *via* Si spacer layer growth under optimized growth conditions. The embedded GeSi HWs generate medium tensile strain on the surface of the Si spacer layers which results in the vertical stacking growth of ordered (Ge)Si HWs. Furthermore, by tuning the growth conditions, other ordered nanostructures such as nano-islands and dumbbells can also be obtained.

Experimental

Growth of Ge HWs

The trenches along the ⟨100⟩ direction are defined by 100 kV electron beam lithography and transferred to a 4-inch Si (001) wafer with an etching depth in the range of 6 to 9 nm, a width of ~60 nm and a length of ~2 μm using reaction ion etching. The patterned wafer is diced into 1 × 1 cm^2 die to fit the sample adaptor for epitaxial growth. Before loading into the molecular beam epitaxy (MBE) chamber, samples are cleaned by the RCA cleaning process and subsequently dipped into diluted hydrofluoric acid to remove the native oxide while obtaining a hydrogen passivated Si surface. After the dehydrogenation and degassing procedure at 720 °C in the MBE chamber, a 60 nm thick Si buffer layer is then deposited at a growth rate of 1 Å s^{-1}. Subsequently, three-layer growth of GeSi HWs is performed. The first layer of GeSi HWs (1st HWs) is obtained by depositing a 6 nm $Ge_{0.33}Si_{0.67}$ alloy (Si: 0.22 Å s^{-1}, Ge: 0.11 Å s^{-1}) at 450 °C followed by a one hour *in situ* annealing process at 530 °C. A Si capping layer (spacer layer) with a thickness of 21 nm is then deposited with the first 7 nm being grown at 350 °C and the remaining 14 nm at 530 °C. The lower growth temperature of 350 °C is to minimize the Si–Ge intermixing, while the higher temperature growth is performed to flatten the surface.[30] The second layer of GeSi HWs (2nd HWs) is achieved by depositing a 1.8 nm $Ge_{0.41}Si_{0.59}$ alloy (Si 0.13 Å s^{-1}, Ge 0.09 Å s^{-1}) upon the spacer surface followed by 1 hour *in situ* annealing. An additional 14 nm thick Si spacer layer (2nd spacer) is deposited with the first 7 nm being grown at 350 °C and the remaining 7 nm at 530 °C. Finally, a 6 Å thick Ge layer is deposited at an appropriate temperature to form different Ge nanostructures, followed by 3 nm thick Si deposition at 330 °C to protect the Ge HWs from oxidation.

Characterization

The surface morphologies were characterized *via* an *ex situ* Bruker multimode 8-HR atomic force microscopy (AFM) system in tapping mode. High angle annular dark field scanning transmission electron microscopy (HAADF-STEM) was performed using JEM-ARM200F instrument, and the STEM sample was fabricated using a Helions NanoLab 600i focus ion beam system.

Results and discussion

Growth and characterization of Ge HWs

Fig. 1 displays the schematic of Ge HW growth. Ordered GeSi HWs are obtained inside the trenches along the ⟨100⟩ direction. Furthermore, these HWs are capped by a Si spacer layer for surface flattening. Such embedded GeSi HWs provide accumulated strain fields on the surface of the Si spacer layer which results in vertical stacking. Ordered Ge HWs on a flattened surface are obtained after three-layer growth of Ge(Si).

Fig. 2 shows the growth process of Ge HWs. Fig. 2a is the AFM image showing the 1st HWs obtained after the deposition of a 6 nm thick $Ge_{0.33}Si_{0.67}$ alloy with subsequent 1 h *in situ* annealing. These 1st HWs are located inside the pre-patterned trenches. They are bound by {105} facets with approximately 9 nm in height and 2 μm in length. At both sides of the wires, there are still two shallow trenches existing with a depth of ~5 nm, as observed from the AFM line-scan across the HWs (black line in Fig. 2f). The surface is flattened after the 21 nm thick Si spacer layer growth. The AFM image in Fig. 2b shows the 2nd HWs after 1.8 nm $Ge_{0.41}Si_{0.59}$ deposition with subsequent 1 h *in situ* annealing. They exhibit an identical wire length of 2 μm and a wire height of ~8 nm. Shallow trenches appear at both sides of the 2nd HWs with a depth of ~2 nm, as shown in the blue line of Fig. 2f. The appearance of these shallow trenches is attributed to the diffusion of Si from highly strained regions (edges of the HWs[33]) into the HWs, which is well known in the case of large Ge islands obtained at a high growth temperature.[34,35] Outside these trenches, we observe satellite-islands with a height of ~6 nm. These satellite-islands intend to evolve into satellite wires at a higher annealing temperature (not discussed in this work). The growth of the satellite islands can be attributed to the spread

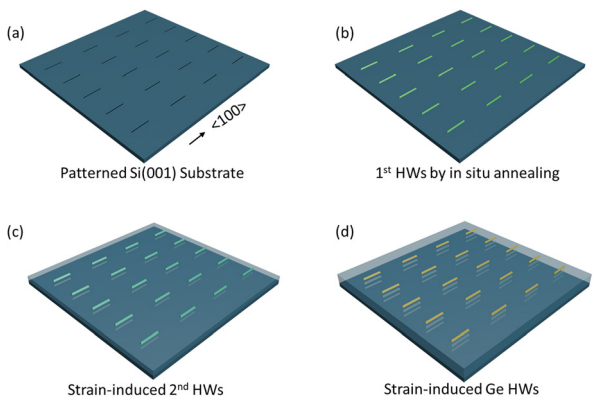

Fig. 1 Schematic of the growth of the site-controlled Ge HWs on Si (001). (a) Periodic trenches fabricated by the top-down process along the ⟨100⟩ direction. (b) 1st HWs obtained inside the trenches. Strain-induced (c) 2nd GeSi and (d) Ge HWs on the top of embedded HWs. Si spacer layers are shown semi-transparent.

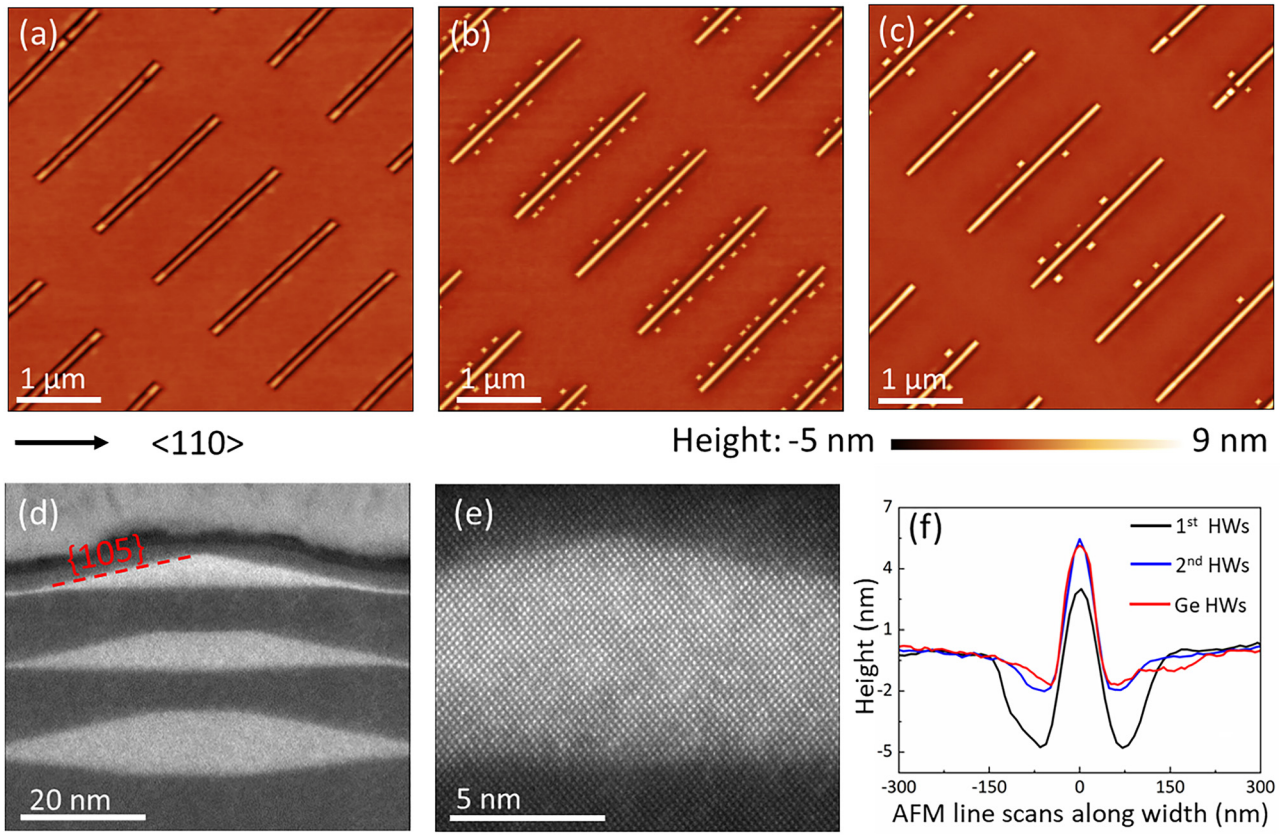

Fig. 2 Strain-induced site-controlled Ge HWs on a Si (001) substrate. (a–c) AFM images of: (a) 1st HWs within the trenches, strain-induced (b) 2nd GeSi and (c) Ge HWs on the top of embedded HWs. (d) Cross-sectional HAADF-STEM image of the vertical stacking growth of HWs and (e) atomic resolution HAADF-STEM image of the Ge HWs. (f) AFM line scans along the width of HWs show the morphological evolution during the three-layer growth; the thicknesses of the spacer and wetting layers are subtracted from the line scan tracers.

tensile strain over the surface of the Si space layer induced by the embedded HWs, where islands tend to nucleate next to the trench due to the attractive force from trench–island interactions.[36]

The 2nd spacer layer of 14 nm caps the 2nd HWs with an almost flattened surface. After subsequent deposition of the 6 Å Ge layer at 610 °C, the Ge HWs with a height of ~7 nm are obtained, as shown in Fig. 2c. They have a sidewall angle of 11.3° (red line in Fig. 2f) corresponding to the {105} facets, as further confirmed by the HAADF-STEM image in Fig. 2d. The strain-induced trenches and satellite-islands are also observed at both sides of the Ge HWs. It needs to be mentioned that although a pure Ge layer is deposited, the Ge HWs actually consist of GeSi alloys due to the Si–Ge intermixing.[15] The vertical alignment of the Ge(Si) HWs is characterized by the HAADF-STEM image in Fig. 2d. These HWs show a decreased lateral size with an elevated Ge content. We also see the truncated top of the 1st and 2nd layers of HWs, which are attributed to the Si–Ge intermixing during the spacer layer growth. Sharp interfaces between the HWs and the spacer layers are observed with no dislocations found in the cross-sectional area (Fig. 2d and e), indicating a high-quality crystal growth of Ge(Si) HWs. The morphological evolution of the three-layer growth is summarized with a line-scan as shown in Fig. 2f.

The overall site-controlled growth of the three-layer HWs is summarized as below. For the 1st layer HWs: the growth of HWs inside the shallow trenches with sidewall angles less than 10° (Fig. 2d and f) is driven by both the elastic relaxation and the exposed-surface minimization.[37] For the upper layer HWs: the nucleation and growth of Ge(Si) nanostructures in the tensile strain regions induced by the embedded HWs is energetically favourable,[26,27] in addition, the atomic diffusion of Ge contents over the Si spacer surface is also enhanced due to the tensile strain[31,32] induced by the embedded HWs, which leads to the lateral growth of long Ge(Si) HWs.

Ordered Ge nanostructures

To achieve precise control of ordered Ge HWs or other nanostructures, it is necessary to study how these growth parameters such as growth temperature, *in situ* annealing and spacer thickness may affect the formation of Ge nanostructures.

Firstly, all parameters of the sample in Fig. 2c are kept constant except lowering the Ge growth temperature from 610 °C

to 590 °C and 570 °C, respectively. The corresponding AFM images are shown in Fig. 3a and b. At a growth temperature of 590 °C, we observe disconnected HWs with a height of ~6 nm and a length ranging from hundreds of nanometres to micrometres (Fig. 3a). They are all oriented along the ⟨100⟩ direction, identical to the pre-patterned trenches. At the growth temperature of 570 °C, ~5 nm high nano-dashes with a length of tens or hundreds of nanometres are obtained. Furthermore, by performing 15 min *in situ* annealing at 570 °C after the Ge layer growth, these nano-dashes merge together into complete wires, as shown in Fig. 3d. They exhibit enlarged sizes with a height of ~11 nm, which indicates a stronger Si–Ge intermixing and a lower Ge content. Dumbbells or matchsticks[30] with islands positioned at the HW ends are also observed after the annealing. This is attributed to the induced tensile strain maxima on top of the HW endpoints by the embedded HWs, which is in line with the calculations in the following section.

The influence of the spacer thickness on the formation of Ge nanostructures has also been studied. After the deposition of the Ge layer under identical conditions as indicated in Fig. 3a, we increased the 2nd spacer layer thickness to 21 nm. Ordered 1D chains of Ge islands are obtained, as shown in Fig. 3c. These Ge chains consist of ~10 nm high hut islands and dome islands with a diameter of ~110 nm and a height of ~15 nm. By changing the growth temperature, chains of uniform dome islands can also be obtained. These results can be explained on the basis of the reduced tensile strain from the increased spacer thickness, which will also be discussed in details in the following section.

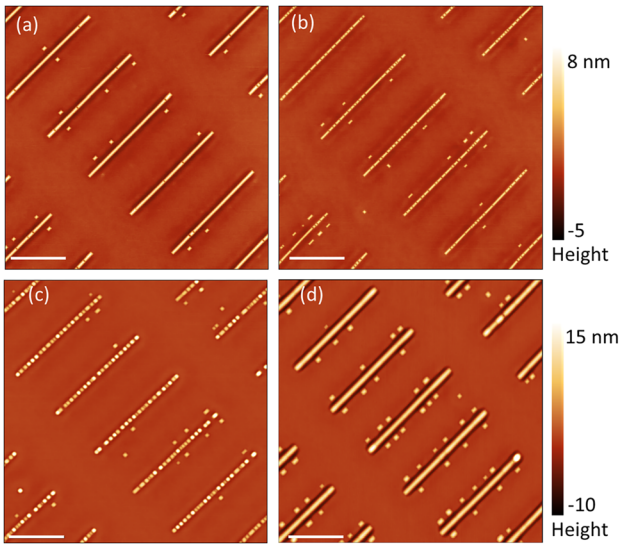

Fig. 3 AFM images of the Ge nanostructure on the top of embedded HWs. (a) Disconnected wires and (b) nano-dashes are obtained under the same growth conditions as Fig. 2(c) except that the temperature was lowered to 590 °C and 570 °C, respectively. (c) Dot chains are obtained under the same growth conditions as in (a) except that the 2nd spacer thickness was increased to 21 nm. (d) The same growth parameters as (b) but follows a 15 min *in situ* annealing at 570 °C after the Ge layer growth. Scale bar: 1 μm.

Strain field calculations

In this section, the surface strain distributions induced by the embedded HWs are calculated. As introduced in ref. 30, the HWs can be treated as a collection of individual ultra-thin cuboids with volume $V = l \times w \times h$ (where l, w and h are the length, width and thickness of the cuboids, respectively) along the growth direction. For each cuboid at a spacer thickness d, the exact formula for the trace of the strain tensor on the spacer surface $(x, y, 0)$ is given by:[38]

$$\varepsilon = \frac{\varepsilon_0(1+\nu)(1-2\nu)}{\pi(1-\nu)} \times \sum_{i,j,k=2}^{2} (-1)^{i+j+k} \tan^{-1} \frac{x_i y_j}{z_k \sqrt{x_i^2 + y_j^2 + z_k^2}}$$

where $x_i = x \pm l/2$, $y_i = y \pm w/2$, $z_1 = d$ and $z_2 = d - h$. $\nu = 0.218$ is the Poisson's ratio of the spacer material, $\varepsilon_0 = (a_{\mathrm{GeSi}} - a_{\mathrm{si}})/a_{\mathrm{Si}}$ is the lattice misfit ratio. For GeSi/Si, a_{si} = 5.431 Å, $a_{\mathrm{Ge_{0.33}si_{0.67}}}$ = 5.5 Å, and $a_{\mathrm{Ge_{0.41}si_{0.59}}}$ = 5.517 Å.[39]

The surface strain field induced by both the 1st and 2nd layers of HWs on the 2nd spacer surface is shown in Fig. 4a. The 1st layer HWs have a Ge content of 0.33 with w_1 = 90 nm (9 nm in height), l_1 = 2000 nm and d_1 = 35 nm. The 2nd layer HWs exhibit an increased Ge content of 0.41 with w_2 = 80 nm (8 nm in height), l_2 = 2000 nm and d_2 = 14 nm. The HW dimensions are extracted from the sample in Fig. 2f. The embedded HWs generate tensile strain on the surface of the Si spacer layer right above the HWs, with existing compressive strain located surrounding the tensile strain area, as is further shown by the line-scan of the surface strain along the width and length directions passing through (0,0,0) orientations (red lines in Fig. 4c and d), respectively. It should be noted that tensile strain regions are energetically favorable for the nucleation and growth of Ge(Si) nano islands. Under certain growth conditions, these Ge(Si) nano islands can also merge into wires in intact form, as schematically illustrated in Fig. 4b. In addition, surface strain calculations are also performed at different Si spacer thicknesses. At an increased spacer thickness of d_2 = 21 nm and d_1 = 42 nm, the tensile strain drops dramatically and distributes more widely along the width direction (black lines in Fig. 4c and d). Ge on such a low tensile strained Si spacer layer has a large diffusion barrier, which leads to the formation of islands.

It is interesting to note that most of our results on HW formation (non-uniform distribution of the strain field and modification of the spacer thickness to the surface strain) are perfectly in line with previous works[25–27,40–43] that focus on the growth of islands. Their model and analysis can be applied to multilayer nanowire formation universally. However, for Ge growth on a Si layer, the large lattice mismatch leads to a large diffusion barrier,[31,32] making it difficult to form long Ge wires. In our approach, we first grow GeSi, which can easily form wires due to the medium lattice mismatch strain; the tensile strain in the Si spacer layer induced by the embedded GeSi wires favours the Ge diffusion and leads to long wire for-

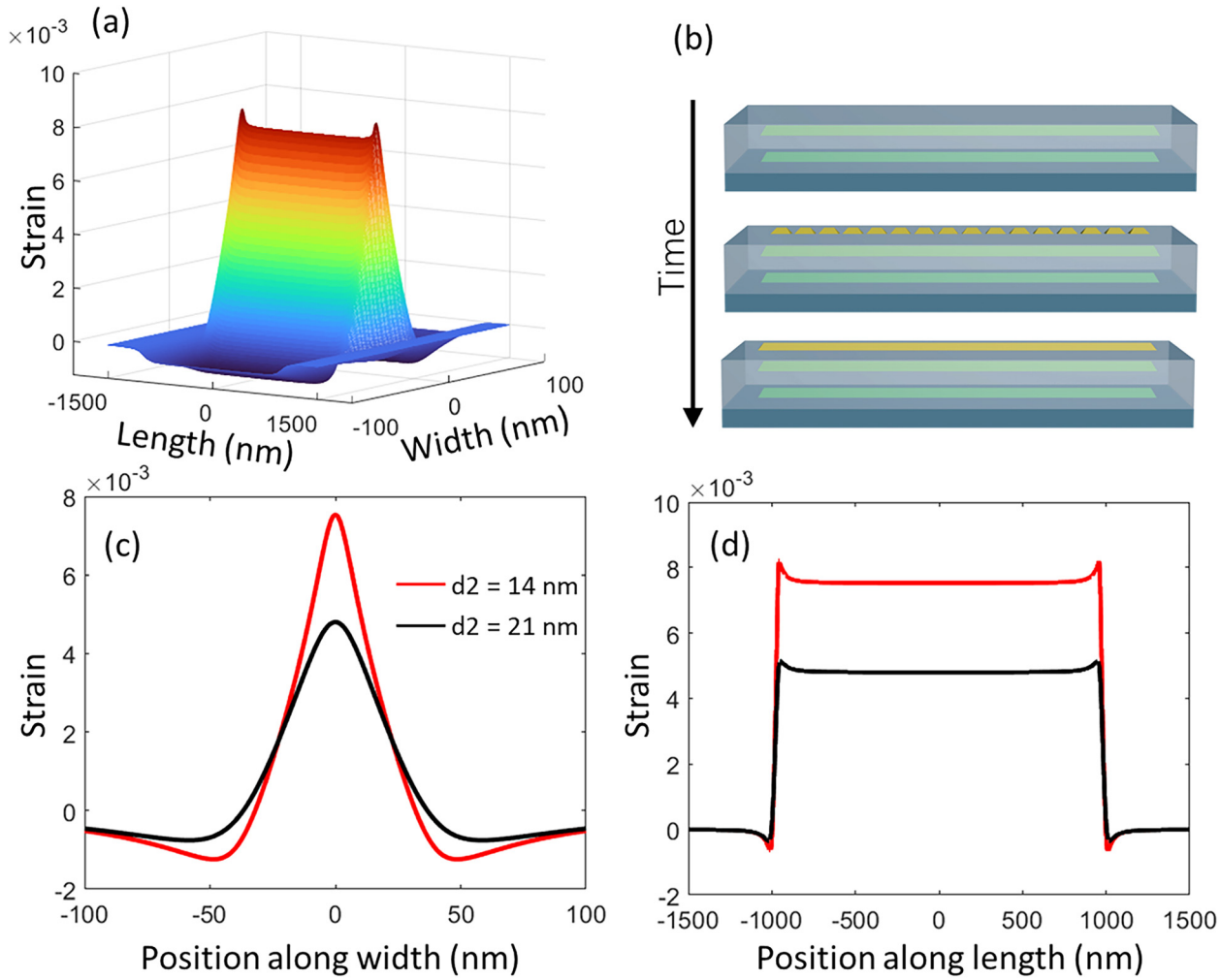

Fig. 4 (a) Surface strain profile induced by two embedded HWs, with the 1st HWs w_1 = 90 nm (9 nm in height), l_1 = 2000 nm and d_1 = 35 nm and the 2nd HWs w_2 = 80 nm (8 nm in height), l_2 = 2000 nm and d_2 = 14 nm. (b) Schematic illustration of the morphological evolution of Ge HWs. (c and d) Line scans of the surface strain profile along (c) the width and (d) the length directions passing through (0,0,0).

mation. The growth of the 1st and 2nd layers of GeSi HWs serves as somehow a "physical catalyst", by lowering the kinetic barrier for the growth of the desired long Ge HWs.

Finally, it should be noted that the growth of self-organized strain induced HWs is a complex process that involves a number of conditions such as the growth temperature, the deposition rate, and the growth thickness. In our model, we focus on the growth regime where the chemical potential is mainly determined by the surface strain field. Once at a high growth temperature, the surface islands nucleate and grow continuously, leading to the formation of multifaceted domes with steeper facets. The surface energy[44] and island–island repulsion[36] would have a more pronounced influence on the nanostructure growth. A more advanced model (*e.g.*, an extension of the approach proposed in ref. 44) would clearly be required for these growth regimes to complete the entire mechanism of lateral nanostructure growth by tackling subtle issues such as determining the critical spacer layer thickness of whether small islands transform into intact wires or domes. In addition, the Si–Ge intermixing[45] during the growth would also need to be considered more carefully. However, some qualitative conclusion can be reached at the current stage. At a lower growth temperature (Fig. 3b), the diffusion length of surface atoms is reduced, therefore, an insufficient amount of Ge atoms is accumulated in the preferential growth regions, leading to the formation of only small islands or nano-dashes. Due to the island–island repulsion[36] force and insufficient diffusion, these small islands or nano-dashes cannot merge into short wires but remain separated as island/dash arrays. But these closely spaced islands or dashes will merge together into disconnected wires (Fig. 3a) and eventually form intact wires only at an increasing growth temperature (Fig. 2c) or optimized *in situ* annealing (Fig. 3d).

Conclusions

In summary, we developed a catalyst-free method to grow ordered Ge HWs on the Si (001) surface. The influences of

growth temperature, annealing and spacer layer thickness on nanostructure formation are investigated through both experiments and surface strain calculations. Ordered Ge dashes, disconnected wires or dot chains can also be obtained by simply tuning the growth parameters. The pre-patterned trenches are flattened during the growth, which avoids negative impacts towards the subsequent device fabrications. In addition, special geometries such as square-shaped, T-shaped or cross-shaped HWs can also be realized by coalescence of perpendicular close spaced HWs. Monolithic growth of these HWs and HW networks will provide an alternative approach for investigating integrated spin qubits and Majorana fermions.

Author contributions

Ming Ming: data curation (lead), formal analysis (lead), investigation (lead), methodology (equal), and writing – original draft (lead). Fei Gao: data curation (lead), investigation (lead), and methodology (equal). Jian-Huan Wang: formal analysis (equal), investigation (equal) and methodology (equal). Jie-Yin Zhang: investigation (equal). Ting Wang: methodology (equal), resources (equal), supervision (equal) and writing – review and editing (equal). Yuan Yao: data curation (equal). Hao Hu: methodology (equal), supervision (equal) and writing – review and editing (equal). Jian-Jun Zhang: formal analysis (lead), funding acquisition (lead), project administration (lead), resources (lead), supervision (lead) and writing – review and editing (lead).

Conflicts of interest

There are no conflicts to declare.

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