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PAPER

Low temperature (Zn,Sn)O deposition for reducing interface open-circuit voltage deficit to achieve highly efficient Se-free $Cu(In,Ga)S_2$ solar cells†

Mohit Sood, *[a] Damilola Adeleye,[a] Sudhanshu Shukla,[a] Tobias Törndahl, [b] Adam Hultqvist[b] and Susanne Siebentritt [a]

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$Cu(In,Ga)S_2$ holds the potential to become a prime candidate for use as the top cell in tandem solar cells owing to its tunable bandgap from 1.55 eV ($CuInS_2$) to 2.50 eV ($CuGaS_2$) and favorable electronic properties. Devices above 14% power conversion efficiency (PCE) can be achieved by replacing the CdS buffer layer with a (Zn,Mg)O or Zn(O,S) buffer layer. However, the maximum achievable PCE of these devices is limited by the necessary high heating temperatures during or after buffer deposition, as this leads to a drop in the quasi-Fermi level splitting (qFLs) and therefore the maximum achievable open-circuit voltage (V_{OC}). In this work, a low-temperature atomic layer deposited (Zn,Sn)O thin film is explored as a buffer layer to mitigate the drop in the qFLs. The devices made with (Zn,Sn)O buffer layers are characterized by calibrated photoluminescence and current–voltage measurements to analyze the optoelectronic and electrical characteristics. An improvement in the qFLs after buffer deposition is observed for devices prepared with the (Zn,Sn)O buffer deposited at 120 °C. Consequently, a device with a V_{OC} value above 1 V was achieved. A 14% PCE is externally measured and certified for the best solar cell. The results show the necessity of developing a low-temperature buffer deposition process to maintain and translate absorber qFLs to device V_{OC}.

Introduction

Realizing power conversion efficiency (PCE) above 30% using tandem solar cells needs high-efficiency high bandgap ~1.5–1.7 eV solar cells to couple with the current state-of-the-art low bandgap solar cells, namely Si, $Cu(In,Ga)Se_2$.[1,2]

[a]*Laboratory for Photovoltaics, Department of Physics and Materials Science, University of Luxembourg, Belvaux, L-4422, Luxembourg. E-mail: mohit.sood@uni.lu*
[b]*Solar Cell Technology, Department of Materials Science and Engineering, Uppsala University, Uppsala, 751 21, Sweden*

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$Cu(In,Ga)S_2$ can fulfill the role of the top cell as it possesses a bandgap (E_G) which is tunable from 1.55 eV ($CuInS_2$) to 2.5 eV ($CuGaS_2$),[3] which can be tuned to perfectly match the bandgap needed to pair with the bottom solar cell, together with suitable electronic properties. The 15.5% PCE of state-of-the-art $Cu(In,Ga)S_2$ further shows the promise of the material.[4] However, the open-circuit voltage (V_{OC}), which is the difference between the electron Fermi level at the front contact and the hole Fermi level at the back contact, is significantly lower (~340 mV) than the maximum achievable Shockley–Queisser V_{OC} (ref. 5) in the best device. Significant inroads must be made to improve the V_{OC} of $Cu(In,Ga)S_2$ to deploy it as a top cell.

In general, achieving a high V_{OC} in a solar cell requires high quasi-Fermi level splitting (qFLs) inside the absorber. Since the qFLs depends majorly on the minority Fermi level under low excitation conditions, high qFLs require significant suppression of non-radiative recombination centers in the bulk of the absorbers.[6] Once a good qFLs is ensured, the next step is to properly translate the qFLs into V_{OC}.

Improving the V_{OC} of $Cu(In,Ga)S_2$ solar cells

Chalcopyrite solar cells comprise a complex multi-layered structure (Mo/$Cu(In,Ga)S_2$/buffer/i-layer/Al:ZnO), resulting in many interfaces. Any of these interfaces can be a source of a significant reduction in either or both the electron and hole Fermi-levels, thus reducing the V_{OC} of the final device. This results in an interface V_{OC} deficit, an important metric to quantify the transport loss in the device, which is defined as the difference between the optically measured qFLs/e of the device and the electrically measured V_{OC} of the device.[7] Several factors can lead to interface V_{OC} deficit; the most common ones are – (i) unfavorable band-offsets at the various interface and (ii) a high density of defects near the interface.

A negative conduction band offset at the absorber/buffer interface is the most common source of interface V_{OC} deficit. The Cu-poor $Cu(In,Ga)S_2$ devices prepared with a CdS buffer layer have been known to suffer from interface V_{OC} deficit[8] owing to a negative conduction band offset (CBO) or 'cliff' at the absorber/buffer interface, *i.e.* the conduction band minimum (CBM) energy of the absorber being higher than the conduction band minimum of the buffer.[9] The presence of the cliff-type CBO at the $Cu(In,Ga)S_2$/CdS interface results in an interface bandgap that is lower than the bulk bandgap. Consequently, the activation energy (E_a) of the dominant recombination current is less than the E_G of the absorber.[8] This causes recombinations at the absorber/buffer interface to dominate, and the electron Fermi-level drops at the interface. Hence the V_{OC} is significantly reduced in comparison to the qFLs/e ('e' is the elementary charge), causing an interface V_{OC} deficit in the device.

Replacement of the traditional CdS buffer layer with an alternate buffer layer, such as Zn(O,S) and ZnMgO, with a higher CBM is a proven solution to mitigate the interface V_{OC} deficit due to a cliff-type CBO.[8,10] However, caution must be exercised when making devices with higher CBM buffer layers. The standard CdS buffer layer is known to already have a cliff-type CBO with the ZnO i-layer.[11] And replacing it with a higher CBM buffer would result in an even larger conduction band cliff at the buffer/i-layer interface. For example, we recently studied CIGSu devices prepared with varying Mg content in (Zn,Mg)O films as a buffer layer

paired with a ZnO i-layer.[10] The (Zn,Mg)O films are known to have a higher CBM than that of ZnO, which increases with increasing Mg content in the films.[12] It was found that devices having a high Mg content and, therefore, a large cliff type CBO at the buffer/i-layer interface display a higher interface V_{OC} deficit compared to devices prepared with low Mg content, *i.e.* with a lower negative CBO at the interface.[10] The deficit originates due to a drop in the electron potential near the buffer/i-layer interface, as observed in numerical simulations.[10] The loss can be reduced by substituting the ZnO i-layer with a higher CBM i-layer. For example, it has been shown that ZnMgO buffer devices made with an Al:ZnMgO i-layer possess a significantly lower interface V_{OC} loss compared to those of ZnO i-layer devices.[10]

Besides the negative CBOs at the various interface, a high density of defects inside the absorber near the interface can be another source of the interface V_{OC} deficit in Cu(In,Ga)S_2 devices. Sulfide as well as selenide based Cu(In,Ga)S(e)$_2$ solar cells realized with an as grown Cu-rich absorber – overall [Cu]/[In + Ga] > 1 – are known to possess high interface V_{OC} deficits even with perfect band alignment at the absorber/buffer and buffer/i-layer interfaces.[13,14] This deficit has been linked to the presence of a high density of acceptor defects near the absorber/buffer interface.[7,15] These defects near the interface act as non-radiative recombination centers and therefore cause a drop in the electron Fermi-level near the absorber/buffer interface.[7] Consequently, the devices suffer from low V_{OC} and, hence, an interface V_{OC} deficit.

The near interface defect formation has been linked to the etching of the Cu_{2-x}S(e) secondary phase that is necessary for working devices, independent of the etchant used.[7,16] The interface V_{OC} deficit due to near interface defects could be somewhat mitigated by doing an S or Se post-deposition treatment after the etching or avoided by making devices using Cu-poor absorbers – [Cu]/[In + Ga] < 1 [14,15,17] – making the etching step unnecessary.

Therefore, the qFLs/*e* translation in chalcopyrite solar cells can be hampered by recombinations occurring at or near the absorber/buffer interface or the buffer/i-layer interface.[14] It must be noted that the interface V_{OC} deficit can also originate from the molybdenum/absorber interface. However, this is something that is not commonly observed in Cu(In,Ga)S_2 devices.

The deposition processes of the buffer, i-layer, or window, when performed at elevated temperatures, can damage the absorber and lead to qFLs loss and consequently result in a lower V_{OC} and, therefore, a global interface V_{OC} deficit. In our recent work, though a device with PCE > 15% could be achieved using a Zn(O,S) buffer layer, the device still possessed an interface V_{OC} deficit of ~40 mV. It was found that the deficit originates due to a loss in the qFLs after the necessary air annealing of the absorber/buffer stack at ~200 °C. This annealing is necessary as devices with high PCE are only realized after air annealing the absorber/buffer stack at ~200 °C.[14]

Thus, achieving higher V_{OC} values in Cu(In,Ga)S_2 solar cells requires mitigation of the above-discussed losses. This can be achieved by using absorbers with a good surface, *i.e.* Cu-poor Cu(In,Ga)S_2 films, an alternate buffer layer that has an optimum CBO (0.0 eV to 0.40 eV) with the absorber,[18] and an i-layer that has a suitable CBO with the buffer. In addition, the buffer and i-layer film should not require high temperatures during or after deposition.

The record Cu(In,Ga)S_2 device has been achieved using an atomic layer deposited (ALD) $Zn_{1-x}Mg_xO$ buffer.[4] Motivated by this fact, we recently explored the ALD $Zn_{1-x}Mg_xO$ buffer layer deposited at 150 °C as an alternate to the Zn(O,S) buffer layer for Cu(In,Ga)S_2 solar cells, with $E_G \sim 1.6$ eV.[10] A high $V_{OC} \sim 943$ mV and a PCE $\sim$ 14% were achieved using an $x = 0.27$ $Zn_{1-x}Mg_xO$ buffer layer. However, even this device exhibited a V_{OC} which was 40 mV lower than the qFLs of the bare absorber. This deficit is partly due to the loss in the qFLs that originated from the ~150 °C temperature required for buffer deposition, which is still detrimental to device optoelectronic properties, and the rest to the contact loss.[10]

ALD (Zn,Sn)O is another promising buffer layer and has helped to achieve a V_{OC} of 1 V for $CuGaSe_2$ devices.[19] Other than this, the (Zn,Sn)O buffer grown at low temperature of 90–125 °C is known to produce high PCE Cu(In,Ga)Se_2 solar cells.[19,20] Moreover, the CBM of ALD (Zn,Sn)O can be tuned either by keeping the composition fixed and varying the deposition temperature[20] or keeping the deposition temperature fixed and varying the [Sn]/([Zn + Sn]) composition.[21]

In this work, we explore the impact of an atomic layer deposited (ALD) zinc tin oxide (Zn,Sn)O buffer layer deposited at two different temperatures, 105 °C and 120 °C (keeping the composition constant), as a partner for Cu-poor Cu(In,Ga)S_2 solar cells. The benefit of the low growth temperature $\leq$ 120 °C on the Cu-poor Cu(In,Ga)S_2 devices' properties, particularly the interface V_{OC} deficit, is explored. Moreover, a variety of i-layers, namely ZnO, Al:ZnMgO, and no i-layer at all, are used as a partner for the buffer layer. The resulting devices' electrical characteristics are measured using current–voltage and external quantum efficiency measurements of the solar cells. Calibrated photoluminescence measurements are performed on the bare absorber and buffer coated absorbers to obtain the qFLs values. The extracted V_{OC} values are compared to the qFLs/e values measured on the bare absorber, and the interface V_{OC} deficits are compared for the different devices. The results presented show that a low-temperature ALD ZnSnO buffer layer with an Al:ZnMgO i-layer can help attain a high PCE in Cu(In,Ga)S_2 devices with an interface V_{OC} deficit comparable to those of the state-of-the-art Cu(In,Ga)Se_2 devices.[22]

Experimental

Absorber deposition

The Cu-poor Cu(In,Ga)S_2 absorbers were prepared on molybdenum coated soda-lime glass substrates *via* a 3-stage co-evaporation process at a temperature of ~570 °C with a final film thickness of ~2 μm. The desired absorber stoichiometry was obtained by controlling the evaporation flux of the Cu, In, and Ga sources and the durations of the three stages of the process. The final bulk compositions of the as-grown absorbers were determined using energy-dispersive X-ray spectroscopy (EDX). The as-deposited absorbers used in this study had a [Cu]/[In + Ga] $\sim$ 0.94 and a [Ga]/[Ga + In] $\sim$ 0.14.

Buffer deposition

The $Zn_{1-x}Sn_xO_y$ buffer layer deposition was carried out in an F-120 Microchemistry system using diethyl zinc (DEZ), tetrakis(dimethylamino)tin (TDMASn) and DI water (as a co-reactant) as precursors, with N_2 as the carrier and purge gas.

A super-cycle approach with a fixed ZnO : SnO_x pulse ratio of 1 : 1 at two different deposition temperatures, 105 °C and 120 °C, was used to deposit (Zn,Sn)O. The buffers at 120 °C were deposited with a total of 750 cycles, whereas the buffers at 105 °C used 938 cycles to compensate for a lower growth per cycle value. The x-values were measured to be 0.19 at 105 °C and 0.18 at 120 °C by X-ray fluorescence on corresponding soda-lime glass pieces placed in the reactor together with the $Cu(In,Ga)S_2$ samples in each run. Throughout this work, the buffers deposited at 105 °C and 120 °C are denoted as B1 and B2, respectively.

i-layer and window layer deposition

The ZnO and Al:ZnMgO i-layer and Al:ZnO window layer deposition was carried out using magnetron sputtering. The sputtering process for Al:ZnMgO was based on a previous work on ZnMgO.[18] The 2-inch undoped ZnO target at 125 W and 2-inch 2 wt% Al_2O_3 doped ZnO target at 140 W were sputtered to deposit i-ZnO and Al:ZnO layers, respectively. Whereas, for depositing $Al:Zn_{1-x}Mg_xO$ with the desired composition of $x = 0.25$, 2-inch targets of MgO with 2 wt% Al_2O_3 and (undoped) ZnO were co-sputtered at a power of 80 W and 110 W, respectively. All the layers were deposited at 1.0 mTorr argon (99.99%) partial pressure, which was maintained with the help of a mass flow controller.

After i-layer and window deposition, using e-beam evaporation, nickel and aluminum metal grids were deposited on the samples to complete the device fabrication process. Devices of area ~0.5 cm^2 were realized by mechanical scribing. On the best device, an anti-reflective coating (ARC) of MgF_2 was deposited using e-beam evaporation.

Characterization methods

EDX with an operating voltage of 20 kV was used for determining the bulk stoichiometry of the as-grown absorbers. As for buffer thickness and stoichiometry measurements, fused silica glass was used, which was placed in each run as a witness sample. The thicknesses of the (Zn,Sn)O layers were estimated by X-ray reflectivity measurements and the stoichiometry using EDX measurements performed at 20 kV.

The qFLs measurements were done using calibrated photoluminescence (PL) using the procedure described in our previous work.[23] The V_{OC} measurements and J–V properties were measured using a xenon short-arc lamp AAA-Standard solar simulator together with an IV source-measure unit. The simulator was calibrated to air mass 1.5 global using a Si reference cell. The devices were measured in the forward sweep direction from −0.5 V to 1.5 V with a sweep speed of 50 mV s^{-1}. For determining the external quantum efficiency (EQE) of the devices, a setup consisting of halogen and xenon lamps, a grating monochromator, a chopper, and calibrated reference diodes was used. The current was measured using a lock-in amplifier and the intensity of the light by calibrated reference diodes.

Results and discussion

Fig. 1 shows the one sun-calibrated PL spectra of devices before and after buffer deposition. Among the two buffer layers, the (Zn,Sn)O buffer layer deposited at 120 °C (B2) leads to a very minute deterioration in the PL signal of the device. In

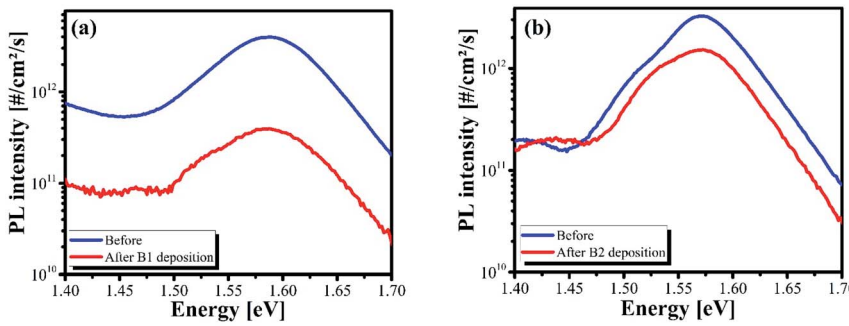

Fig. 1 (a) Absolute calibrated photoluminescence spectra of Cu(In,Ga)S_2 before and after (Zn,Sn)O buffer layer was deposited at (a) 105 °C (B1) and (b) 120 °C (B2), measured at an illumination intensity equivalent to one sun.

contrast, the buffer deposited at 105 °C (B1) leads to a one-order of magnitude drop in the PL signal. Consequently, the qFLs/e drops by 49 mV for the B1 device and 11 mV for the B2 device compared to the bare absorbers.

Fig. 2a shows the J–V characteristic curves of the best devices prepared with a (Zn,Sn)O buffer layer deposited at either 105 °C (B1) or 120 °C (B2), shown by dotted and solid lines, respectively. The corresponding electrical characteristic values are reported in Table 1. The PCEs of the devices were obtained by using the following expression:

$$\mathrm{PCE} = J_{\mathrm{SC}} \times V_{\mathrm{OC}} \times \mathrm{FF}/P_{\mathrm{in}},$$

where P_{in} is the input power, J_{SC} is the short-circuit current density and FF is the fill factor. The statistical distribution of J–V characteristics follows a trend similar to the one for best devices reported in Table 1 and can be found in the ESI (Fig. S1 and S2†).

Among the B1 devices, the device without an i-layer yields the highest V_{OC} and consequently possesses the lowest interface V_{OC} deficit, followed by the Al:ZnMgO

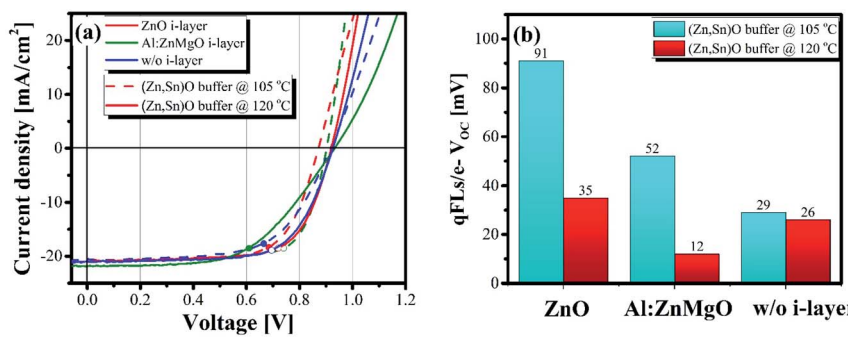

Fig. 2 (a) The characteristic J–V curves of the Cu(In,Ga)S_2 devices prepared with (Zn,Sn)O buffer layers deposited at 105 °C (B1) and 120 °C (B2), represented by dashed and solid lines respectively. The devices prepared with ZnO, Al:ZnMgO and without an i-layer are represented by red, green and blue lines, respectively. (b) Interface V_{OC} deficit bar plot of devices made with B1 and B2 with various i-layer combinations.

Table 1 *I–V* characteristics of the best Cu(In,Ga)S_2 devices prepared with (Zn,Sn)O buffer layers deposited at 105 °C (B1) and 120 °C (B2) using different i-layer combinations. The qFLs/*e* values reported are measured on the bare absorber. The J_{SC} values reported in the table are the ones measured by integrating the external quantum efficiency spectra

Buffer layer	i-layer	PCE (%)	FF (%)	J_{SC} (mA cm^{-2})	V_{OC} (mV)	qFLs/*e* @1 sun (mV)	qFLs/*e* − V_{OC} (mV)	R_s (Ω cm^2)	R_{sh} (Ω cm^2)
ZnSnO 105 °C	ZnO	12.6	68.4	21.1	872	963	91	3.3	730
ZnSnO 105 °C	Al:ZnMgO	13.7	73	21.0	902	954	52	1.3	831
ZnSnO 105 °C	W/o	11.8	62.3	20.6	917	946	29	4.5	303
ZnSnO 120 °C	ZnO	13.3	69	21.0	920	955	35	2.0	800
ZnSnO 120 °C	Al:ZnMgO	11.2	55	21.9	932	944	12	9.8	2232
ZnSnO 120 °C	W/o	13.2	67.7	21.0	926	952	26	3.0	1141

i-layer device and the ZnO i-layer device (see Fig. 2b). However, the device without an i-layer exhibits the worst PCE. This is because the device has a significantly lower fill factor (FF) than those of the Al:ZnMgO and ZnO i-layer devices. On the other hand, the Al:ZnMgO i-layer device exhibits the highest FF and a relatively low interface V_{OC} deficit compared to those of the ZnO i-layer device among the three B1 devices. The device thus possesses the highest PCE of $\sim$ 13.7% among the devices prepared in this study (see Table 1).

To contemplate why the three B1 devices have different FF, the light *J–V* curves of the device were fitted with the one-diode model using the *J–V* routine to extract the series and shunt resistance of the device.[24] The values are reported in Table 1. The B1 device without an i-layer has a significantly higher series resistance R_s (4.5 Ω cm^2) than the B1 devices with a ZnO (2.3 Ω cm^2) or Al:ZnMgO (1.3 Ω cm^2) i-layer (see Table 1). This trend is in line with the FF observations for the devices, suggesting that the FFs of the device without an i-layer and the ZnO i-layer device are limited primarily due to the high R_s in the devices.

Apart from the high R_s, the low FF of the device without an i-layer also results partly from the low shunt resistance R_{sh} (303 Ω cm^2). This could have possibly originated from the sputter deposition of highly conductive Al:ZnO directly on top of the buffer.[25–27] It is possible that the buffer is easily damaged during the sputtering. Hence, during Al:ZnO deposition, the highly conductive window layer comes directly into contact with the absorbers, or worse, with the back contact, resulting in shunting pathways in the device. Therefore, these results suggest that B1 does not provide adequate protection from sputter damage.

As for B2 devices, the Al:ZnMgO i-layer device remarkably exhibits a V_{OC} value of 932 mV, the highest among all the devices prepared in this study. Consequently, it has an interface V_{OC} deficit of a mere 12 mV (see Table 1), which is on par with those of the state-of-the-art Cu(In,Ga)Se_2 devices.[22] When compared to B1 devices with the same i-layer, the B2 devices exhibit a higher V_{OC}, thus, a lower interface V_{OC} deficit value than their counterparts (see Fig. 2b). This suggests that

B2 provides better protection against absorber qFLs loss during the i-layer and window deposition processes. The better protection may be related to the fact that ALD deposited (Zn,Sn)O films grown at higher temperatures with similar compositions are known to be characterized with denser morphologies.[28]

Unexpectedly, the device with an Al:ZnMgO i-layer performs the worst among this lot. If not for the poor FF, the device would have PCE $\sim$ 15% without the ARC coating (assuming a similar FF value of 73%, as achieved with the B1 Al:ZnMgO device). Since devices with another batch of absorbers (not shown here) display significantly higher FFs, we treat this as an outlier.

Among all B2 devices, the ZnO i-layer device has the highest PCE $\sim$ 13.3%. The device displays a 50 mV improvement in the V_{OC} compared to the B1 ZnO i-layer device, and hence a low interface V_{OC} deficit in the device of $\sim$35 mV. Consequently, it has a 0.7% gain in absolute PCE when compared to the B1 ZnO i-layer device.

The device without an i-layer performs equally well as the ZnO i-layer B2 device. This device also shows significant improvement when compared to the B1 device made without an i-layer. While the interface V_{OC} deficit remains nearly the same, it is the FF in B2 without the i-layer device that makes all the difference. As is evident from Table 1, the absolute FF improves by 5.4%, which can be attributed to a lower R_s value of $\sim$3.0 Ω cm^2 and a significantly higher R_{sh} value of $\sim$1141 Ω cm^2 as compared to an R_s value of 4.5 Ω cm^2 and R_{sh} value of 303 Ω cm^2 in the B1 device. In fact, all the B2 devices possess R_{sh} values higher than those of the B1 devices. This is a direct indication that B2 provides better protection from any sputter-induced damage to the junction. B2 being deposited at a higher temperature might be the reason for it, as it is less amorphous than B1. Consequently, devices made with it could be less prone to sputter damage during the sputtering of the i-layer and window layer, hence possessing higher V_{OC}, FF and PCE.

To achieve an even higher PCE from the best device obtained in this study, *i.e.* the Al:ZnMgO i-layer device with B1, it was covered with 110 nm MgF_2 ARC coating to decrease the optical losses observed in EQE (Fig. S3†). The device was certified to have a PCE of 13.98 $\pm$ 0.39% by the Fraunhofer Institute for Solar Energy Systems. The PCE was obtained by calculating the ratio of maximum-power out from the device to the power-in from solar simulation, *i.e.* one sun. A different procedure was used as the device displayed different current–voltage *I*–*V* curves when measured in the forward (negative to positive) and backward (positive to negative) applied voltage directions (see Fig. 3). Transient *I*–*V* characteristics were measured until stable voltage, current, and power values were reached (see Fig. S4†). This power-point was then used as the maximum power-point to calculate the PCE of the device. The device had a measured V_{OC} of 911.8 $\pm$ 9.2 mV and 908.9 $\pm$ 9.1 mV, an I_{SC} of 9.71 $\pm$ 0.18 mA and 9.70 $\pm$ 0.18 mA and a FF of 72.31% and 69.93% in the forward and reverse measurement directions, respectively, after obtaining a stable maximum power-point.

Towards 1 V V_{OC} using a thicker buffer

We have previously observed that the density of the buffer has a major impact on the qFLs loss, thus, it is reasonable to assume that the thickness might also have a significant impact on the qFLs value. Therefore, we also explored the impact of

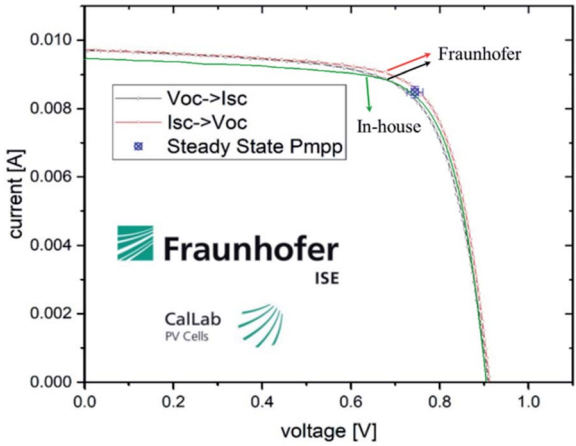

Fig. 3 Cu(In,Ga)S_2/(Zn,Sn)O/Al:ZnMgO/Al:ZnO certified *I–V* curves of the 14.0% efficiency device measured at the Fraunhofer Institute for Solar Energy Systems. The red curve is the measurement from the short-circuit current to the external open-circuit voltage, and the black curve is the measurement from the external open-circuit voltage to the short-circuit current. The olive curve is the in-house measurement. The blue square point shows the steady-state maximum power-point of the device achieved by keeping the device at V_{mpp} for 5 minutes.

the (Zn,Sn)O B2 buffer thickness (by varying the total ALD cycles) on the qFLs of the absorber. Five different numbers of cycles were used – 350, 550, 750, 1000, and 1250 cycles.

Fig. 4a shows the variation in the qFLs as a function of the total (Zn,Sn)O buffer ALD cycles. The qFLs loss decreases with increasing ALD cycles and even increases for the device with 1250 buffer cycles . A thicker buffer or mild annealing at 120 °C might be the origin of this improvement.

Cu(In,Ga)S_2 absorbers grown with high Ga in the first stage of the three-stage growth process with a bandgap of 1.61 eV possess qFLs values higher than 1 eV

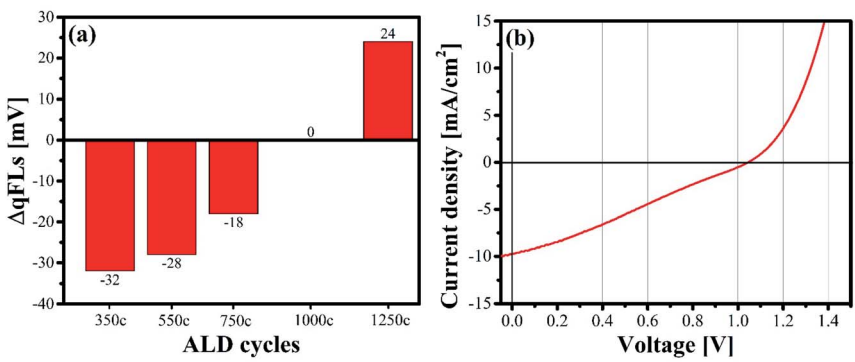

Fig. 4 (a) Bar chart showing the change in the qFLs of Cu(In,Ga)S_2 absorber before and after buffer deposition as a function of the (Zn,Sn)O buffer thickness. (b) The characteristic *J–V* curve of the Cu(In,Ga)S_2 device prepared with a50 nm thick (Zn,Sn)O buffer layer deposited at 120 °C.

(obtained from the band to band transition of the PL spectrum).[29] Devices prepared using these absorbers together with the optimized buffer thickness resulted in a device V_{OC} value of ~1.04 V (see Fig. 4b). However, the device possessed poor FF and J_{SC} values and consequently had a mere 2.5% PCE. Nonetheless, the fact that we could achieve V_{OC} values above 1 V is very promising and gives us hope that a PCE above 16% can be achieved provided that V_{OC} values above 1 V can be maintained together with FF values above 73% and J_{SC} values above 22 mA cm^{-2}. This could be a major breakthrough for Cu(In,Ga)S_2 solar cells.

Conclusions

The present work shows that by using a (Zn,Sn)O buffer layer deposited at temperatures of ~120 °C, interface V_{OC} deficit values on par with those of state-of-the-art Cu(In,Ga)Se_2 devices can be achieved. This breakthrough was achieved by using a lower buffer deposition temperature compared to our previous work, where 150 °C was used and a higher interface V_{OC} deficit was observed.[10] Our results also suggest that the buffer should be dense enough to protect against absorber degradation and sputter damage, which would otherwise lead to a higher interface V_{OC} deficit and low FF in the device. Even though the (Zn,Sn)O buffer layer deposited at temperatures of ~105 °C resulted in a certified device with PCE of 14%, the buffer process also led to a higher interface V_{OC} deficit. We speculated that this could have resulted from the low density of the (Zn,Sn)O buffer.

In addition to these results, we also found that the interface V_{OC} deficit is also dependent on the i-layer used in combination with the buffer, highlighting the importance of the i-layer in the device.

Overall, this work demonstrates that a low interface V_{OC} deficit and, consequently, a high V_{OC}, together with high PCE, can be achieved using Cu(In,Ga)S_2 solar cells with a low-temperature (Zn,Sn)O buffer and Al:ZnMgO i-layer.

Conflicts of interest

The authors declare that there is no conflict of interest.

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