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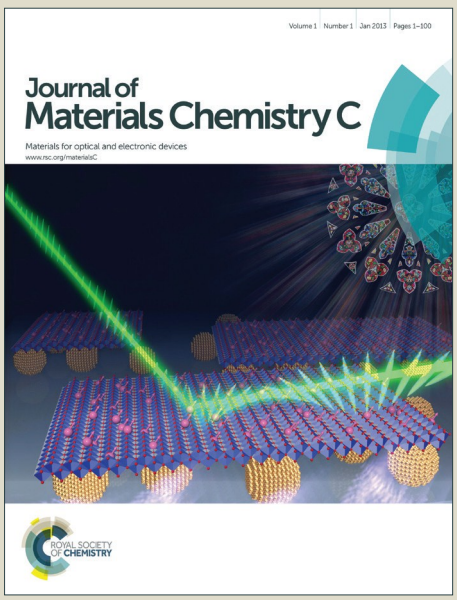

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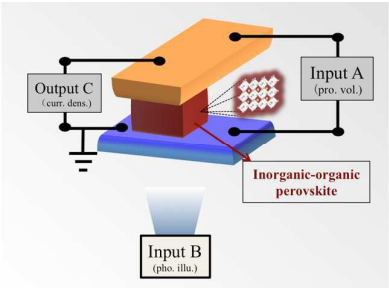

Electrically bistable and non-volatile rewritable memory effect on a sandwich architecture, ITO/PEDOT:PSS/organic-inorganic hybrid perovskite/Cu.

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ARTICLE

Organic-Inorganic Hybrid Perovskite Logic Gate for Better Computing

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A practicable mean for significantly reducing energy consumption and speeding up the operating rate of computer chips is placing processor and memory into one device, which processes and stores information simultaneously like human brain. Here we demonstrate that in novel sandwich architecture the organic-inorganic hybrid perovskite materials could be used as building-block materials of non-volatile memristor accompanying with photoresponsive performance. Owing to the distinct photo-response of two resistance states of memristor, it is feasible to drive the device as logic OR gate by employing electrical field and light illumination as input sources. This study provides a potential application in logic circuits, optical digital computation and optical quantum information for its beneficial supplement of von Neumann architecture or even going beyond it.

Memory and processor are key components of modern computer according to von Neumann architecture[1] described in 1945. Due to substantial latency of data shuttling between memory and processor, the closer of memory and processor becomes the better computing achieves.[2] The two-terminal resistance switching memory showing hysteretic current-voltage behavior was called memristor (short for memory resistor), [3-6] which has the ability to store and process information simultaneously when hybridized with complementary metal oxide semiconductor (CMOS) circuits.[7-9] This brings hope to make memory and processor integrate into one device that could go beyond von Neumann architecture. Meanwhile, to achieve the next generation optical digital computation or all-optical computer with massively parallel computing capability, low heating of junctions, high speed and high density, photon is highly recommended to be input source.[10] Recently, a new class of perovskite materials with organic-inorganic hybrid components is widely researched because it is one of the most competitive candidates as absorbing material for thin-film photovoltaic applications. It has certain advantages in flexibility, large-area film forming, fabricating convenience, and cheapness[11]. The energy conversion efficiencies reached confirmed value of 16.2% and unconfirmed value of 19.3% in photovoltaic cells from simple solution processes.[12] Moreover, due to the stunning exciton diffusion distance and strong photon absorbance coefficient, perovskite-material-based photodetectors[13,14] show excellent photoconductive performances. This star-material was also reported to have memristive property.[15,16] Memristors that exhibit hysteresis loops in *I-V* curve are mainly built from a simple conductor/semiconductor/conductor (CSC) thin film stack.[7] Central semiconductor materials are traditionally metal oxides,[17,18] chalcogenides[19] and organic films.[20-25] Perovskite material is commonly a kind of metal oxides with ABX_3 crystal type, showing rich and colourful physical properties.[26,27] The devices fabricated with perovskite oxide $SrRuO_3$[28], $SrTiO_3$[29] and $CH_3NH_3PbI_3$[16] have been reported to have memristive property with the ON/OFF current ratio of no more than four orders of magnitudes.

Because both the photoconductivity and the memristive effect have been observed in the same star-material, it offers us an opportunity of fabricating device with new function. Herein, a sandwich architecture, indium tin oxide (ITO)/poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS)/organic-inorganic hybrid perovskite/metal, was built. This device exhibited the function of memristor with ON/OFF ratio reaching about 10^4 at the read-out voltage of 50 mV, which is the best result of organic-inorganic hybrid perovskite based memristors. Additionally, it can achieve logic OR operation when light switched ON/OFF and electrical bias swept positive/negative. In one word, this device contains the function of electrically controlled memory and photo induced logic circuit (ECM & PILC) simultaneously. It has the potential of storing and processing information without data shuttling between memory and processor, making it a promising model for better computing that goes beyond von Neumann architecture.

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An organic-inorganic hybrid $CH_3NH_3PbI_3$ layer was fabricated by two-step solution process and sandwiched between PEDOT:PSS treated ITO substrate and copper (Cu) electrode described in experimental section. The UV-Vis absorption spectrum of the synthesized perovskite material proves that the material has strong photon-absorbing property with a broad range from ultraviolet to near-infrared (Figure S1a). The X-Ray diffraction (XRD) spectrum of the material indicated the formation of perovskites structure, and no impurity peak was identified from XRD patterns[13,14] (Figure S1b). The scanning electron microscopy (SEM) image of the perovskite layer shows the continuous and full coverage of $CH_3NH_3PbI_3$ thin film on ITO substrate (Figure S1c). The atomic force microscopy (AFM) image shows the root-mean-square (RMS) value of $CH_3NH_3PbI_3$ thin film is 9.73 nm, revealing the surface has a very low roughness (Figure S1d). All of these guarantee the respectable photoresponsive and memristive properties of the fabricated device.

A schematic diagram of the device is shown in Figure 1a, and this architecture can be further identified by cross-sectional SEM image (Figure S2). The bias was applied to the top Cu electrode, and the bottom ITO electrode was grounded. Energy diagram of the device is illustrated in Figure 1b. The lowest unoccupied molecular orbital (LUMO) and the highest occupied molecular orbital (HOMO) levels of $CH_3NH_3PbI_3$ are -3.9 and -5.4 eV, respectively. The Fermi level of ITO, PEDOT:PSS and Cu electrode is -4.7, -4.9 and -4.65 eV, respectively. The energy level difference of PEDOT:PSS/$CH_3NH_3PbI_3$ (HOMO) and $CH_3NH_3PbI_3$ (LUMO)/Cu were only 0.5 eV and 0.75 eV, respectively. Upon implementing a negative voltage to the Cu electrode, the relatively small energy level difference favors the charge injections.

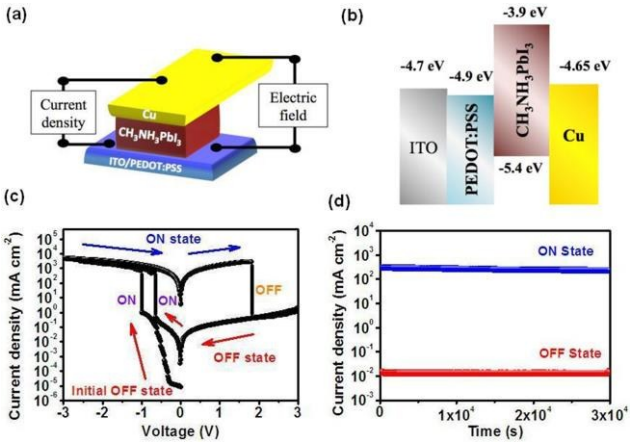

Fig. 1 Organic-Inorganic hybrid perovskite memristor. (a) Schematic structure of the hybrid perovskite memristor. (b) Energy diagram of the perovskite memristor. (c) Current-Voltage (*I-V*) characteristics of the memristor device. (d) Long-time response (i.e., retention times) of the ON and OFF state of the device, probed under a constant stress of -50 mV.

The *I-V* curve of the device with the structure of ITO/PEDOT:PSS/$CH_3NH_3PbI_3$/Cu shows the obvious features of electrical bistable and non-volatile rewritable memory effect (Figure 1c). In detail, when the voltage was swept from zero to a negative value (with ITO as the anode and Cu as the cathode), the current density firstly showed a tendency to increase slowly and the saltation process happened at about -1 V (resistance switching from initial high resistance state (HRS) to low resistance state (LRS)). After that, the voltage was swept from negative to positive value, and the current remained high until another saltation process of current (resistance switching from LRS to HRS) happened at around +2 V. The device was still at low-conductivity state during the following sweep process (from 2 V to 3 V, then to zero voltage). The resistance state was reversibly switched between LRS and HRS by sweeping the voltage repeatedly between negative and positive value. For the second sweep, the set voltage became -0.6 V and almost unchanged in the following cycles. The set process (resistance switching from HRS to LRS) occurred in the negative voltage region, whereas the reset process (resistance switching from LRS to HRS) happened at positive voltage region, coinciding with the bipolar type of resistance switching memory[30]. What should be emphasized here is the set/reset process occurs almost instantaneously in our device which is different from the results in literature[16], suggesting the mechanism is totally different. This process could also be expressed in Resistance-Voltage curve (Figure S3a). It shows obvious pinched hysteresis loop with instantaneous set/reset process. This phenomenon could not be achieved if the device was initially swept positively (with ITO as the cathode and Cu as the anode) from 0 to 5 V. The energy barrier of PEDOT:PSS/ $CH_3NH_3PbI_3$ (LUMO) is 1 V, electrons could not get sufficient energy to switch the device to the ON state if ITO/PEDOT:PSS was used as the cathode.

The retention performance of the ITO/ PEDOT:PSS/$CH_3NH_3PbI_3$/Cu device is shown in Figure 1d. With the constant "read" voltage, change of conducting state of the device is an important indicator for the device stability.[7,30] In this study, a constant "read" voltage (-50 mV) was imposed on the device at OFF or ON state, respectively. The currents were found to be stable with a high ON/OFF ratio of over 10^4 under the "read" voltage for a long time up to 3×10^4 s, which indicates that the device has good stability. The endurance characterization of the device was also carried out by iteratively sweeping the voltage between 3 V and -3 V (Figure S3b). After the aging, the device still remained the unchanged set/reset voltages and the resistance ratio kept at the magnitude of about 10^2. The "write–read–erase–read–rewrite" cycles could be reached 3000 times in this study. This indicates that the storage performance of ITO/ PEDOT:PSS/$CH_3NH_3PbI_3$/Cu cell is good and repeatable. Similar to other non-volatile memory, the ON and OFF state of our device can be retained after removing the power supply and rewritten for many times, suggesting the ITO/PEDOT:PSS/$CH_3NH_3PbI_3$/Cu sandwich device has potential application in non-volatile random access memory (NV-RAM).

Due to the outstanding photo-responsive effect of organic-inorganic hybrid perovskite material.[13,14] we characterized the photo-responsive performance of the device with the sandwich structure ITO/PEDOT:PSS/$CH_3NH_3PbI_3$/Cu under HRS state and LRS state, respectively. Figure 2a presents six cycles of the *I-t* response when the device stayed at HRS. The corresponding photocurrent was measured at 10 mV bias ("read" voltage) under solar simulator irradiation (100 mW cm^{-2}) switching ON/OFF for 8 /18 s. It can be seen that the current density of the device stayed at HRS could be converted from 10^{-6} to 10^{-3} mA cm^{-2}. The photo-responsive ON/OFF ratio of the device is more than 10^3, and the transfer is consistent

and repeatable. Figure 2b shows the *I-t* responses of the device at LRS, which were measured at a "read" voltage of 10 mV, 1 mV and 0.1 mV, respectively. The photocurrent is hardly distinguished from the dark current at each measurement bias. In other words, the device at LRS did not show obvious photoresponse.

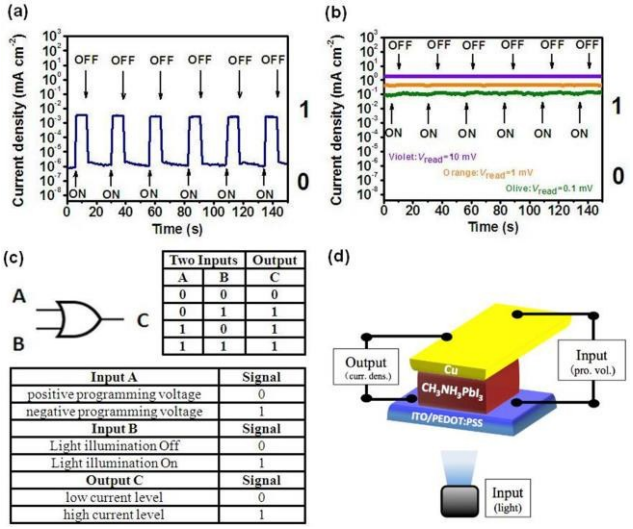

Figure 2 Photo-induced logic OR device. (a) *I-t* response of the device programmed to HRS under light ON/OFF switching irradiation with a read voltage of 10 mV. (b) *I-t* response of the device programmed to LRS under light ON/OFF switching irradiation with read voltages of 0.1, 1, or 10 mV, respectively. (c) State diagram of the logic OR device with two types of input sources and one output terminal. For input source A, which is the electrical field, signal "1" and "0" represent negative field and positive field, respectively. For input source B, which is light illumination, signal "0" and "1" represent light off and light on, respectively. (d) Schematic diagram of the light illumination induced logic OR gate.

Consequently, a photo-induced logic OR gate was designed as showed in Figure 2c (The input A and B are electric field and light illumination, respectively, and the output C is the current level). We could define the positive electric field as signal "0" and the negative electric field as signal "1" for input A; light off as signal "0" and light on as signal "1" for input B; the low current level as signal "0" and the high current level as signal "1" for output C. For this device, if one or both of the inputs was signal "1", the output was always signal "1" (high current level). On the contrary, only both of the inputs were signal "0", the output would be signal "0" (low current level). Thus, the device showed a capability of implementing logical disjunction like a logic OR gate. The information-flow in these gates can be further achieved by additional current-voltage converter.

To determine the origin of electric field-induced resistance switching behaviour of the perovskite memristor, the role of metal electrode was first explored. Cu atoms may migrate under the electric field to trigger the switching but a positive bias should be applied on Cu electrode (with Cu as the anode) before the migration of Cu atoms[31]. In our study, initial set process could not be achieved if the device was initially swept positively. A negative bias is initially applied on the Cu electrode to obtain a LRS, which is inconsistent with the model of migration of Cu atoms. In addition, no metallic filament can be formed in covalently bonded PbI_4^-. Thus, the Cu filamentary mechanism could be excluded. The CH_3NH_3I is quite stable. The filament of carbon could not be formed in the device of ITO/PEDOT:PSS/$CH_3NH_3PbI_3$/Cu. To decrease the possibility of chemical reaction at the interface of Cu/perovskite, we tested devices under the flow of N_2. The memory behavior did not show obviously difference. Then, the conduction mechanism was investigated with the ln(*I*)-ln(*V*) plots for HRS and LRS as depicted in Figure 3. The slope of the LRS curve is fixed, which means that LRS current is governed by Ohmic conduction. The slopes of the HRS curve in the high-electric-field and low-electric-field regions are 3.29 and 0.94, respectively, which suggests that the dominant conduction mechanisms of HRS were Frenkel-Poole emission in the high-electric-field region and Ohmic conduction in the low-electric-field region[30]. The linear fit of ln(*J*/*V*)-$V^{1/2}$ curve of HRS suggests that the electrical property was influenced by the barrier, which can be given by the expression,

$$R_c = A\exp(2aV^{\frac{1}{2}}/T - q\Phi_B/k_bT) \quad (1)$$

where R_c, A, k_b, q, a and T are resistense of interface, prefacter, Boltzmann constant, electronic charge, a positive constant and temperature, respectively, which are all unchanged. Thus，It could be inferred from expression (1) that R_c is basically dominated by the barrier height Φ_B. Therefore, the transformation of resistance between high and low was ascribed to the variation of barrier**.**

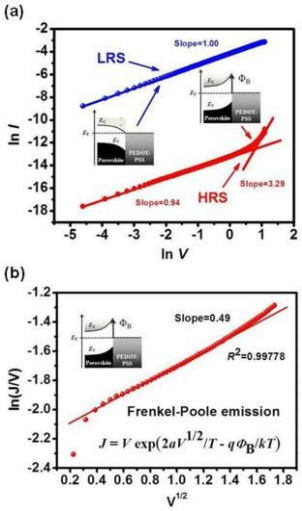

Fig. 3 Mechanism of the hybrid perovskite memristor. (a) ln(*J*)-ln(*V*) plots of the memristor in LRS and HRS. (b) ln(*J*/*V*)-ln(*V*) plots of the memristor in HRS (insets: Band diagrams of the $CH_3NH_3PbI_3$ memristor at OFF and ON states, taking into consideration of barriers at the PEDOT:PSS/perovskite contacts. E_c, E_v and E_f are the conduction band energy, valence band energy and Fermi level energy, respectively. Φ_B is the barrier height.)

An important issue is to confirm that the barrier is situated at PEDOT:PSS/perovskite or perovskite/Cu interface. Here we measured the *I-V* curves of Cu/$CH_3NH_3PbI_3$/Cu, Cu/$CH_3NH_3PbI_3$/Au, ITO/PEDOT:PSS/$CH_3NH_3PbI_3$/ITO and ITO/PEDOT:PSS/CH3NH3PbI3/Au structures for the control experiments (Figure S4). The Cu/$CH_3NH_3PbI_3$/Cu device kept at LRS，showing no memristive phenomenon, which means that no barrier existed in Cu/CH3NH3PbI3 interface (Figure S4a). Cu/$CH_3NH_3PbI_3$/Au device also showed no memristive phenomenon，which excluded the possibility that memristive behaviour was

generated by asymmetry electrode (Figure S4b). We tested the Cu/Cu and Cu/Au devices as the control device for metallic contact. The devices show much lower resistance than the devices of Cu/$CH_3NH_3PbI_3$/Cu and Cu/$CH_3NH_3PbI_3$/Au, which can exclude the metallic contact of the control devices of Cu/$CH_3NH_3PbI_3$/Cu and Cu/$CH_3NH_3PbI_3$/Au. To check the other interface, we measured the ITO/PEDOT:PSS/$CH_3NH_3PbI_3$/ITO device, and found memristive phenomenon still existed (Figure S4c). ITO/PEDOT:PSS/$CH_3NH_3PbI_3$/Au device was also explored, and the unipolar memristive behaviour was similar to the reference [16]. The energy level difference of $CH_3NH_3PbI_3$ (LUMO)/Au (Fermi level) was about 1.2 eV. Upon implementing a negative voltage to the Au electrode, the relatively high energy level difference may prevent the charge injections. Therefore, the device of ITO/PEDOT:PSS/$CH_3NH_3PbI_3$/Au show no sharp set/reset voltage. As the energy level difference of $CH_3NH_3PbI_3$ (LUMO)/Ag (Fermi level) was only 0.3~0.4 eV, the silver may react with $CH_3NH_3PbI_3$ under the condition of thermal-evaporate, thus the silver was not recommended. Consequently, we tend to ascribe the memristive phenomenon to the variation of a barrier on the PEDOT:PSS/$CH_3NH_3PbI_3$ interface, as showed in the insets of Figure 3.

The variation of barrier was ascribed to change of interface states induced by charge trapping at the metal/semiconductor interface[32]. The point defects near the surface of perovskite crystal could act as electron-trapping centers[33]. Similar to other solid, a finite concentration of point defects inevitably existed in $CH_3NH_3PbI_3$ at non-zero temperatures because of the configurational entropy. The density of defect states is in the order of 1×10^{17} to 1×10^{19} m^{-3} in the perovskite films deposited by solution process and thermal annealing[33]. Because of the densely packed crystal lattice of $CH_3NH_3PbI_3$ and other perovskite-type materials, the point defects might arrive from vacancies on any of three sublattices.

Consequently, the resistance switching behaviour could be explained by the modification of barrier, which was induced by the charge trapping of perovskite materials. A simplified charge-trapping model is showed in Figure 4. At the initial state the charges were equalized at each part of the device. Ascribe to the barrier on PEDOT:PSS/perovskite interface, the device showed HRS (Figure 4a). By applying a negative electric field (from ITO to Cu electrode), charges were injected from Cu cathode to perovskite material. The charge equilibrium of initial state was broken. The barrier subsequently vanished, leading to the formation of conducting path. Thus, the device showed up as LRS (Figure 4b). Owing to charge trapping ability of the perovskite film, even if the electric field was removed, charges were still trapped on perovskite material (LRS). After that, by applying positive electric field, the charges were extracted from the perovskite film, and the barrier between PEDOT:PSS/perovskite interface was reconstructed, which resulted in the HRS of device (Figure 4c). Removing the electric field, the barrier still existed, so that the resistance stayed at high state, and so forth.

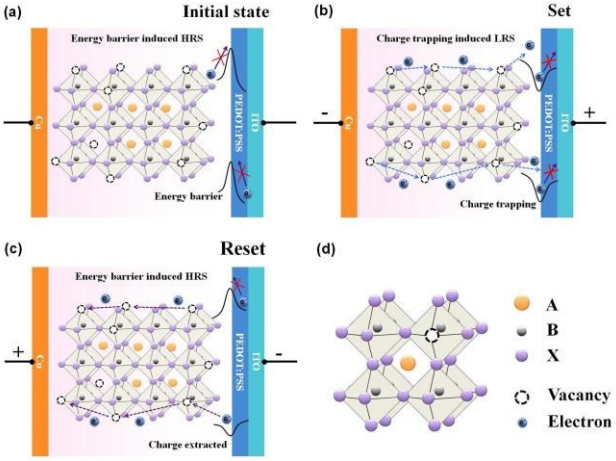

Fig. 4 Electron flowing and barrier switching under the external bias. (a) Initial HRS state of the device with the barrier on PEDOT:PSS/perovskite interface. (b) Applying a negative electric field. (c) Applying a positive electric field. (d) Perovskite crystal structure of $CH_3NH_3PbI_3$. A, B and X stand for CH_3NH_3, Pb and I, respectively.

Two other hybrid perovskite materials were further explored. We choose $CH_3NH_3PbI_{3-x}Cl_x$ for its excellent ultra-long carrier diffusion distance[34] and $CH_3NH_3Pb_{0.5}Sn_{0.5}I_3$ for its near-infrared absorption property[15] as representative perovskite materials, respectively. XRD spectra show that these two materials were successfully synthesized (Figure S5). The memristive phenomenon also exists in both ITO/PEDOT:PSS/$CH_3NH_3PbI_{3-x}Cl_x$/Cu and ITO/PEDOT:PSS/$CH_3NH_3Pb_{0.5}Sn_{0.5}I_3$/Cu devices (Figure S6). This proves that by altering the constituent of perovskite materials, the set or reset voltages, on/off ratio, *etc.* could be tuned.

To understand the mechanism of photoresponsive phenomenon when the device stays at different resistance states (LRS and HRS), the photogain factor G is considered, which is defined by[35,36]

$$G = \frac{\tau_c}{\tau_t} \quad (2)$$

where τ_c is the lifetime of the photogenerated carriers, and τ_t is the time required for the carriers drifting from one electrode to another. This formula can be further change-formed into[34] (For brevity, the derivation described in reference [34] is not repeated here again.)

$$G = \frac{\tau_c \mu V}{l^2} \quad (3)$$

where μ, V and l are the carrier mobility of the material, voltage applied on the device and the distance of electrode pair, respectively. Note that in the photoconductive measurement, τ_c and μ are the intrinsic properties of the perovskite materials (Because the memristive phenomenon is due to the change of contact type on perovskite/PEDOT:PSS surface, no matter when the device is at HRS or LRS, τ_c and μ of the perovskite in bluk phase will not change), and V is kept constant to the "read" voltage. Electrode distance l is also stationary both in the programming process and the photoconductive measurement. Thus, when the device is under

light illumination, the photogain is the same no matter the device is programmed to be ON state or OFF state.

On the other hand, the photogain factor *G* reveals how many carriers generated *per photon* absorbed in the device[36],

$$G = (\frac{I_{\mathrm{ph}}/\, q}{P_{\mathrm{in}}/hv}) \times 100\% \qquad (4)$$

where I_{ph} is the photo-generated current, and P_{in} is the power of the incident light beam with frequency *v*. The electronic charge *q* and Planck's constant *h* are both constants. When the device is under light radiation, P_{in} stays at 100 mW cm^{-2}. Thus, the I_{ph}, which was determined by the difference between photocurrent and dark-current (I_{ph}=I_{photo}-I_{dark}), will also be equal due to the equal photogain in both ON state and OFF state proved in preamble.

If the device is programmed to be OFF state before photoconductive measurement, the dark current will stay at a low level. When photon radiates, the photo-generated current I_{ph} will produce orders of magnitude difference between photo-current and dark-current, as showed in Figure 2a. Thus, the device output high current level or signal "1" in the logic OR device when light illuminates and low current level or signal "0" when absence of photon illumination. Conversely, if the device is programmed to be ON state before photoconductive measurement, the dark current will stay at a high level. The same *G* or I_{ph} value generated by photon illumination will not produce obvious difference between photo-current and dark-current, making the device output high current level or signal "1" in the logic OR device.

Conclusions

In summary, we built a sandwich architecture, ITO/PEDOT:PSS/organic-inorganic hybrid perovskite/Cu, which contains the function of ECM and PILC simultaneously. It exhibited excellent electrically bistable and non-volatile rewritable memory effect with outstanding ON/OFF ratio (10^4) at the read-out voltage of 50 mV, long retention time up to 3×10^4 s and 3000 times endurance cycles at least. The charge trapping on the point defects of the materials varied the barrier on the PEDOT:PSS/$CH_3NH_3PbI_3$ interface. Additionally, it showed different photoresponse when the device stayed at different resistance states (LRS and HRS). The photo-responsive ON/OFF ratio of the device at HRS is more than 10^3, and the transfer is consistent and repeatable, but the photocurrent is hardly distinguished from the dark current at LRS. These entire phenomena have been attributed to the special structure of the new organic-inorganic hybrid perovskite. The combination of electrical programming and photo-regulation achieve logic OR operation successfully for better computing.

Acknowledgements

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