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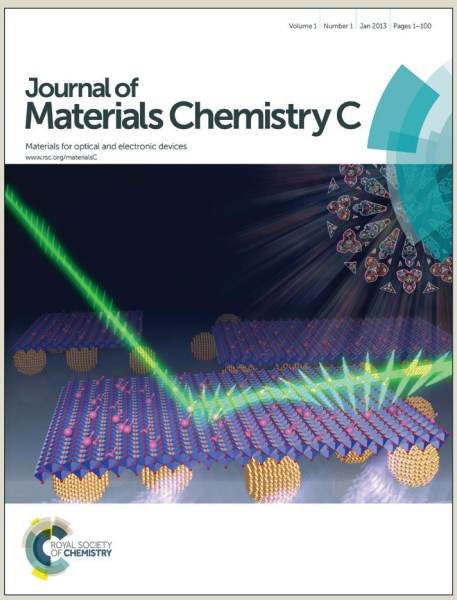

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Gold nanoparticle density-multiplication by tuning block copolymer self-assembly processes toward increased charge storage

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We describe a simple and versatile approach for enhanced nanoparticle density multiplication through block copolymer self-assembly technique for application in memory devices. Templates of block copolymers with functional groups directed the selective electrostatic self-assembly of the pre-formed gold nanoparticles to form gold nanoclusters arrays. By simply increasing the density of the polymer templates by manipulating the spin coating conditions, a lateral increase in the nanoparticle density is observed. The significance of the particle density multiplication was best observed when they were used as charge storage centers in flash memories. Minimization of the pitch (or maximization of the template density) resulted in a maximum memory window of about 1.63 V, with a charge trap state density of 4.93×10^{11} cm^{-2} in the gold nanocluster arrays. The reported approach offers exciting opportunities to fabricate multicomponent nanostructure-based memory devices tailored for enhanced memory performance. In addition, the nanoparticle density can be increased significantly further when combined systematically with the hierarchical block copolymer self-assembly approach.

1. Introduction

Nanoparticles have been of significant importance in micro-nano-technology. By virtue of their physical, electronic and optical properties, nanoparticles of different size, structure, shape and material composition find application in electronics,[1, 2] sensing,[3, 4] photovoltaics,[5] catalysis,[6] plasmonics[7-9] and in environmental applications.[6, 10, 11] Methods to fabricate nanoparticle superlattices within polymer matrix and their possible integration into functional devices are also common.[12] Of the many research areas where nanoparticles find utility, fabrication of memory devices has been extensively studied towards device miniaturization. Memory devices made of metal, metal-oxide and semiconductor nanoparticles attract widespread interest due to their simple device architecture and their potential for fabricating 3D stacks of the memory cells for enhanced bit densities, in contrast to the conventional continuous floating gate memory devices of the silicon-oxide-nitride-oxide-silicon (SONOS) kind.[13-16] The key metric for a memory device is the enhanced charge storage capability that defines its merit. With memory devices getting miniaturized, the memory performance relies on how best the device architecture can deliver enhanced charge storage within the constraint of the stringent norms imposed by continuous scaling down of device dimensions.[17]

One way of improving the charge storage density is to increase the charge storage centers or simply, the nanoparticle density. At the same time, increase in the nanoparticle density must also comply with the increasing demands towards scaling down device dimensions by increasing the nanoparticles foot print. This far, nanoparticle assembling methods based on as layer-by-layer (L-b-L) technique,[18, 19] block copolymer (BCP) self-assembly,[20, 21] Langmuir-Blodgett (LB) deposition,[22] thermal evaporation and annealing[23] have been reported. However, thin films that encapsulate nanoparticles formed by LB deposition are fragile due to the weak van der Waal's forces and eventually break down over time. Deposition by metal evaporation followed by annealing results not only in uncontrolled nanoparticle size but also introduces uneven distribution in the amount of charges that is stored in each of the de-wetted metal features. On the other hand, with the L-b-L technique, an increase in the nanoparticle density is accompanied by increasing number of layers and thereby contributes to increase in the floating gate thickness. It is thus, clear that a trade-off between the nanoparticle density multiplication and quality of the nanoparticle assembling techniques posts a serious challenge. Hence, the need to develop a fabrication route that provides nanoparticle density

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multiplication laterally with a high degree of control over the process and device dimensions becomes imperative.

Employing polymeric surfaces in assembling nanoparticles is of utmost interest since the polymeric surfaces provide the necessary functional groups for binding of nanoparticles with ease.[24] Some of the common techniques to assemble nanoparticles using polymers are encapsulation within polymer matrix,[18, 25] AuNP–thiol covalent binding,[26, 27] block copolymer self -assembly[21, 28] and utilizing electrostatic interactions.[21, 29, 30] Nanoparticle assemblies based on block copolymer self-organization draws significant attention since they provide opportunities to selectively direct the attachment of particles to form cluster arrays of nanoparticles. Furthermore, block copolymers offer polymer templates that have definite geometry and are produced in a simple and cost effective fashion. The long-range lateral ordering of block copolymer domains guided by the inherent defective patterns in the underlying substrate that increases the feature density many-fold was recently reported.[20] In another instance, the diblock copolymer domains self-assembled on Angstrom-smooth surfaces were chosen to be the guiding templates to prepare nanoparticle assemblies with different pitch and separation.[31, 32] Such nano-patterns achieved either by the substrate- or the template-guided approaches[28] offer versatility in extending the range of possibilities and opportunities to realize directed self-assembly and feature density multiplication that are not easily obtained by other conventional techniques.

In a recent report, we have demonstrated charge storage enhancement by increasing the nanoparticle density through hierarchical assemblies based on block copolymer self-organization.[33] Application of in-situ gold nanoarrays generated using BCP towards flash memory device applications were also reported.[34] In this work, by simply varying the self-assembly process conditions, we demonstrate a cost-effective BCP template-guided approach to provide nanoparticle density multiplication that not only offers lateral coverage but also the increase in the nanoparticle density that translates into increase in the charge storage capacity as demonstrated by the C-V measurements.

2. Experimental

2.a. Material

p-type silicon wafers with thermally grown silicon oxide were obtained from Globalfoundries Singapore Pte Ltd, Singapore. 2-propanol and *m*-xylene were obtained as anhydrous solvents with purity > 99 % from Sigma-Aldrich Pte Ltd. Sodium citrate (Sigma) and Hydrogen tetrachloroaurate (III) trihydrate ($HAuCl_4.3H_2O$) (99.9%, Aldrich) were used as received. Polystyrene-*block*-poly(2-vinylpyridine) (PS-*b*-PVP) (Mw = 248,000-*b*-195,000 g mol-1, PDI = 1.1) was purchased from Polymer Source Inc, Canada. Point Probe Plus silicon tips for imaging in tapping mode with atomic force microscopy were purchased from Nanosensors (Neuchatel, Switzerland).

2.b. Method

The silicon substrates were diced into chips of size 10mm x 10mm. They were cleaned by in acetone and 2-propanol for 15 min and finally treated with UV/Ozone (SAMCO UV-1, SAMCO Inc., Kyoto, Japan) for 10 minutes. The thickness of the tunnel oxide layer was measured using an ellipsometer (Wvase 32, J.A.Woollam.Co., Inc., Lincoln, USA). The array of Au nanoparticles (AuNPs) was fabricated as described elsewhere.[21] In short, reverse micelle of PS-*b*-PVP of 0.5 % (w/w) concentration in *m*-xylene were self-assembled on the Si surface by spin-coating to yield periodicities of 200 nm, 182 nm and 167 nm. This was followed by immersion of the substrates in aqueous suspension of citrate ion stabilized pre-synthesized AuNPs for 2 hours in order to direct the electrostatic self-assembly of the negatively charged AuNPs on to the positively charged pyridyl units of the reverse micelles. The copolymer template was then removed by exposing them to O_2 plasma reactive ion etch (RIE) (Oxford plasmalab 100, Oxfordshire, UK) for 10 min (at 30 W, 65 mTorr, 20 sccm O_2) to complete the nanocluster array fabrication. The stable colloidal Au NPs were synthesized according to a procedure reported in the literature.[35] Briefly, in a round-bottom flask fitted with a reflux condenser, 30 mL of 1 mM $HAuCl_4$ was boiled with stirring. Later, 6 mL of 38.8 mM sodium citrate was added to the boiling solution and during the course of reduction, the color of the solution turned from black to purple to wine-red. The solution was then cooled before performing experiments. The pattern geometry such as the mean heights, width, periodicity and inter-feature spacing of the reverse micelle arrays were characterized using tapping mode AFM (Dimension Icon, Bruker Corporation, CA, USA). The plan view and cross-sectional view of the gold nanoparticle cluster arrays were obtained using transmission electron microscopy performed using Philips CM300 TEM operating at 300 kV. In short, the samples were first deposited with ~100nm thick SiO_2 using e-beam deposition at room temperature. For cross-sectional TEM imaging, two pieces (3 mm x 1 mm each) were cut from the same sample and their top surfaces were bonded with epoxy glue and cured. The samples were then mechanically polished with SiC lapping film down to ~40µm thickness. Dimple grinding and ion milling were then carried out to further thin down the sample thickness until they were electron transparent. For planar TEM imaging, the processes involving polishing, dimpling and ion milling were performed from the bottom side of the substrate. The SiO_2 control oxide was deposited using a SiO_2 target (99.995 % pure) with a copper backing plate in unbalanced magnetron (UBM) sputtering system (Nanofilm Technologies International Pte. Ltd., Singapore). The variation in film uniformity was typically <5 %. The deposition was carried out at a chamber base pressure of < 10^{-6} Torr. Subsequently, 120 nm thick gold top-electrodes were deposited through a metal stencil mask of 0.3 mm diameter and spacing of 1 mm. The

electrode deposition was carried out using an electron beam evaporator (Denton Vacuum Explorer Coating System, NJ, USA). 500 nm of Gold back-electrode was sputtered on the backside of the silicon substrate after stripping the native oxide using sandpaper. The C-V characterization was performed using the HP4284A precision LCR meter (Hewlett-Packard, USA) under a measurement frequency of 1MHz. C-t measurements were performed using the same instrument by monitoring the capacitance as a function of time at the VFB.

3. Results and discussion

3.a. Gold nanoparticle density-multiplication by tuning self-assembly of BCP templates

Figure 1 illustrates the process of constructing gold nanocluster arrays. The gold nanocluster arrays were fabricated adapting a self-assembly process that was recently reported.[21, 36] The methodology utilizes the polymeric features in the templates to direct the electrostatic self-assembly of the gold nanoparticles in the following step. Polymer templates with different periodicities of 200 nm, 182 nm and 167 nm (Figure 2) were obtained by varying the spin speeds for coating PS-*b*-PVP reverse micelles on the surface. PVP formed the core while PS formed the continuous layer. These polymer features served as the templates in guiding the electro-static self-assembly of negatively charged pre-synthesized gold nanoparticles. Since, the protonated pyridyl units of PVP exhibited positive charge, the electrostatic attraction of the citrate-stabilized gold nanoparticles resulted in selective deposition of AuNPs, thereby forming AuNP cluster arrays - AuNP-200, AuNP-182 and AuNP-167 (where 200, 182 and 167 denote the pitch of the respective nanocluster array) (Figure 2). The pre-synthesized citrate-stabilized AuNPs exhibited a diameter of ~11.3 nm as shown in the inset of Figure 3 (a). Following the selective deposition of the AuNPs on to the polymer features, the underlying polymeric template was removed by oxygen plasma etch for 10 min.

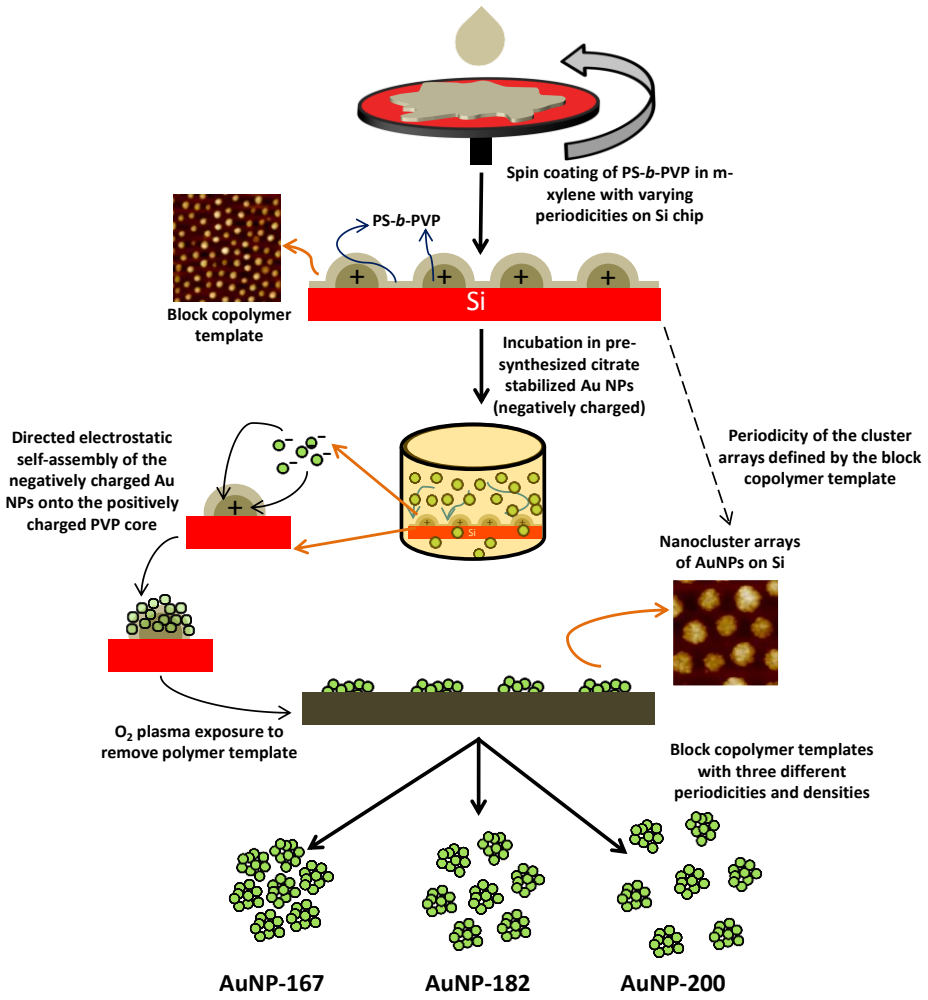

Figure 1. Scheme illustrating the process of obtaining the gold nanocluster arrays namely, AuNP-200, AuNP-182 and AuNP-167 of different periodicities through electrostatic self-assembly of citrate-stabilized gold nanoparticles on to the features of the polymeric template obtained through self-assembly of reverse micelles of PS-*b*-PVP. Following this, the polymeric template was removed by an oxygen reactive ion etch. The AFM images in the schematic shows the self-assembled polymer template and the electrostatically self-assembled gold nano arrays.

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The PVP core of the template with diameter of ~120 nm (±12 nm) can be visualized to form hemispherical polymeric features on the surface of the substrate upon spin coating. It has earlier been reported that the gold nanoparticles of similar size within the same cluster exhibit an inter-particle distance of ~4.2 nm.[36] Thus, for the given foot-print, the number of gold nanoparticles that occupy every polymer feature of the template determined by the latter's surface area (estimated using AFM results) can be estimated to be ~94.[21] Considering a substrate area of 1 cm^2, in the case of AuNP-167 arrays with the highest polymer feature density, the total surface area offered by the polymer templates with functionalities toward selective gold nanoparticle intake is ~0.7 cm^2. This allows packing of 2.82E+11 AuNPs in the form of clusters. However, the density of the polymeric arrays controlled through systematic variation in periodicity, will see an increase in nanoparticle density in the arrays with smaller pitch. The nanoparticle densities for the gold nanocluster arrays AuNP-200, AuNP-182 and AuNP-167 can be calculated to be 1.88E+11 per cm^2, 2.35E+11 per cm^2 (1.25 times AuNP-200) and 2.82E+11 per cm^2 (1.5 times AuNP-200) respectively. While the results establish a definite trend in the particle density enhancement with the increase in density of the polymer templates, each of the nanocluster arrays exhibits a tolerable error in the density as a result of standard deviation (~5%) in the separation of polymer features characteristic to the block copolymer self-assembly process.[21, 37] Thus, an extension of the particle density multiplication process obtained by tuning the pitch of the templates will aim at filling up the voids between the arrays with nanoparticle clusters of smaller sizes through a systematic hierarchical self-assembly approach.[21]

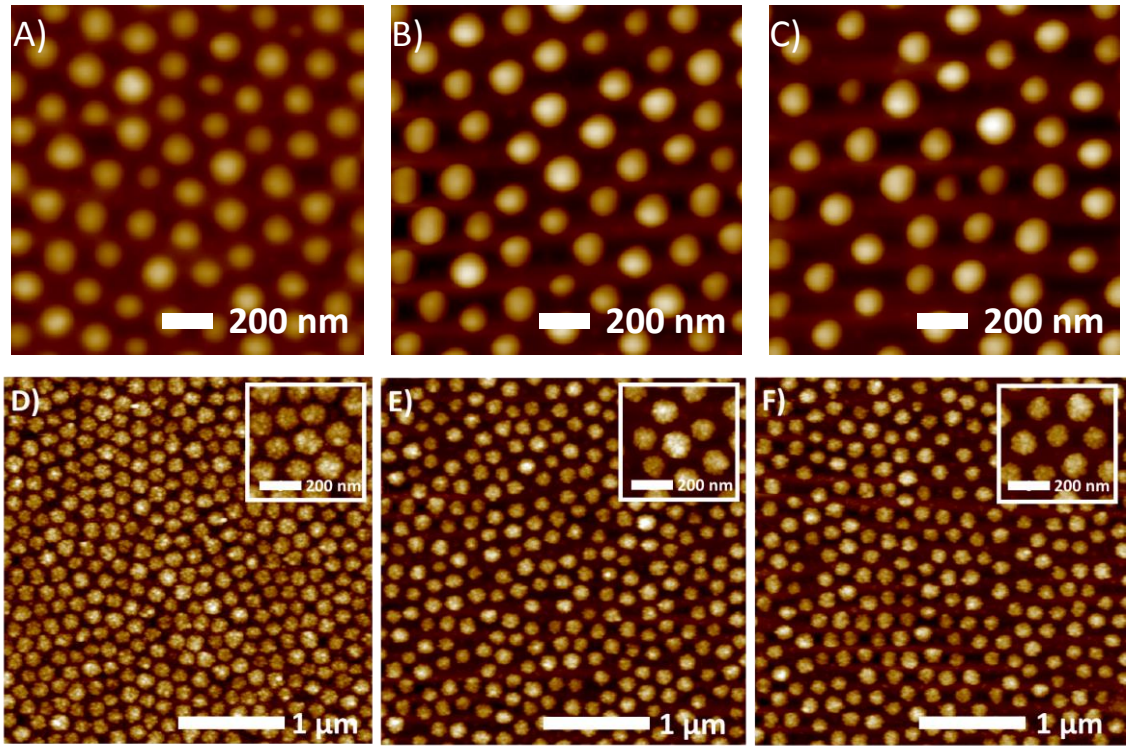

Figure 2. Reverse micelles of PS-*b*-PVP self-assembled onto the surface of Si chip forming the polymer template exhibiting a pitch of **A)** 167 nm, **B)** 182 nm and **C)** 200 nm. Gold nanocluster arrays **(D, E and F)** obtained after the directed electrostatic self-assembly of the citrate-stabilized pre-synthesized gold nanoparticles onto the polymer features of the templates as shown in **(A, B and C)** respectively. Inset shows the magnified image of the gold nanocluster arrays.

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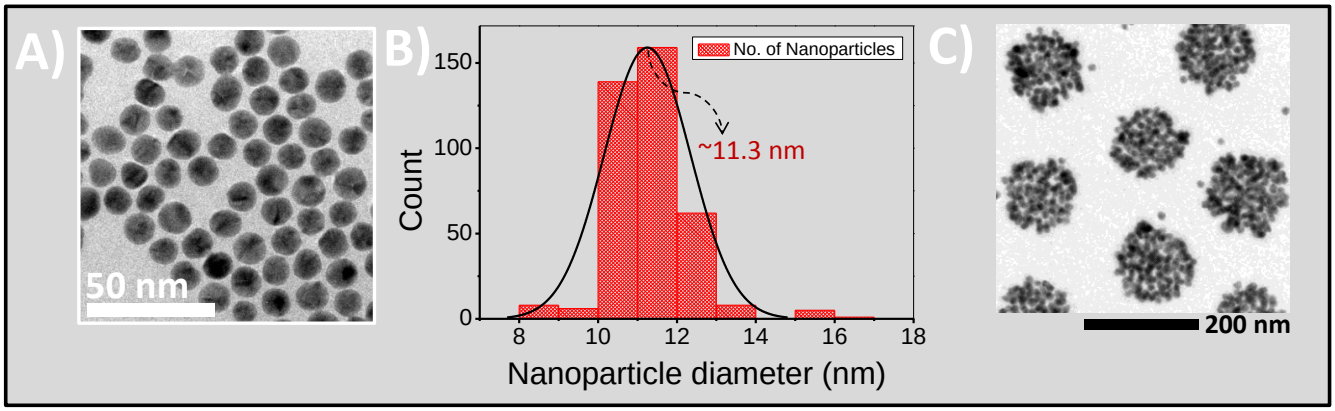

Figure 3. A) TEM image of the pre-synthesized citrate stabilized AuNP with **B)** histogram representing the size distribution in the nanoparticles with the mean particle size of 11.3 nm. **C)** Plan-view TEM of the AuNP-200 arrays showing the selective adsorption of the gold nanoparticles on the periodic polymer features comprising the array.

3.b. Gold nanoarrays-MIS device characteristics

The enhanced nanoparticle density and their significance in electronic devices was studied by investigating their charge storage and retention performance by incorporating them within a metal-insulator-semiconductor (MIS) capacitor device constructed as a Au/*p*-Si/SiO_2/Gold nanocluster arrays/SiO_2 (50nm)/Au stack structure **(Figure 4)**. Briefly, the gold nanocluster arrays were fabricated on *p*-Si substrates consisting of a 3 nm thick thermally grown tunnelling oxide. The control oxide comprised of 50 nm of silicon dioxide deposited by radio frequency sputtering completely covering the nanoparticle assemblies (TEM and STEM image in **Figure 4**) preventing any shorting with the top electrode. The substrates were annealed following the control oxide deposition. Au was deposited as top and bottom electrodes (*cf*. Methods section for electrode fabrication details).

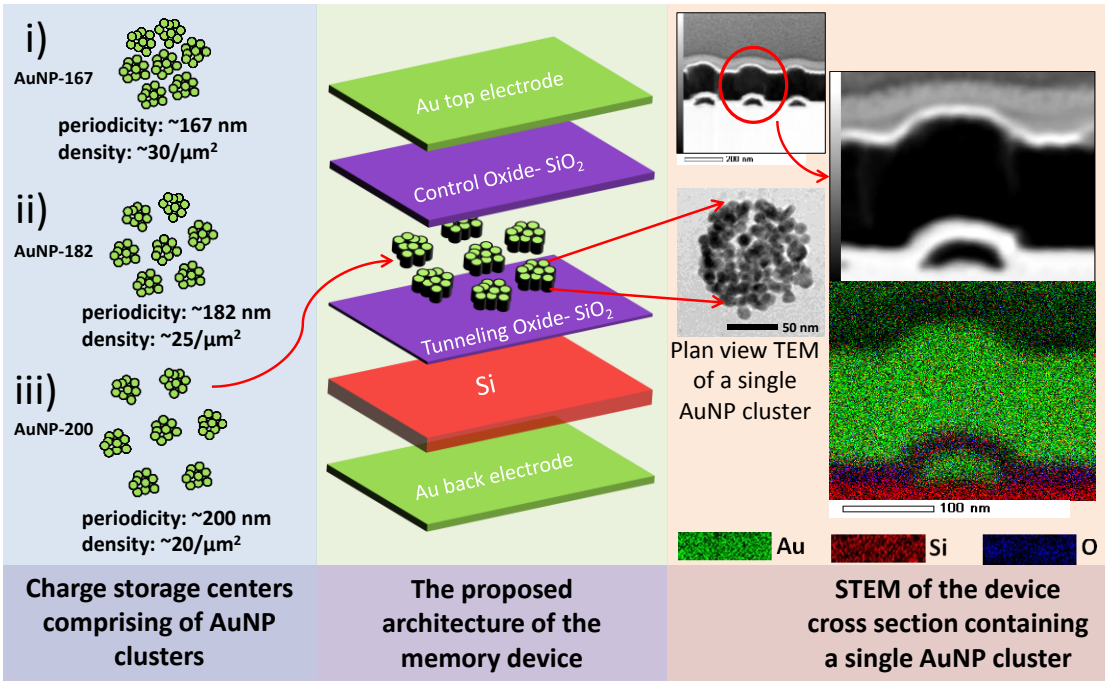

Figure 4. Schematic showing the device architecture that comprises of the gold nanocluster arrays **i)** AuNP-167 , **ii)** AuNP-182 and **iii)** AuNP-200. The STEM shows the composition of the device with green representing Au, violet representing O and red representing Si (*ref Figure S1 of the supporting info for a detailed STEM analysis*). The cross-section TEM of the device also shows that the control oxide offers a good cover preventing any shorting between the gold nanocluster arrays and the top electrode.

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3.c. Capacitance-Voltage (C-V) and Capacitance-time (C-t) characteristics

The hysteresis curves or the memory windows of the MIS memory device comprising the gold nanocluster arrays with different nanoparticle densities are shown in **Figure 5**. The gate was biased with the voltage sweep of ±4V. As the applied bias voltage was swept more towards negative potential, a counter-clockwise hysteresis was observed which shows that the charge storage centers (CSCs) are loaded with net positive charge owing to hole trapping from the substrate accumulation layer into the gold nanocluster arrays.[38] The devices comprising of AuNP-200, AuNP-182 and AuNP-167 exhibited a memory window of 0.98 V, 1.31 V and 1.63 V respectively for the nanoparticle densities of 1.88E+11 per cm^2, 2.35E+11 per cm^2 and 2.82E+11 per cm^2.

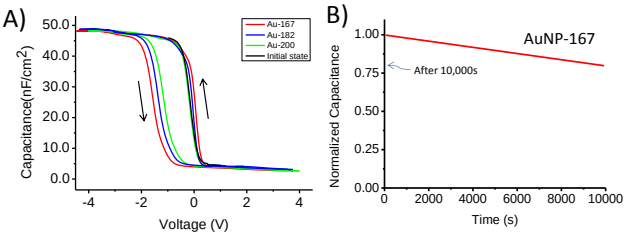

Figure 5. A) C-V characteristics of the gold nanocluster arrays AuNP-167, AuNP-182 and AuNP-200 exhibiting a counter clockwise hysteresis. Asn increase in the shift in the memory window is observed with increase in the nanoparticle density of the gold nanocluster arrays that comprise the charge storage centers. **B)** The retention characteristics of the gold nanocluster arrays with the highest nanoparticle density (AuNP-167) shows that over 75% of the charge is retained after discharging the device for 10,000s *(ref Figure S2 of the supporting info for Ct of AuNP-182 and AuNP-200 devices).*

For a quantitative explanation for the observed hysteresis behavior, the following equation was used to estimate the charge trap state densities:[39] Q = (C*VFB)/(qA), where C is the capacitance of the dielectric stack layer, VFB is the flat band voltage shift, q is the charge of an electron and A is the area of the electrode. Thus, the charge trap state densities calculated for the MIS device comprising of AuNP-200, AuNP-182 and AuNP-167 are ~3E+11 cm^{-2}, ~4E+11 cm^{-2} and ~5E+11 cm^{-2} respectively, increasing significantly with increase in nanoparticle density . The values remain largely unaffected due to the error in the density of the template features. Thus, it is clear that, with the lateral increase in the nanoparticle density, the density of charge trap states also increases and thereby an enhancement in the charge storage is observed.

The MIS device with the largest memory window (AuNP-167) was tested for the Capacitance-time characteristics in order to assess the charge decay after charging the device at VG of -4 V for 30 s. A voltage equal to the flatband voltage (VFB = -0.04 V) was applied to the top electrode for 10,000 s with the back electrode grounded. The C-t characteristics in Figure 5B show that over 75 % of the injected charges were retained after 10,000 s. Previous reports on the retention behavior of the nanoparticle based memory devices suggest that the devices are affected through lateral charge conduction.[40, 41] However, with the devices comprising the gold nanocluster arrays described in this work, any lateral charge conduction is highly inhibited due to the discrete arrangement of the arrays and thereby mitigates charge leakage to the Si substrate.

In an earlier work, we reported the assembly of gold nanoparticles in a hierarchical fashion in order to enhance the particle density footprint.[33] The results showed good improvements in charge storage capacity due to increase in particle density. While the increase in the memory window was significant, the number of charges stored per nanoparticle decreased after the second level of hierarchy, possibly due to the heavy screening of freshly injected charges by the charges that are already stored in the charge storage centers. In an attempt to address the screening effect, particle density multiplication performed by increasing the density of the BCP templates as an alternate to building layer-by-layer assemblies not only allowed increasing the particle density laterally, but also prevented the undesirable addition to the height of the device structure. Patterning the nanoparticles by tuning the density of the block copolymers offers an additional advantage in suppressing any leakage due to lateral conduction despite lateral increase in the particle density due to clustered nature of the assemblies. Thus, any conceivable charge leakage due to pin-hole defects in the tunneling oxide layer will have effect only on the affected cluster while other clusters of gold nanoparticles will retain the stored charges, thus minimizing the overall charge leakage.

Figure 6 schematically describes a continuous floating gate memory and clustered nanocrystal memory in a scenario when the tunneling oxide offers a pin-hole leakage path thereby draining the stored charges. In order to significantly bring out the importance of having nano clusters in the device architectures, it is fair to make an assumption that all injected charges are stored only in the continuous floating gate or in nanoclusters for the respective devices. The AuNP cluster arrangement achieved by simply tuning the density of the self-assembled template becomes distinctively advantageous when

the device performance is compared to any of the other conventional SONOS based devices where the floating gate is a continuous thin film.[42, 43] The latter is vulnerable to heavy charge leakage through the tunnel oxide that almost leaves the floating gate empty. However, such a consequence is not observed in the cluster of nanoparticles that are built on ITRS17 specified tunneling oxide thickness of 3 nm made of thermally grown silicon oxide. Thus, the device architecture combines the dual advantage of using an ultrathin thermally-grown silicon oxide that do not offer any leakage path and the engineered clusters of gold nanoparticles that are not susceptible to an avalanche of charge leakage if one of the many clusters would leak.

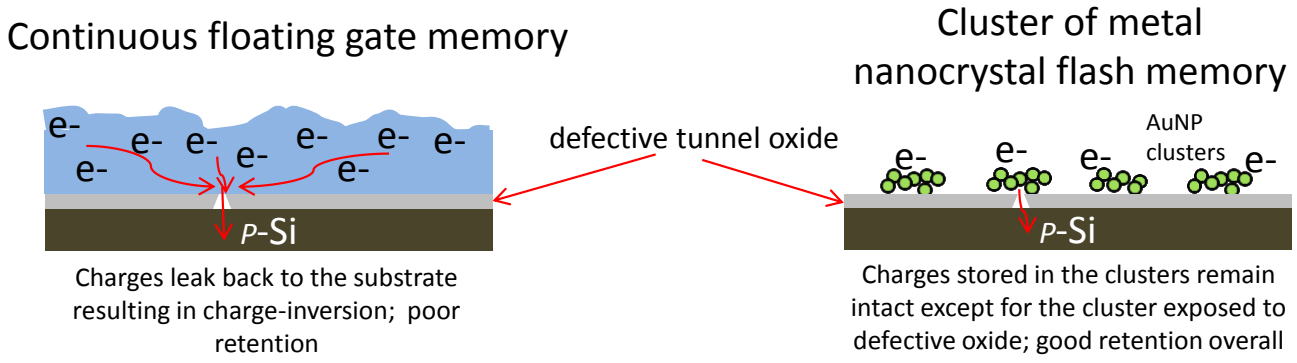

Figure 6. Schematic explaining the mechanism involved in the leakage of stored charges via a pin-hole defect in the tunnel oxide layer in the (left) conventional continuous floating gate memory devices and (right) nanocluster arrays. By virtue of their charge trapping behavior that involve charge hopping and trapping in the continuous shallow traps, all stored charges leak with a minute pin-hole defect. On the other hand, with the nanocluster arrays, only the charges stored in that cluster that is affected by the defective tunnel oxide would leak.

4. Conclusions

We have demonstrated that a simple tuning of the BCP self-assembly process creates surfaces with increased particle density suitable for applications in memory devices. The electrostatically directed self-assembly of gold nanoparticles offers a lateral ordering in the nanocluster arrays with high particle densities which is not readily attainable through other lithography techniques. This patterning of nanoparticle assemblies relying on simple tuning of the self-assembly processes extends opportunities to realize diverse cluster size, cluster-to-cluster distance, particle-to-particle distance, and other significant feature characteristics. BCP comprising of polymer chains of different molecular weights will add to the versatility of the process by offering polymer features in the sub-10nm regime towards realizing densities at the Terabit scale. The approach surpasses the simple layer-additive characteristics of conventional nanoparticle-assembly techniques by offering templates with functionalities toward wide range of other anionic nanoparticles and hold great promise for various other applications in metamaterials, plasmonics and photonics where the size, shape and geometry for the nanoparticle arrays are key performance indicators.

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Gold nanoparticle density-multiplication by tuning block copolymer self-assembly processes toward increased charge storage

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Enhanced charge storage in flash memories using AuNPs as charge storage centers enabled through block copolymer self -assembly process