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ARTICLE

Ultra Low Density of Interfacial Traps with mixed Thermal and Plasma Enhanced ALD of High-κ Gate Dielectrics

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Anomalous growth per cycle was observed using *in-situ* ellipsometry during the initial cycles of plasma enhanced atomic layer deposition (ALD) of high-κ dielectrics, while thermal atomic layer deposition of these oxides exhibited linear growth per cycle. The anomalous growth per cycle was attributed to oxidation of the substrate by plasma oxygen. Thermally grown films have lower capacitance density and higher leakage current but lower density of interfacial traps compared to plasma enhanced grown films. For plasma enhanced films, the leakage current is dominated by direct tunnelling while trap assisted tunnelling seems to be dominant in thermal grown films. Initiating the oxide growth with thermal atomic layer deposition and then switching to the plasma enhanced process protects the substrate surface from plasma oxygen and lowers the density of interfacial traps (D_{it}). Starting with ten cycles of thermal atomic layer deposition of ZrO_2 enhances the capacitance density while decreasing the D_{it}. The lowest value of D_{it} was obtained with twenty cycles of thermal atomic layer deposition ($1.8x10^{10}$ cm^{-2} eV^{-1}). The mid-gap D_{it} reduces systematically with increasing number of thermal ALD cycles. Furthermore, the frequency dispersion in accumulation is reduced with increasing number of thermal ALD cycles up to twenty.

Introduction:

Deposited oxide thin films are used in many advanced electronic applications such as logic and memory devices, III-V power and high frequency devices, optoelectronics, tunnel junctions, and spintronics [1–5]. Many of these devices rely on a metal-oxide-semiconductor structure (MOS) and a well-defined and atomically abrupt oxide-semiconductor interface without any interfacial substrate oxide, which degrades performance of this structure [6,7]. However, the ultra-low density of interfacial traps (D_{it}~ 10^{10} cm^{-2} eV^{-1}) found at the Si/SiO_2 interface is difficult to achieve at the deposited high-κ dielectric/Si interface mainly due to large differences in the atomic crystal coordinates of silicon and high-κ oxides [8,9]. The semiconductor-gate dielectric interface is one of the most crucial regions of a MOS device [8,10].

Deposited high-κ oxide thin films replaced thermally grown SiO_2 in silicon MOS devices due to scaling issues with SiO_2 as a gate dielectric[7,11]. For III-V compound devices, where there are no good quality semiconductor native oxides, a deposited gate oxide is the only option[12]. Oxide thin films have been deposited by variety of physical vapour and chemical vapour deposition techniques[13–15]. Atomic layer deposition (ALD) uses organometallic precursors as the source for cation and divides the deposition into two self-terminating reactions [16,17]. Each cycle includes the organometallic precursor pulsed in and purged out, followed by the oxidant specie pulsed in and purged out [18,19]. Plasma enhanced ALD uses the plasma oxygen as oxidant agent while water vapour is the main oxidant specie in thermal ALD [18,20]. Plasma enhanced atomic layer deposition (PEALD) is being used commercially for growth of the oxide high-κ gate dielectrics [21,22]. Prior to high-κ dielectric deposition, native oxide must be removed to improve equivalent oxide thickness (EOT).

ALD gown films are pin-hole free[20], but during the first cycles of PEALD the precursor is chemisorbed to the surface but will not fill all of the available sites due to steric hindrance [20,23,24]. The subsequent plasma oxygen replaces the organic ligands with oxygen and may oxidize the substrate and cause surface defects due to incomplete protection of the semiconductor surface. Substrate oxidation degrades the EOT and increases the D_{it} [25]. III-V substrates are affected even more than silicon, as they do not grow a robust and protective oxide [26]. During thermal ALD water oxidizes the highly reactive chemisorbed organometallic precursor but will not react directly with substrate during dielectric growth. On the other hand, gate dielectrics grown by thermal ALD (TALD) have inferior electrical characteristics compared to PEALD films due mainly to the higher concentration of bulk defects [21]. Residual oxidants are readily found in TALD films due to the surplus of water during deposition [27,28]. These residual oxidant species cause oxygen defects during post-heat treatment of MOS devices at temperatures roughly above 400 °C [27]. Interestingly, when plasma oxygen is used as oxidant, instead of water vapour, such species (e.g. oxygen interstitials) are not detected [29].

In this paper we propose that the combination of TALD and PEALD into a two-step gate oxide process will provide a superior gate oxide than is possible with TALD or PEALD alone. The proposal is that if a process is initiated with TALD, a protective layer will form that will protect the substrate from the oxygen plasma when the process is switched to PEALD. However, TALD films are susceptible to higher concentrations of bulk defects including oxygen defects. Oxygen vacancy causes numerous trap states [2,4] and, in turn, can be accounted as main component of trap assisted tunnelling in high-κ gate leakage current [30]. Starting with TALD and then switching to PEALD keeps the total number of bulk defects

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low, while maintaining a high quality interface. Electrical measurements are used to infer the presence, concentration and nature of the defects in high-κ dielectric thin films [30,31].

While there are many investigations comparing TALD and PEALD grown high-κ gate dielectrics, there is no systematic study of mixing the two techniques for optimal electrical characteristics. In this paper an in-depth electrical characterization and comparison of high-κ dielectrics (HfO_2 and ZrO_2) grown by PEALD, TALD and a mixed process is presented.

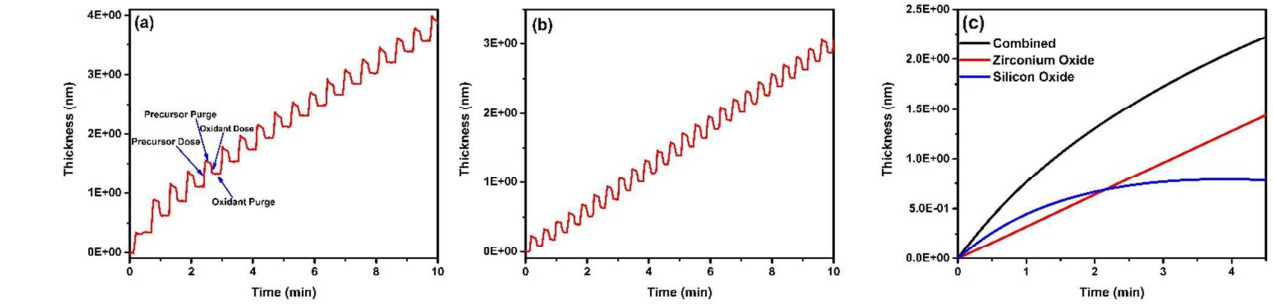
Experimental:

The MOS capacitors (MOSCAPs) were fabricated on p-type (100) silicon (10^{16} cm^{-3}). First, the substrate was buffer oxide etched for 2 minutes prior to gate dielectric deposition. High-κ dielectrics (HfO_2 and ZrO_2) were deposited utilizing low temperature ALD reactor (Kurt J. Lesker 150LX). The detailed description of the deposition procedure can be found in previous publications [8,9,32]. Substrate temperature was maintained at 100 °C and chamber pressure was kept at 1.07 Torr during thin film growth. Tetrakis(dimethylamido)-zirconium (Sigma-Aldrich >99.99%) and tetrakis(dimethylamido)-hafnium (Sigma-Aldrich >99.99%) were utilized as precursor for zirconium and hafnium, respectively. Different ratio of thermal to plasma enhanced ALD cycles were tried, while keeping the total number of cycles constant (60 cycles) for all specimen, to reach the optimum electrical characteristics.

Chromium contacts were deposited using DC magnetron sputtering and patterned by conventional lithography into a planar MOSCAP structures. The schematic of the MOSCAP devices can be found in previous publications [8,32]. The MOSCAPs were post-fabrication heat treated at 400 °C for 15 min under forming gas ($95\%N_2+5\%H_2$) to activate the device and anneal out the defects. *In-situ* spectroscopic ellipsometry (J.A. Woollam M2000DI) was utilized to investigate optical properties and thickness of the oxide films during growth. X-ray photoelectron spectroscopy (Kratos AXIS 165) was used to study stoichiometry and chemical state of the thin films. Electrical measurements were carried out utilizing a Keithley 4200-SCS to characterize the high-κ dielectric-semiconductor interface and thin film (HfO_2 and ZrO_2) quality. Cross section of the MOSCAP devices were investigated using field emission scanning electron microscopy (Zeiss, Sigma FE-SEM).

Results and Discussion:

In-situ spectroscopic ellipsometry was utilized to investigate the thickness evolution of the high-κ gate dielectrics during growth. The Tauc-Lorentz model was used to build an optical model for analysing the raw ellipsometry data. The ellipsometry resolved the thicknesses of 7.88 and 8.78 nm for specimen with 60 cycles of thermal and plasma enhanced ALD zirconia, respectively. Interestingly, growth per cycles (GPC) of 0.131 and 0.132 nm were resolved for thermal and plasma enhanced ALD, respectively, at 100 °C on silicon with native oxide. Assuming constant GPC, the plasma enhanced ALD grown zirconia is 0.86 nm thicker than expected value (0.132 nm x 60 cycles). Fig. 1 depicts the thickness evolution of (a) plasma enhanced ALD and (b) thermal ALD with time for zirconia by *in-situ* ellipsometry. Each individual step can be distinguished during an ALD cycle and studied independently in Fig. 1(a). The first cycles of plasma enhanced ALD have a higher GPC which gradually drops to 0.132 (nm) at approximately fourteen cycles. Conversely, thermal ALD has a steady growth per cycle from the initial cycles.



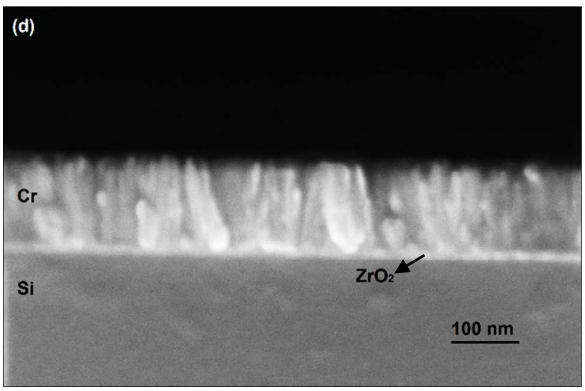


Figure 1. Real time thickness evolution of PEALD (a) and TALD (b) ZrO_2 thin films during growth (resolved from *in-situ* ellipsometry using Tauc-Lorentz model). (c) Resolving contribution of zirconium oxide and silicon oxide in PEALD grown ZrO_2 thin films assuming constant GPC for ZrO_2. (d) FE-SEM cross section of the MOSCAP device with 60 cycles of PEALD grown ZrO_2.

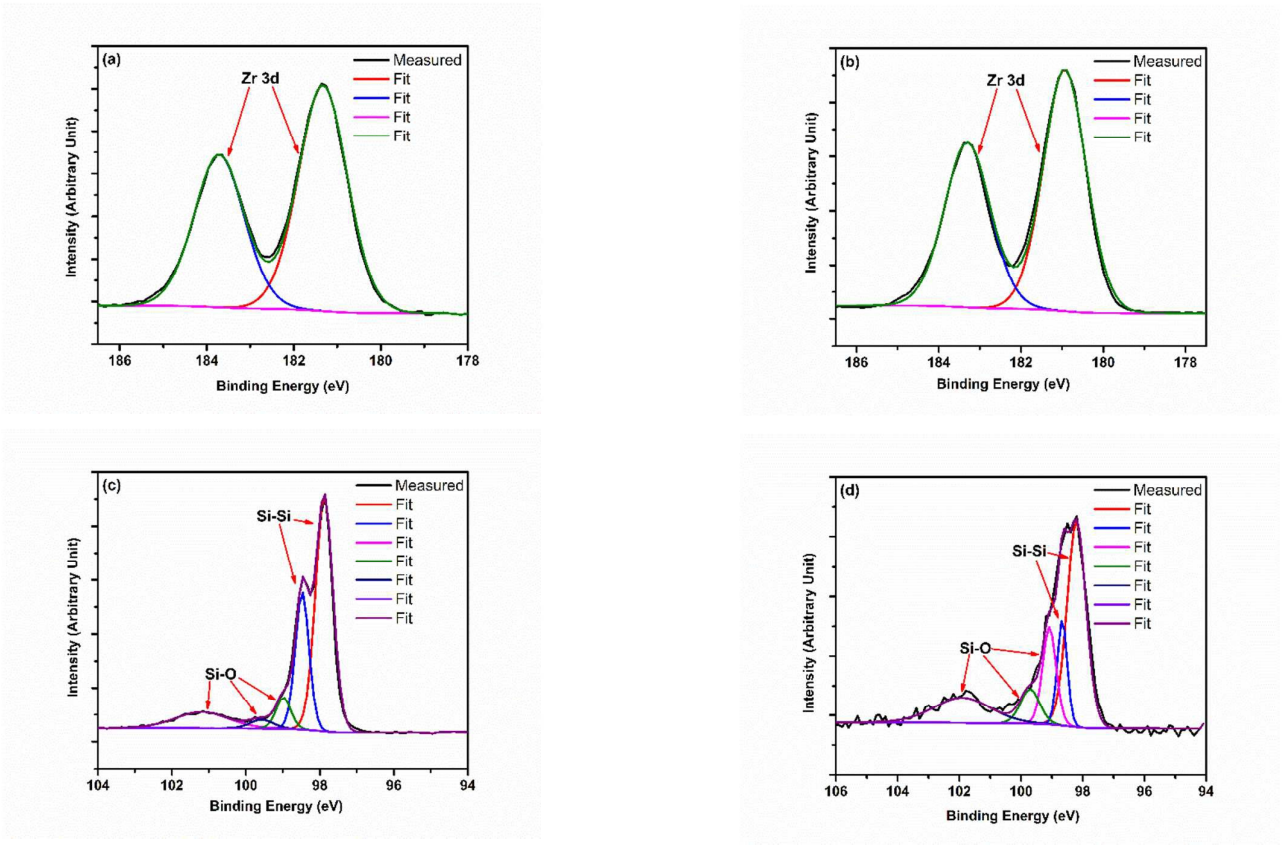


Figure 2. XPS results for Zr 3d for (a) TALD and (b) PEALD grown as-deposited zirconia films. Figure 2 (c) and (d) reveal Si 2p substrate XPS peaks for TALD and PEALD grown as-deposited ZrO_2.

After the first cycle, the surface is not completely covered with the metalorganic molecules due to steric hindrance of the organometallic ligands and, as a result, oxygen plasma can oxidize the silicon readily [23,24]. The silicon oxide unit cell is larger than the unit cell of silicon in the growth direction and adds to the GPC of ZrO_2 in ellipsometry results. Assuming a constant GPC for plasma enhanced ALD grown ZrO_2, the silicon oxide thickness evolution was determined in Fig. 1 (c). Evidently, silicon oxidation starts very fast, and gradually slows down with ZrO_2 growth and eventually plateaus at 0.8nm. Fig. 1 (d) illustrates the FE-SEM cross section of the MOSCAP device with 60 cycles of plasma enhanced ALD grown ZrO_2 (d).

Although ALD is well known for pin-hole free thin films [24,33], but plasma oxygen can diffuse through the underlying layer even at 100 °C [34]. Atomic oxygen lowers the thermodynamic barrier to diffusion compared to an oxygen molecule. Additionally, it takes a finite film thickness to inhibit oxygen diffusion completely. A. Afshar *et al.* reported that 45 cycles of thermal ALD grown alumina protected the underlying silver layer completely from oxidation by plasma oxygen at 100 °C [34].

The XPS results for the zirconium 3d in (a) TALD and (b) PEALD as-deposited ZrO_2 films is shown in Figure 2. The FWHM of Zr peaks in both Fig. 2(a) and (b) confirms the presence of pure zirconium oxide and no sub oxide peak or any shoulder peak is recognizable. Fig. 2(c) and (d) illustrate the silicon substrate 2p peaks for TALD and PEALD as-deposited ZrO_2 films, respectively. The PEALD grown films have a higher silicon oxide concentration (42.04 at%) than TALD grown films (20.54 at%). The contribution of interfacial silicon atoms compared to bulk silicon atoms cannot be resolved unambiguously from the x-ray photo electron signal. Furthermore, the XPS signal exponentially decays with thickness and the silicon oxide forms on the interface, and consequently disproportionately strong compared to the remaining silicon signal. Accordingly, the XPS results do not draw a quantitative picture but rather is a qualitative proof that there is a higher degree of substrate oxidation in PEALD growth compared to TALD growth.

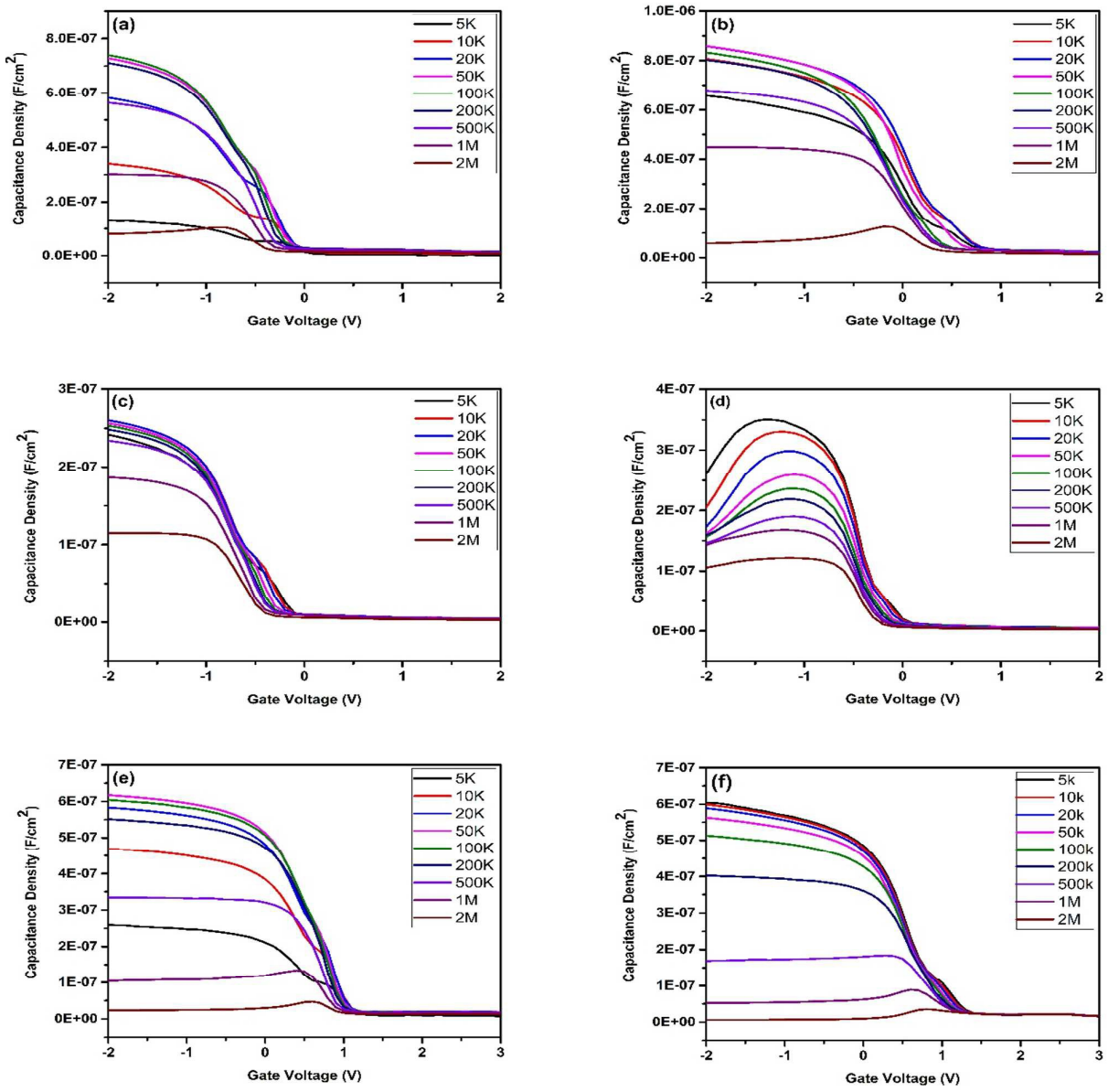


Fig. 3 (a-d) depicts the frequency dependent capacitance-voltage characteristics for ZrO_2 MOSCAPs. Keeping the total number of ZrO_2 cycles fixed (60 cycles), the number of TALD cycles are (a) 0, (b) 10, (c) 20, and (d) 60. Fig. 3(e) and (f) illustrate the CV characteristics for HfO_2 with (e) 0 and (f) 10 TALD cycles, respectively.

The capacitance density in accumulation (large negative bias) first enhances and then diminishes sharply with increasing TALD cycles. In PEALD the substrate oxidation degrades the EOT and D_{it} [25] while in TALD remaining oxidant groups will turn into bulk defects during post-fabrication heat treatment [27]. As expected, having the whole 60 cycles deposited with thermal ALD will lead to copious bulk defects and capacitance instability in accumulation (Fig. 4(d)). Starting with 30 cycles of TALD and then switching to PEALD also reveals almost the same characteristics (data not shown here). TALD grown dielectrics generally reveal a lower dielectric constant mainly due to formation of higher defect concentration [21]. The specimen with 10 cycles of TALD zirconia followed by 50 cycles of PEALD zirconia reveals highest accumulation capacitance density (0.88 $\mu F/cm^2$). The relatively steep transition to accumulation in all CV characteristics suggest high quality interfaces for MOSCAPs. Deep depletion can be detected from the finite slope at positive gate biases. Reaching the deep depletion is the major indicator that the Fermi level is not pinned and essentially moves into the other half of the band gap [35,36].

The frequency dispersion at just before entering accumulation, decreases systematically with increasing number of thermal ALD cycles. The hump before entering accumulation is mainly attributed to mid-gap D_{it} response [35,37]. The mid-gap D_{it} typically corresponds to semiconductor surface damage [38]. Consequently, increasing number of thermal ALD cycles can protect

the semiconductor surface from the following plasma oxygen. The hafnium oxide films also follow the same pattern. Furthermore, the low frequency (5K, 10K and 20K) capacitance of HfO_2 dielectrics boosts with increasing thermal ALD cycles which indicates higher interfacial quality. Furthermore, the specimen displays a significantly lower frequency dispersion in accumulation with increasing thermal ALD cycles up to twenty cycles. Above twenty cycles of TALD the bulk defects will dominate the CV response and amplify the frequency dispersion.

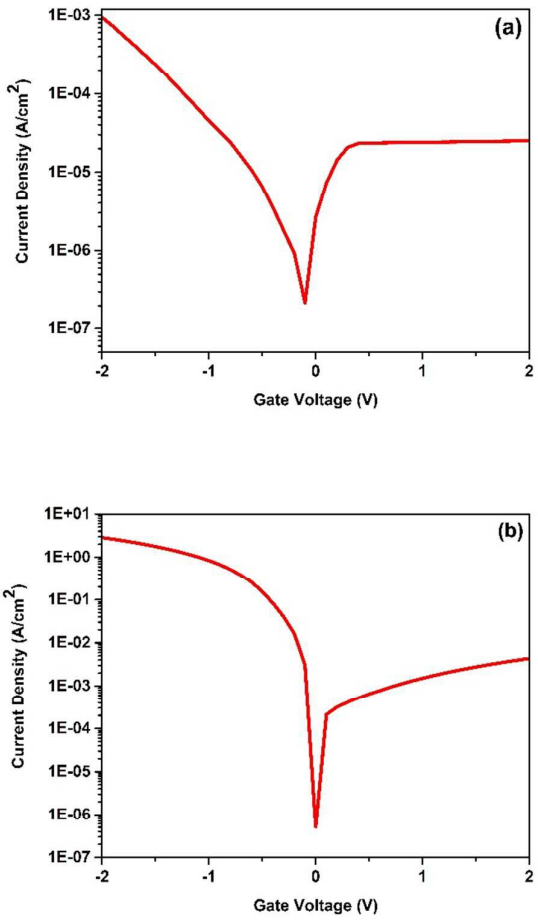


Figure 4. IV characteristics between -2V and 2 V of (a) plasma enhanced and (b) thermal ALD grown ZrO_2 MOSCAPs.

Figure 4(a) and (b) illustrate the leakage current of the PEALD and TALD grown ZrO_2 dielectrics as a function of gate voltage. The gate dielectric leakage current densities are 0.045 and 838 mA cm^{-2} at -1 V gate bias for PEALD and TALD grown zirconia dielectrics. The gate dielectric leakage current is over four orders of magnitude higher in TALD grown zirconia compared to PEALD one. The copious bulk defects in thermal ALD grown zirconia amplifies the leakage current. The leakage data for PEALD grown ZrO_2 is consistent with direct tunnelling as we have observed in prior work [8]. The direct tunnelling (DT) component of current density can be calculated using the following equation in one-dimension [25,39,40].

$$J_{DT} = \frac{q^3}{16\pi^2\hbar\emptyset_{OX}} E^2 . \exp\left(\frac{-4\sqrt{2m^*\emptyset_{Ox}{}^3}}{3\hbar q} E \left(1 - \left(1 - \frac{V}{\emptyset_{OX}}\right)^{\frac{3}{2}}\right)\right) \quad 1$$

Where m^*, q, $\hbar$, $\emptyset_{Ox}$ and E are the effective mass, elementary charge, the reduced Planck's constant, effective barrier height and the electric field, respectively.

On the other hand, the leakage current for TALD grown ZrO_2 is dominated by trap assisted tunnelling. Trap assisted tunnelling happens when minority carriers tunnel through the gate dielectric from occupied trap states. The trap centres are intermediate energy states, commonly, formed by defects. TALD grown dielectrics are assumed to have plentiful oxygen related defects mainly due to oxidant groups from abundant water during growth [27,28]. Trap assisted tunnelling (TAT) component of current density can be calculated according to following equation in one-dimension [29,30].

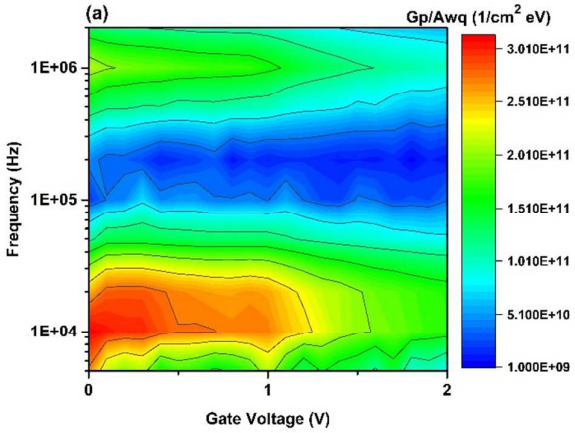
$$J_{TAT} = \frac{q^3 m^* M^2 N_T}{8\pi\hbar^3 (E_g - E_T)} E . \exp\left(\frac{-4\sqrt{2m^*(E_g - E_T)^3}}{3\hbar q E}\right) \quad 2$$

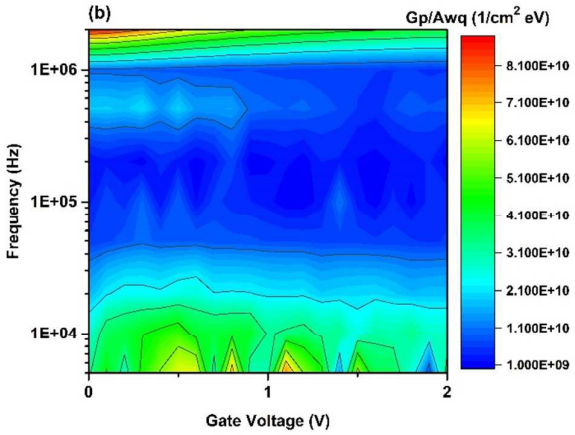
Where m^*, q, $\hbar$, E_g, E_T, N_T, M and E are the effective mass, elementary charge, the reduced Planck's constant, band gap, energy level associated with the trap centres, matrix element corresponding to the trap potential and the electric field, respectively.

Figure 5 depicts the normalized parallel conductance peak values as a function of gate voltage and frequency, where w is the frequency, A the active region area, Gp the parallel conductance, and q the carrier charge. Fig. 5(a) and (b) represent normalized parallel conductance of the zirconia MOSCAPs with 0 and 20 TALD cycles, respectively (total number of cycles were 60). The D_{it} can be reckoned by multiplying the normalized parallel conductance peak by a factor of 2.5. The D_{it} at 50 KHz and 1 V gate bias for specimen with 0, 10, 20, and 60 cycles of TALD zirconia were extracted to be $3.1x10^{11}$, $4.3x10^{10}$, $1.8x10^{10}$, and $4.5x10^{10}$ cm^{-2} eV^{-1}, respectively. Fig. 5(c) illustrates D_{it} with respect to number of TALD cycles. HfO_2 dielectrics revealed roughly one order of magnitude higher D_{it} but followed the same pattern (data not shown here). The D_{it} results disclose a very low concentration of interfacial states. Even the PEALD grown zirconia offers around one order of magnitude lower D_{it} than common high-κ/Si. The low concentration of interfacial states implies that the MOSCAP has a high quality of oxide-semiconductor interface. The main reason can be attributed to low deposition temperature which, in turn, reduces the magnitude of thermal expansion mismatch stress. K. Bothe *et al.* reported $4x10^{10}$ cm^{-2} eV^{-1} D_{it} for MOSCAPs with 40 cycles of PEALD zirconia on GaN grown at 100 °C substrate temperature [8]. Additionally, D_{it} systematically diminishes with increasing number of thermal ALD cycles and then rises trivially at higher TALD cycles. This implies that plasma oxygen contributes to the density of interfacial defects. For higher TALD cycles the remaining oxidant species generate abundant oxygen interstitials and migrate to the interface during post-fabrication heat treatment which, in turn, diminishes the D_{it} [27,28]. The D_{it} of the MOSCAP with 20 cycles of TALD followed by 40 cycles of PEALD is very low ($1.8x10^{10}$ cm^{-2} eV^{-1}) and comparable to the Si/SiO_2 interface mainly due to the combination of low temperature growth technique and twenty cycles of protective thermal ALD ZrO_2.

The conductance map provides the opportunity to study the nature of the interfacial defects and their life time. It also

provides a measure of the efficiency of the Fermi level moving in the band gap [41,42]. The normalized parallel conductance shifts over two orders of magnitude as the gate bias is swept from -0.25 and -1 V for all specimens, which indicates significant band bending with respect to gate bias sweeping (data not shown here).





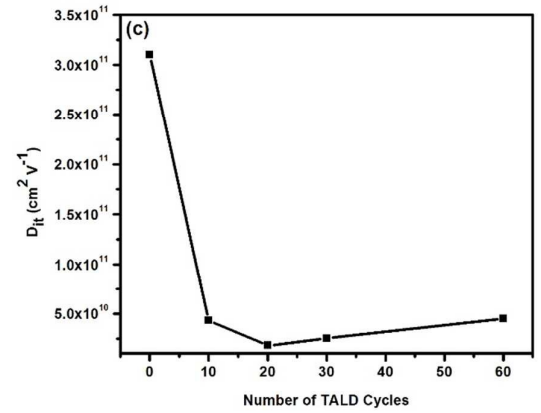


Figure 5. Conductance map between 0 V to 2 V and 10 KHz to 2 MHz of ZrO_2 gate dielectric MOSCAPs with (a) 0 and (b) twenty cycles of thermal ALD. w is the frequency, A the active region area, Gp the parallel conductance, and q the carrier charge (c) Density of interfacial traps with respect to number of TALD cycles (total number of cycles were 60 for all specimens).

Conclusion:

The electronic properties of PEALD and TALD grown high-κ gate dielectrics are significantly different. PEALD grown oxides show higher capacitance density for the same number of cycles and dramatically lower leakage current while higher density of interfacial traps. On the other hand, TALD grown dielectrics have a higher concentration of bulk defects. Leakage current is dominated by direct tunnelling in PEALD grown oxides while trap assisted tunnelling is predominant in TALD grown dielectrics. Starting with TALD and then switching to PEALD protects the substrate surface from plasma oxygen and lowers the D_{it}. Starting with ten cycles of TALD and then switching to PEALD enhanced the capacitance density while decreasing the D_{it}. The reason for the increasing capacitance density for ten cycles of TALD could not be resolved unambiguously. The specimen with twenty cycles of TALD had the lowest D_{it} ($1.8x10^{10}$ cm^{-2} eV^{-1}) but the capacitance density declined mainly due to inferior electrical characteristics of thermal ALD films. The specimen with ten cycles of TALD had the highest capacitance density (0.88 $\mu F.cm^{-2}$) but higher D_{it}. The mid-gap D_{it} decreased systematically with increasing number of thermal ALD cycles while the frequency dispersion in accumulation decreased significantly with increasing thermal ALD cycles up to twenty. In conclusion, the sample with ten cycles of TALD showed optimum capacitance density. On the other hand, the optimum process for minimal D_{it} includes twenty cycles of TALD followed by PEALD.

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