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All-solution-processed, flexible thin-film transistor based on PANI/PETA as gate/gate insulator

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Polyaniline (PANI)/pentaerythritol triacrylate (PETA) as gate/gate insulator are introduced to improve the device performance for all-solution-processed organic thin film transistors (TFTs). Direct comparison of the TIPS-pentacene crystal growth patterns between on PANI/PETA and on Si/SiO$_2$ as gate/gate insulators are investigated for the origin of different device performance.

Organic thin film transistors (TFTs) are envisaged as main electronic components in future electronic devices.[1] Along with advancements in organic electronics in general, organic TFTs will lead to the development of flexible, shatterproof, light-weight, and highly portable displays, like those in future-generation smart phones and tablet PCs, by enabling flexible pixel-switching devices. However, the use of inorganic materials for gate/gate insulators has been a main obstacle in realizing bendable and flexible form factors. It is therefore important to identify various materials that can be used as alternative flexible electrodes. Among the various materials that have been suggested, polyaniline (PANI) is considered as a promising candidate for low-cost and flexible electrodes in organic TFTs because of its high conductivity, solution processability, long-term stability, and superior mechanical flexibility.[2] Secondary doping of PANI with camphorsulfonic acid (CSA) in m-cresol makes this polymer highly-conductive and appropriate for use as thin-film electrodes on various substrates.[3] In terms of the gate insulators for organic TFTs, the material should have the functions such as abrasion resistance for subsequent solution deposition, good contact with neighbour materials, and water resistance for ambient fabrication condition.

In this study, we fabricated organic TFTs with 6,13-bis(triisopropylsilylethynyl)-pentacene (TIPS-pentacene) as an organic semiconductor, CSA-doped PANI as a gate electrode, and cross-linked pentaerythritol triacrylate (PETA) as a gate insulator. Polyethersulfone (PES) as a plastic substrate and silver (Ag) as
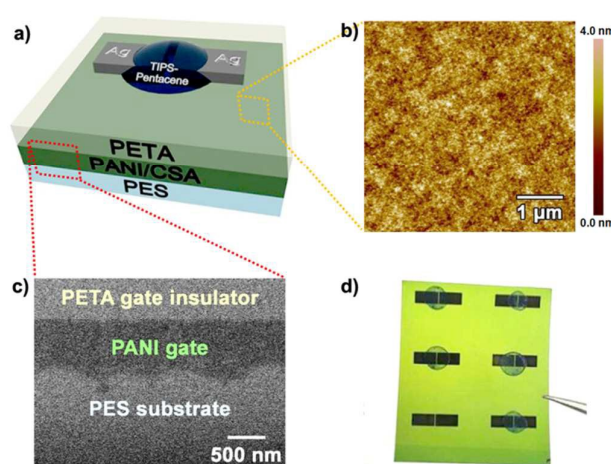

Fig. 1 (a) Schematic device configuration of the bottom-gated TIPS-pentacene TFT consisted of the PANI/PETA as the gate/gate insulator. (b) AFM image of a PETA gate insulating layer. (c) Cross-sectional SEM image consisting of a CSA-doped PANI gate and a PETA gate insulator on a PES substrate. (d) Photograph of as-prepared TIPS-pentacene TFTs.

source and drain electrodes were employed for all-solution-processed TFTs. The TIPS-pentacene was chosen as a representative organic semiconductor because of its its high mobility, air stability, and solution processability.[4] Particularly, CSA-doped PANI and PETA are highly compatible with the PES substrate, exhibiting good wettability, which provides mechanical stability and flexibility. We correlate the device performance to the morphology of the semiconductor on the gate insulator between PETA and SiO$_2$. The resulting PANI/PETA gate/gate insulator device produced a higher mobility than the Si/SiO2 device. This was attributed to the large crystal domains in the surface morphology of TIPS-pentacene on the PETA gate insulator.

As shown in Fig. 1a, Bottom-gate bottom-contact TIPS-pentacene TFT consisted of printed Ag source/drain electrodes on a cross-linked polymer gate insulator/CSA-doped PANI gate electrode which was spin-coated on a PES substrate. For comparison, we also fabricated reference TFT with Si/SiO$_2$ as gate/gate insulator in the identical configuration (Fig. S1, ESI†). The PANI gate adhered strongly to the PES and was in intimate contact (Fig. 1c), resulting in

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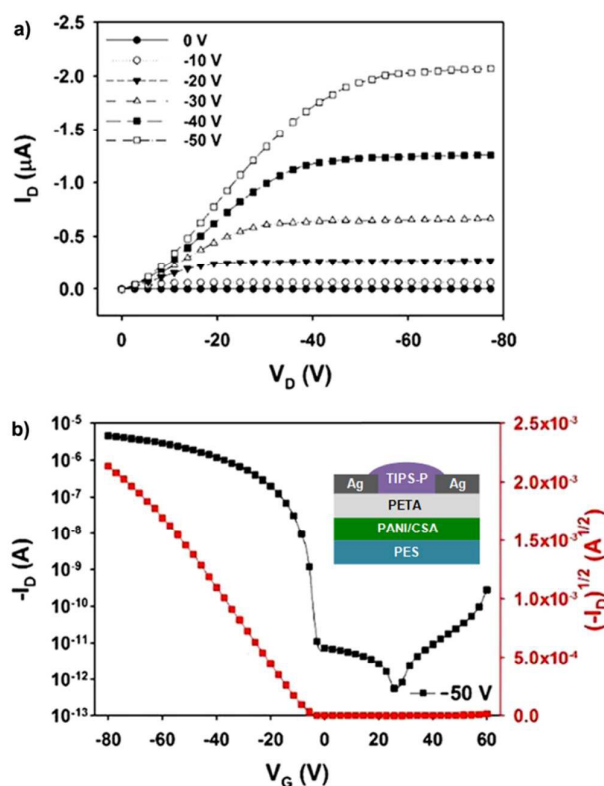
Fig. 2 (a-b) Source-drain current versus drain voltage characteristics of the TIPS-pentacene OTFTs with the PANI/PETA as gate electrode/gate insulator at gate voltages from 0 to –50 V. (b) Source-drain current versus gate voltage at V_{DS} = –50 V for the TIPS-pentacene OTFTs with the PANI/PETA as gate electrode/gate insulator.

a gate electrode on the substrate that was mechanically stable with regard to bending and folding condition. The PANI gate electrode (~700 nm thick), having macroporous structure originating from its intrinsically fibrous morphology (Fig. S2, ESI†),[5] showed a very low sheet resistance of 60 Ω sq^{-1} measured by 4-point probe system.

In this study, we adopt the PETA material as a gate insulator. It has been reported that the most commonly used gate insulator materials (*e.g.* poly(4-vinylphenol) (PVP) and poly(vinyl alcohol) (PVA)) are too sensitive to be employed in the device fabrication with ambient atmosphere due to oxygen and moisture. The performance of TFTs often degrades when the devices are exposed to air and moisture. It has been known that the PETA is a suitable material for a gate insulator material due to its ease in handling and processing, chemical resistance, and low volatility under ambient condition of the TFT fabrication process. The PETA film formation was successfully completed with UV-curing after spin-coating process within very short time (< 60 sec). All procedures were

Table 1. Electrical characteristics of TIPS-pentacene TFTs.

Samples (Gate electrode /insulator)	Parameters [a]		
	Mobility (cm^2/Vs)[b]	On/off ratio	V_{th} (V)
PANI/PETA	0.109 ± 0.02	8.04 × 10^6	–6.19
Si/SiO$_2$	0.019 ± 0.03	3.43 × 10^6	–4.23

[a] Saturation mobility at V_{DS}= –50 V
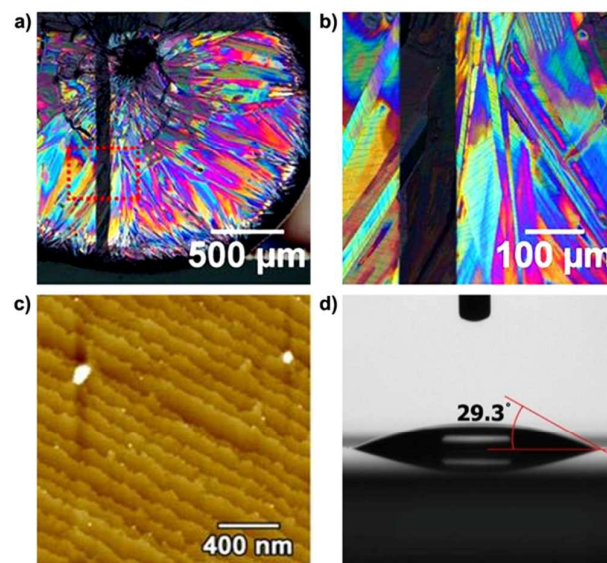[b] Total 20 devices were measured and calculated.

Fig. 3 (a) Optical microscope images of channel area in PANI/PETA-based TFTs. Dashed red areas in (a) is enlarged to (b). (c) AFM images of TIPS-pentacene in the channel area of TFTs. (d) Optical images of water droplet on the surface of the PANI/PETA substrate.

performed at room temperature in a glove box that provided oxygen-free conditions. The conversion value (degree of curing) of the as-prepared PETA film was estimated as 99.3 %, indicating high crosslinking yield. In addition, the root-mean-square (RMS) roughness of the PETA layer was 0.786 nm and the film thickness is about 750 nm by AFM (Fig. 1b, Fig. S3, S4, ESI†).

Fig. 1d illustrated the photographic images of PANI/PETA-based TFTs. Rectangular Ag source/drain electrodes (1.5 mm width and 3.0 mm length) were constructed on the cross-linked gate insulator film using an inkjet printer with a channel length of 100 μm. Drop-casted TIPS-pentacene semiconductor on the inkjet-printed channel showed radial growth patterns of crystallites.

Fig. 2 describes the electrical output and transfer characteristics of PANI/PETA-based TFTs. Most importantly, the calculated mobility of the PANI/PETA TFTs was roughly 6 times higher than that of the Si/SiO$_2$ TFTs (Table 1 and Fig. S5, ESI†). A Gaussian fit in Fig. S6 indicates the carrier mobility values of 0.109 ± 0.02 and 0.019 ± 0.01 cm^2 V^{-1} s^{-1} for PANI/PETA-based and Si/SiO$_2$-based TFT devices, respectively. The output curves from both TFTs are S-shaped in the linear region in Fig. 2. These curve patterns can be attributed to the contact resistance between TIPS-pentacene and Ag.[6] As mentioned it above, the PETA has a relatively higher roughness value than that of Si/SiO$_2$ surface (the roughness of thermally grown bare SiO$_2$ was known as ~0.2 nm in the literatures).[7] Charges transport along rough surfaces are more vulnerable to trapping, while smooth surface assists charges transport at the interface.[8] Thus, the rough surface of the PETA layer can be another reason for more inclined S-shaped output curve in the PANI/PETA device (Fig. 2a).

Despite the disadvantages of the rougher surface of PETA, the PANI/PETA devices exhibited enhanced mobility compared to that of Si/SiO$_2$ devices. In general, the mobility in semiconductors depends on the size and quality of the crystalline domains, which can be affected by deposition conditions and the nature of the insulator surface.[9] We therefore hypothesized that the origin of high mobility in these PANI/PETA-based TFTs is associated with the crystal
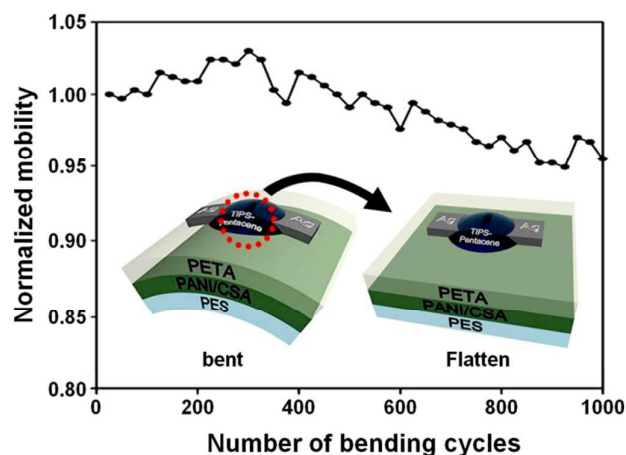
Fig. 4 A change in normalized mobility of the PANI/PETA-based TFT during 1000 times of bending cycles. The bending tests were performed using a home-made bending machine with bending radius of 20 mm.

growth pattern of TIPS-pentacene on the gate insulator. Many researchers have employed self-assembled monolayers over SiO_2 gate insulators to improve the molecular ordering of the polymeric semiconductor. In general, this resulted in increased mobility over bare SiO_2.[10] In this study, however, surface modification of the gate insulators was avoided in order to allow a direct comparison of crystal growth pattern on PETA and on bare SiO_2. The growth patterns of the semiconductor on both PANI/PETA and Si/SiO$_2$ were investigated, and correlated to device performance.

In Fig. 3a and b, optical microscope images show the crystal structures in the channel area of PANI/PETA TFTs. It can be easily observed that the morphology of TIPS-pentacene is largely dependent on that of the underlying layer. In order to gain insight of the morphology in the channel region, the AFM analysis was conducted. The AFM images proved that the differences in the crystal growth pattern of the TIPS-pentacene depended on differences in the gate insulator (Fig. S7, ESI†). In both PANI/PETA and Si/SiO$_2$ TFTs, we can distinguish three different regions along the transistor channel: a center region, a transition region, and an outer region, respectively. In particular, the morphologies of the transition regions of the PANI/PETA and Si/SiO$_2$ TFTs are significantly different. Akkerman *et al.* reported that the TIPS-pentacene channel was divided into different regions according to morphology where the largest field-effect mobility was observed in the transition region.[11] As presented in Fig. 3c and Fig. S7e, the width of the narrow elongated crystalline domains on PANI/PETA is larger than that on Si/SiO$_2$. We believe that this morphological difference is a dominant factor in enhancing the mobility of the PANI/PETA TFTs over that of Si/SiO$_2$ TFTs. The crystalline domains can be, moreover, identified with the interaction between non-polar TIPS-pentacene molecules and the surface of gate insulator. Water contact angle measurement revealed that the surface of the PETA (Fig. 3d), which was modified by the UV-curing process during the film forming, was more polar than that of SiO_2 in Fig. S8. The molecules of TIPS-pentacene can be attracted each other readily away from the polar surface of the PETA layer, increasing the size of the crystal domain. However, non-polar surface of the SiO_2 layer reduce the molecular packing of the organic semiconductor due to the pinning interaction between the SiO_2

surface and the TIPS-pentacene molecules, decreasing the crystal domain size.[12] **It also has been known that the polar interface of gate insulator induces the broadening of the density of states so that more trap states hinder the carrier transport.[13] However, it is believed that the crystal orientation-dependent morphology is more critical factor when determining the device performances, rather than carrier trapping effect by the polar surface of the gate insulator.** Consequently, deposition of TIPS-pentacene onto the relatively polar surface of PETA resulted in the growth of large crystal domains compared to those grown on the non-polar surface of the SiO_2 gate insulator. The narrowness of the crystalline domains in Si/SiO$_2$ TFTs may result in a large resistance between crystalline domains in the channel, thereby decreasing carrier mobility.

Furthermore, the cyclic bending test was performed to demonstrate the flexibility of the fabricated devices. The bending tests were performed using a home-made bending machine with bending radius of 20 mm. In Fig. 4, there is little change in normalized mobility over 1000 cycles. The initial mobility (0.11 $cm^2V^{-1}s^{-1}$) of the PANI/PETA-based TFT device was preserved by 95.4 % (0.10 $cm^2V^{-1}s^{-1}$) even though there is a slight fluctuation, indicating superior flexiblity and long-term durability of the PANI/PETA-based TFT devices.

Conclusions

In summary, PANI/PETA as gate/gate insulator was prepared by consecutive spin-coating of PANI and UV-cured PETA onto a PES substrate. This gate/gate insulator was incorporated into TIPS-pentacene TFTs through all-solution processing in an ambient atmosphere. Differences in the crystal growth pattern of TIPS-pentacene on different gate insulators were attributed to the polarity of the surfaces. Large crystalline domains enhanced carrier mobility in PANI/PETA-gated TIPS-pentacene TFTs. This result presents a practical strategy for the fabrication of high-performance, all-solution-processed, flexible electronic devices by introducing a highly conductive and flexible PANI/PETA gate/gate insulator.

Acknowledgement

Notes and references

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Graphical Abstract
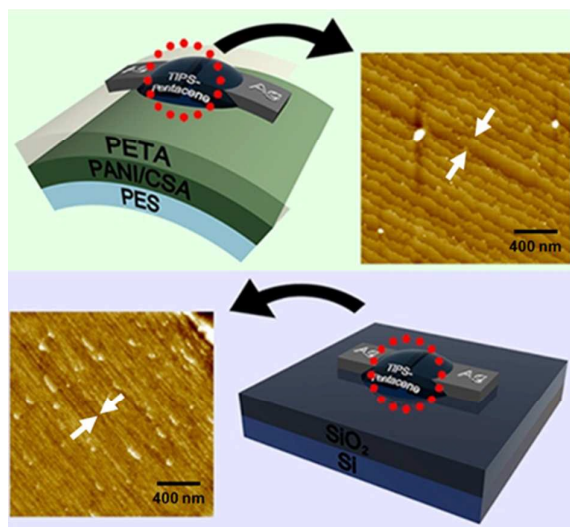
All-solution processed flexible thin-film transistor based on a PANI/PETA gate/gate insulator exhibited higher mobility than the device with a Si/SiO$_2$ gate/gate insulator because of large crystalline domains in the transition region.