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Optimization of textured process of silicon wafers by modifying the texturing temperature for heterojunction solar cells applications

Received 00th January 20xx,
Accepted 00th January 20xx

DOI: 10.1039/x0xx00000x

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In this work, a simple and effective method by two-step texturing temperature control is proposed to optimize the textured process of Commercial Cz-silicon wafers. The effective lifetime after the passivation of a-Si:H films is up to 1002.4 μs at 10^{15} cm^{-3} injection level by using this method which is close to the bulk lifetime of the silicon wafers. The result shows over 50% enhancement compared with those at the constant texturing temperatures. Furthermore, the lower reflectivity after the chemical polish treatment is achieved. The results of scanning electron microscope (SEM) images demonstrate that pyramid nucleation is more homogeneous and compact. This method is found remarkable performence to the improvement of external quantum efficiency at the wave band of blue visible light and the fill factor of silicon heterojunction solar cell. This study provides a universal textured process for heterojunction solar cells applications.

Introduction

Silicon surface texturing is a significant and standard process in crystalline silicon solar-cell fabrication. Texturing can reduce reflection and improve light trapping. Various methods are used to form pyramidal structure on <100>-oriented monocrystalline silicon wafers. Examples include the following: etching solutions of inorganic alkali: potassium hydroxide (KOH) or sodium hydroxide (NaOH) with IPA (isopropyl alcohol),[1–4] or other additives such as sodium carbonate (Na_2CO_3),[5] carbonate (K_2CO_3),[6] potassium, sodium phosphate (Na_3PO_4),[7], and Alkatex Zero™(GP Solar GmbH);[8,9] tetramethyl ammonium hydroxide[(CH3)4NOH];[10] organic alkali such as tetramethylammonium hydroxide (TMAH);[11] and ethylenediamine anhydrous (EDA).[12]

Among the methods mentioned above, etchant solutions of NaOH, IPA, and DIW (deionized water) are commonly used as a standard process for industrial solar-cell texturization. However, only a small number of studies have reported on the details of the texturing and effects on the silicon heterojunction solar cells, which has become a research hotspot in the photovoltaic field.[13, 14] As one of the most promising types of solar cell, silicon heterojunction (SHJ) solar cells exhibit high efficiency, low temperature processes, and low temperature coefficients. As with diffused junction crystalline-silicon solar cells, the optical gains of SHJ solar cells are generally improved by texturization. The electrical performance of the SHJ solar cells deteriorates because the rough silicon surface morphology easily leads to nonuniform deposition of the a-Si:H and the local epitaxy in the pyramid valleys. This harms the passivation of the a-Si:H/c-Si interface and the performance of the solar cells. [15] Therefore, the effects of texturing processes on optical properties, surface morphology, and electrical characteristics of the SHJ solar cells are worthy of studying in detail.

In the present study, attempts were made to investigate the influence of the etching temperature on the texturing surface morphology, and their effects on the passivation of the a-Si:H/c-Si interface. Then a novel method that adjusts the etching temperature during one process texturization to obtain an optimizing process is proposed. Finally, applications of the texturing process on silicon heterojunction solar cells are described.

Experimental

Texturization of the silicon wafers

Commercial as-cut, [100] oriented, 190 ± 20 μm, and n-doped (1–3 Ωcm) Cz-silicon substrates of area 5 cm × 5 cm were used in all etching processes and in solar-cell fabrication. The bulk lifetime of this kind of Cz-silicon substrates at 10^{15} cm^{-3} injection level is about 1 ms. To maintain a constant temperature and limit the evaporation of the solution, the etching processes were carried out in a capped glass vessel immersed in a constant-temperature water bath. Before the etching process, samples were cleaned by ultrasonication using acetone for 10 min to remove organic residues and were rinsed in deionized water. Then the samples were immersed in a Piranha solution (H_2SiO_4:H_2O_2 = 3:1) for 5 min to wipe off oxide organic residues that were not removed by the first step.

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Next, the oxide layer was removed with a 1% HF solution. In order to remove the saw damage, the wafers were dipped in a 10wt% NaOH solution at 80 ºC for 15 min. After that, wafer texturization was conducted for 40 min at different temperatures in a solution of 1wt% NaOH, 1wt% Na_2SiO_3, and 6% IPA, followed by a chemical polished solution ($HF:HNO_3:CH_3COOH$ = 1:3:3) for 30 s. Finally, the textured wafers were cleaned by the standard RCA cleaning process followed by a smoothing process [1% HF for 3 min, Piranha solution ($H_2SiO_4:H_2O_2$ = 3:1) for 5 min]. Before the wafers were transferred into the load-lock of a plasma-enhanced chemical vapor deposition (PECVD), they were dipped in 1% HF solution to remove their native oxide layer.

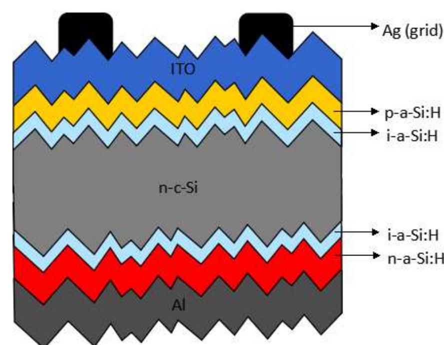

Fig. 1 The structure of the silicon heterojunction solar cells.

Fabrication of SHJ solar cells

The SHJ solar cells were deposited by a multichamber cluster radio frequency PECVD system. As is shown in Fig. 1, the structure of the silicon heterojunction solar cells is Ag/ITO/p-a-Si:H/i-a-Si:H/n-c-Si/i-a-Si:H/n-a-Si:H/Al. P-a-Si:H and n-a-Si:H films were deposited in two separation chambers of the PECVD system at 180 ºC. The p-a-Si:H films were deposited using gaseous mixtures of silane (SiH_4), trimethylboron (TMB), and H_2. The n-a-Si:H films were deposited using gaseous mixtures of SiH_4, phosphine (PH_3), and H_2.The ITO layer(～80 nm thick), the Ag grid(～600 nm thick), and Al back contact (～600 nm thick) were made by thermal evaporation and patterned onto the 1 cm^2 pad area.

Characterization

The surface morphology of the textured silicon surface was measured with a scanning electron microscope (SEM, ZEISS SUPRA 55VP). Spectral hemispherical reflection of the textured wafers was tested using a Varian-Cary 5000 integrating sphere spectrophotometer. To quantify the quality of passivation, 10-nm-thick i-a-Si:H films were symmetrically deposited on the textured wafers, and effective lifetime measurements were made by a noncontact Sinton WCT-120 tool in transient mode. The current-voltage (J-V) characteristics of the solar cells were measured at 100 mW cm^{-2} at 25ºC by using an AM 1.5 G solar simulator. The external quantum efficiency (EQE) was obtained by measuring the spectral response.

Results and discussion

Influence of the etching temperature on texturization

Generally, the temperature range in a texturing process involving alkaline and IPA mixed solution is from 75ºC to 80ºC. The boiling temperature of IPA is known to be 82ºC, so if the temperature exceeds 80ºC, excessively quick evaporation of IPA from the etching solution will deteriorate the texturization. Fig. 2 shows SEM images of the textured silicon surface when the texturing temperature is 80ºC after 40 min of texturing time. From the areas marked by the black circles in Fig. 2(a), one can see that at some places no pyramids exist, and at other places the peaks of certain pyramids collapse. Obviously, reflection will become high in areas that are not fully covered by the pyramids. In addition, the sizes of many pyramids processed at such temperature exceed 10 µm. Meanwhile, the sizes of some other pyramids are still on the submicron scale. The high etching temperature yields a high etching rate and results in the formation of large pyramids. However, the density of the pyramids is not sufficient to cover the surface completely. Furthermore, the inhomogeneous distribution and inadequate coverage of the pyramids will lead to more defects and deteriorate the passivation of the a-Si:H/c-Si interface.

Fig. 2(b) shows a SEM image of the textured silicon surface at 80ºC for 40 min before the chemical polish treatment. There are many submicronic pyramids at the edges of the large pyramids. This indicates that the nucleation and growth of pyramids occur simultaneously. This agrees with the observations of Bachtouli et al.[16] From Fig. 2(a) and (b), we can conclude that at 80ºC the etching rate is too high to be controlled easily.

Fig. 3 shows a SEM image of the textured silicon surface at 75ºC for 40 min. There are many areas marked with black circles, and that no pyramids form at those places. This will increase the reflection of the texturing surface. In addition, the sizes of the pyramids range from approximately 5 µm to submicrons—smaller than those at 80ºC. In principle, the higher the temperature, the faster the etching rate. Furthermore, the faster the etching rate, the bigger the size of the pyramids. This occurs because the etching rates of the (100) and (110) crystallographic planes increase faster than those of the (111) crystallographic plane when the temperature increases.[17] Generally, pyramid density will increase if the pyramids are small; as a result, the density of pyramid valleys (which plays a role in the degradation in quality of a-Si:H/c-Si interface passivation) will increase. The increased recombination rate in these valleys can be explained by local epitaxial growth and/or a mixed phase, making a nonabrupt a-Si:H/c-Si interface.[18]

As is well known, the stage of pyramid nucleation is a crucial period for texturing. Therefore, in order to understand fully the origin of differences between morphology at 80ºC and 75ºC after the 40-min texturing time, texturing experiments whose duration is only 5 min at different temperatures are carried out.Figs. 4(a),(b) (c) and (d) show SEM images of the textured silicon surface at 75ºC,

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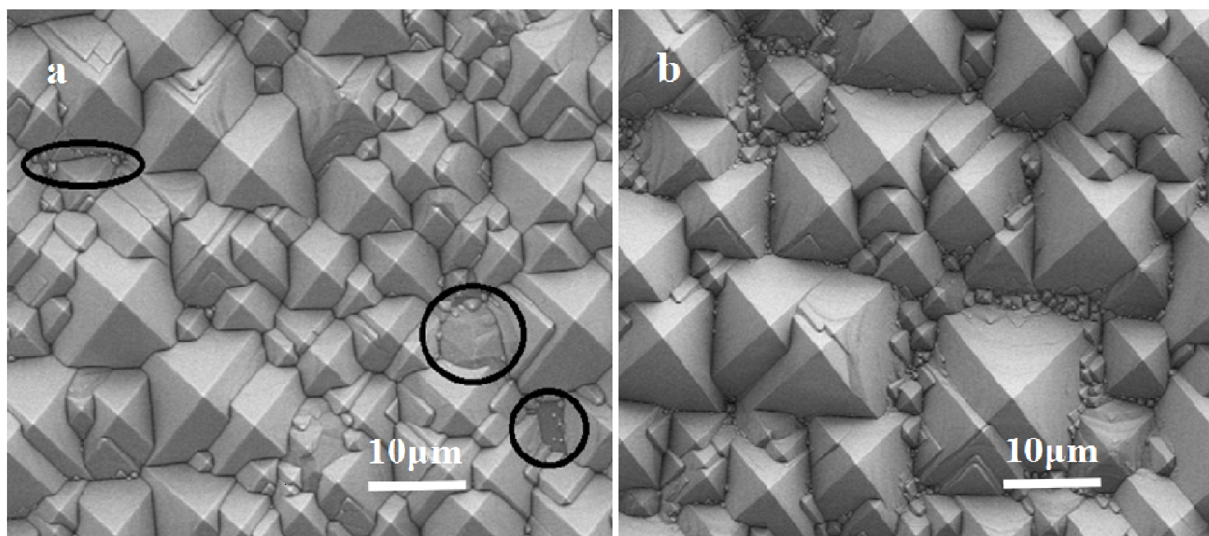


Fig. 2 SEM images of the textured silicon surface at 80°C for 40min. (a) after the chemical polish treatment, (b) before the chemical polish treatment.

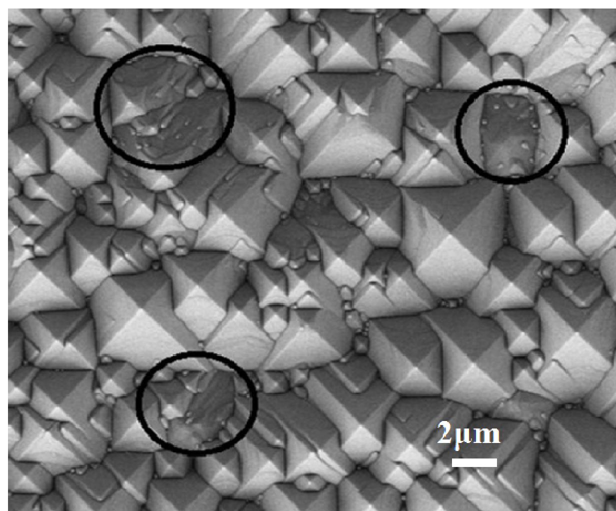
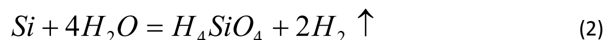


Fig. 3 SEM image of the textured silicon surface at 75°C for 40min(magnified by 2000 times).

75ºC, 80ºC, and 75/80ºC (increasing the temperature from 75ºC to 80ºC at a constant rate in 5 min, and then keeping the temperature constant at 80ºC for another 35 min) with a duration of 5 min. Comparing Fig. 4(a) with Fig. 4(c), the density of pyramid nucleation at 75ºC is higher than the density at 80ºC. However, both approaches result in pyramids of approximately 2 μm, owing to the competition between the nucleation and growth of pyramids. Low temperature increases the absorption of nonreactive and massive ions and particles (Na^+, IPA) on the surface and restricts the access of OH-, which is responsible for silicon oxidation. This leads to a large number of pyramid starting points and a low etching rate. Therefore, low temperatures such as 75ºC are beneficial for pyramid nucleation. However, one can observe from Fig. 4 (b) that some flocculent precipitates leave around the pyramids. As is well known, the chemical equation of the etching reaction is as follows:

$$Si + 2NaOH + H_2O = Na_2SiO_3 + 2H_2\uparrow \quad (1)$$

In equation (1), the oxidant is water (H_2O), and the deoxidizer is silicon (Si). Actually, the reaction process is composed of three reactions:



$$Si + 4H_2O = H_4SiO_4 + 2H_2\uparrow \quad (2)$$

$$H_4SiO_4 = H_2SiO_3 + H_2O \quad (3)$$

$$H_2SiO_3 + 2NaOH = Na_2SiO_3 + 2H_2O \quad (4)$$

If the reaction product H_4SiO_4 [e.g., $Si(OH)_4$] cannot be decomposed into H_2SiO_3 and H_2O [as shown in reaction (3)] and transported into the solution, where it is neutralized by NaOH through reaction (4) in a sufficient and timely manner, it will polymerize and become precipitates. Therefore, we deduce that the flocculent precipitates shown in Fig. 4(b) are residual polymerized $Si(OH)_4$, which are harmful to texturing. Clearly, 75ºC is too low a temperature for the timely neutralization of the $Si(OH)_4$. Similarly, Seidel et al[19] reported that for alkaline solutions with a high water concentration, the rate of dissolution of Si atoms from the crystal surface is so high that the transport of the $Si(OH)_4$ complex into the bulk solution cannot maintain its production. When the concentration of this complex on the Si surface becomes too high, it will polymerize and cover the surface.

A further observation from Fig. 4(a) is the nonuniform distribution of pyramid nucleation. However, temperatures that are too high, such as 80ºC, will lead to the excessively quick

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Fig. 4 SEM images of the textured silicon surface (a) at 75°C for 5min, (b) at 75°C for 5min, (c) at 80°C for 5min, (d) using the method of modifying the temperature of the solution with duration of 5min.

evaporation of IPA, which results in the inhomogeneity of pyramid nucleation, as shown in Fig. 4 (c).

As mentioned above, we can conclude that pyramid nucleation is sensitive to temperature. Low temperatures lead to a large number of pyramid nucleations but have no benefit for the decomposition of $Si(OH)_4$. By contrast, at high temperatures, the etching process is inclined to grow pyramids instead of resulting in pyramid nucleation. Meanwhile, high temperatures will lead to excessively quick evaporation of IPA and water. This is detrimental to the homogeneity of pyramid distribution. In other words, constant temperature, whether high or low, is not good enough to result in texturing at the stage of pyramid nucleation. Therefore, we propose a novel texturing process method by two-step texturing temperature control. At the beginning, a low temperature (75ºC) should be used to ensure that large numbers of pyramid nucleations occur on the surface of silicon wafer. However, to avoid the harmful effects of low temperature (75ºC), once the wafers are immersed in the solution, the temperature increases to 80ºC at a constant rate in 5 min. This is an effective method to avoid the disadvantageous influence of low temperatures and to improve the growth of pyramids. Secondly, the temperature is kept constant at 80ºC for 35 min to ensure that the pyramids grow to large sizes and cover the surface completely.

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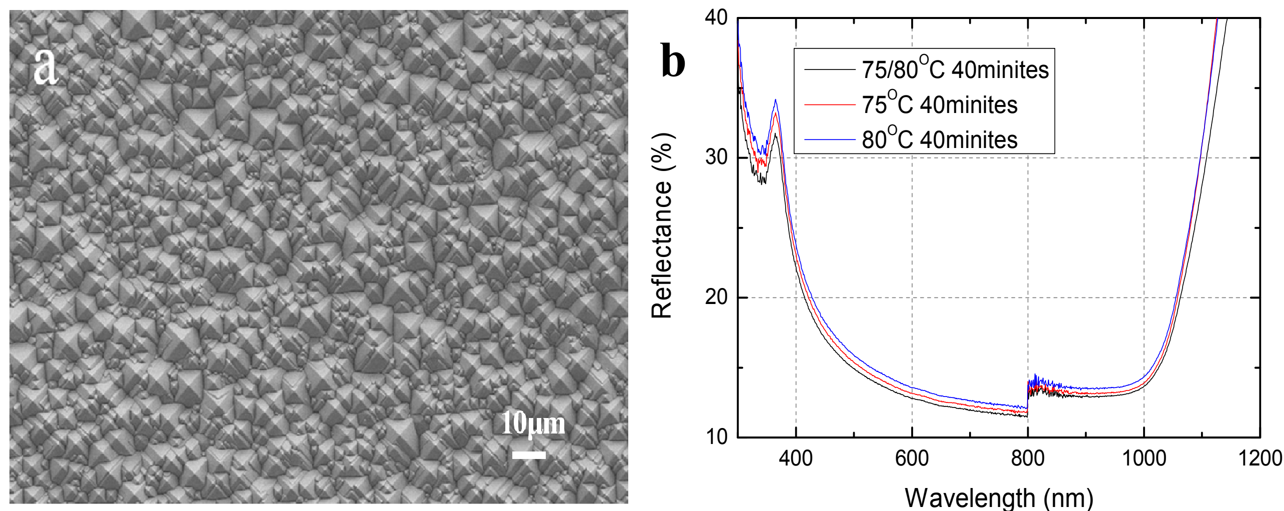

Fig. 5 (a) SEM image of the textured silicon surface using the method of modifying the temperature of the solution with duration of 40min. (b) Reflectance of wafers textured at different temperatures after CP133 treatment as a function of wavelength.

In the following pictures we will mark this method as “75/80ºC”.

Fig. 4(d) shows a SEM image of the textured silicon surface using the method of modifying the temperature of the solution (e.g., the first step of the two-step texturing temperature control) for 5 min. The morphology of the silicon surface shown in Fig. 4(d) is at the stage of pyramid nucleation. Comparing Fig. 4(d) with Fig. 4(a) and Fig. 4(c), one can see that pyramid nucleation using a variable-temperature process is more homogeneous and compact.

Fig. 5 (a) shows a SEM image of the textured silicon surface using the method of modifying the temperature of the solution for 40 min. We can see that the pyramids fully cover the surface and that no blank area exists. Fig. 5(b) plots the reflectance of wafers textured at different temperatures after a chemical polish treatment as a function of wavelength. We observe that reflectance using variable-temperature method is lower than that at 75ºC and 80ºC. As can be seen from Fig. 5(a), the structure of pyramid distribution with variable temperature is large pyramids (approximately 10 μm) that are surrounded by some small pyramids of several microns each. Furthermore, the pyramids fully cover the surface, and no blank area exists. Shui-Yang Lien et al[14] found that this kind of structure with large pyramids surrounded by small pyramids can achieve low reflectance by reflecting incident light three times.

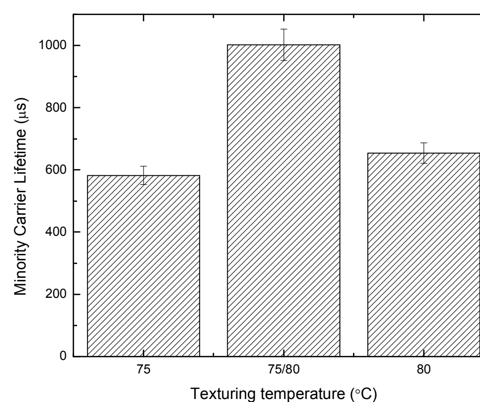

Fig. 6 Minority carrier lifetime at an injection level of 10^{15} cm^{-3} for texturization substrates at different textured temperatures, using symmetrical 10 nm i a-Si:H layers .

Fig. 6 plots the minority carrier lifetime at an injection level of 10^{15} cm^{-3} for texturization substrates at different texturing temperatures, using symmetrical 10-nm i-a-Si:H layers. As shown in Fig. 6, the effective lifetime and the corresponding implied

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V_{oc}(not shown in Fig. 6) of silicon wafers using the variable-temperature method are 1002.4 µs (close to the bulk lifetime of the silicon wafers) and 0.727 V, respectively. These results are higher than those of constant low temperature (75ºC) (584.23 µs, 0.713 V) or constant high temperature (80ºC) (655.77 µs, 0.714 V). Especially, the effective lifetime shows over 50% enhancement comparing to those at the constant texturing temperatures. As previously shown, the texturing effect of the wafers using variable temperatures provides the best results, in which the surface is completely covered with pyramids and no blank areas. The average size of the pyramids at 75ºC is smaller than that at 80ºC. Consequently, the density of the pyramid valleys, which is detrimental to the passivation of the a-Si:H/c-Si interface, is higher than that at 80ºC. Therefore, compared with the passivation effect of silicon wafers at 80ºC, the effective lifetime and corresponding implied V_{oc} of the silicon wafers textured at 75ºC is slightly lower.

Performance of SHJ solar cells based on different textured wafers

The results of the J-V measurements are shown in Fig.7. Clearly, owing to a beneficial passivation effect and low reflection, the parameters of the solar cell at variable texturing temperatures are better than others. As is well-known, open-circuit voltage is strongly dependent on the passivation effect of the silicon wafers. We can also find out this dependence from the relationship between the lifetime and the corresponding implied V_{oc}. From the results shown in Fig.6, we see that the samples at variable texturing temperatures have the highest lifetimes, i.e., the best passivation effects. As a result, the open-circuit voltage of the solar cell at variable texturing temperatures is the highest among the different texturing temperature processes. Improved external quantum efficiency in the wave band of blue visible light is achieved, as shown in Fig. 8. From Fig. 5(b), one can see that the reflectance of the sample using a variable texturing temperature is the lowestamong the different texturing temperature processes, which means that much more incident light can be absorbed by the solar cell. Meanwhile, excellent passivation (seen in Fig. 6) reduces the recombination of photo-induced carriers at the a-Si:H/c-Si interface. These two factors improve the external quantum efficiency of the solar cell. Because of the improvement in morphology and excellent passivation at the a-Si:H/c-Si interface by using the method presented above, films deposit more uniformly and there is no epitaxy growth on the surface of the silicon wafer. These characteristics also improve the fill factor of the solar cell.

Conclusions

In this work, texturing solutions with NaOH/IPA at different temperatures have been investigated with respect to the size and density of pyramids as well as the reflection and passivation of the a-Si:H/c-Si interface. SEM images of the texturing silicon surfaces show that pyramid nucleation is sensitive to temperature. Constant temperatures are not suitable for texturing at the stage of pyramid nucleation. Therefore, we proposed a novel texturing process method by two-step texturing temperature control. As a

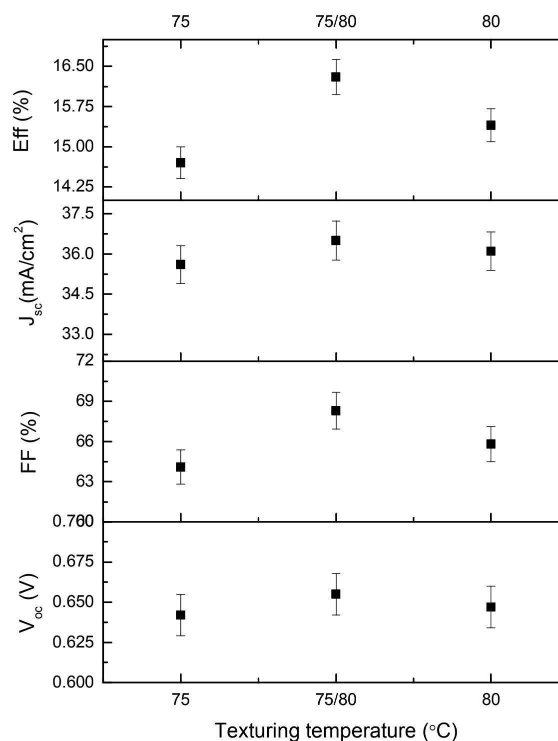

Fig. 7 Performance of SHJ solar cell for three types of textured substrates prepared at different temperatures.

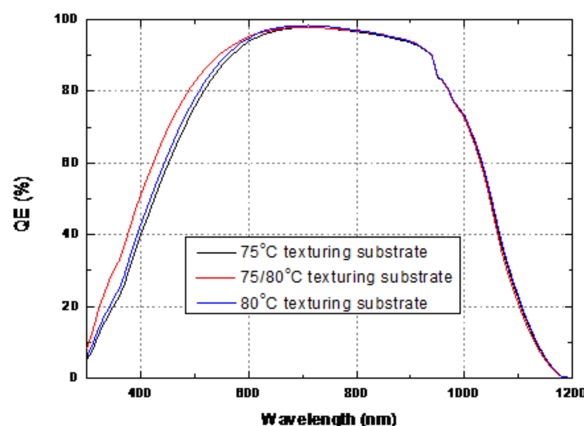

Fig. 8 External quantum efficiency (EQE) curves of silicon heterojunction solar cells prepared with different texturing temperatures.

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result, the effective lifetime which is close to the bulk lifetime of the silicon wafers and low reflection were achieved. With respect to the application of SHJ solar cells, the external quantum efficiency at the wave band of blue visible light and the fill factor of the solar cell were improved.

Acknowledgements

The authors gratefully acknowledge the supports from National Basic Research Program of China (Grant Nos. 2011CBA00706, No.2011CBA00707), Hi-Tech Research and Development Program of China (2013AA050302), Science and Technology Support Program of Tianjin (12ZCZDGX03600), Major Science and Technology Support Project of Tianjin City (11TXSYGX22100), Natural Science Foundation of China(61474065), International cooperation projects of the Ministry of science and technology(2014DFE60170), and Specialized Research Fund for the PhD Program of Higher Education (20120031110039).

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