RSC Advances

ROYAL SOCIETY OF CHEMISTRY

www.rsc.org/advances

RSC Advances

RSCPublishing

COMMUNICATION

Solution-processed SiO_2 gate insulator formed at low temperature for zinc oxide thin-film transistors

Cite this: DOI: 10.1039/xoxxoooooox

Yesul Jeong,[a] Christopher Pearson,[a] Hyun-Gwan Kim,[b] Man-Young Park,[b] Hongdoo Kim,[c] Lee-Mi Do[d] and Michael C Petty[a*]

Received ooth January 2015,
Accepted ooth January 2015

DOI: 10.1039/xoxxoooooox

www.rsc.org/

We report on the low-temperature formation (180 °C) of a SiO_2 dielectric layer from solution-processed perhydropolysilazane. A bottom-gate zinc oxide thin-film transistor has subsequently been fabricated that possesses a carrier mobility of 3 cm^2/Vs, an on/off ratio of 10^7 and minimal hysteresis in its transfer and output characteristics.

There is worldwide academic and industrial interest in the science and technology of flexible displays. Much of the research is focused on the development of thin film transistors (TFTs) with excellent electrical behaviour coupled with long device lifetime. An additional desirable feature is the ability to fabricate the TFTs at a low (< 200 °C) temperature, which will reduce the processing costs. In these respects, the semiconductor zinc oxide (ZnO) has received much attention.

Studies of compatible gate insulators to use with ZnO TFTs are now increasing. Organic materials, e.g. PS-b-PMMA, inorganic compounds, e.g. Al_2O_3, Y_2O_3, HfO, and hybrid structures, e.g. $LaZrO_X/SiO_2$, PVP/Al_2O_3 PMMA/SiO_2, CNO-PMMA, PMSQ are all attractive candidates for solution-processed gate delectrics.[1-6] However, it should be noted that there are relatively few studies reporting ZnO TFTs using solution processing for fabricating both the semiconductor *and* gate insulator layers.[7-10] There remain many issues to be addressed. For example, Jung et al.[7] noted that films of organic gate insulators including poly(4-vinyphenol), poly-methacrylate, polyimide and polyvinyl alcohol can be solution processed at low temperature. However, the thin films can easily be damaged by ammonia in the ZnO solution. In addition, solution-processed ZnO TFTs with organic gate insulators can possess relatively low field-effect mobilities.[8] Ko et al.[9] examined solution-processed ZnO transistors with a $HfLaO_X$ gate insulator. This material, annealed at 500 °C, exhibited a low leakage current and a high dielectric constant; a TFT with good electrical properties was subsequently fabricated (carrier mobility of 1.6 cm^2/Vs). However, the processing temperature of 500 °C is unsuitable for flexible display substrates.

Organosiloxane-based organic-inorganic hybrid gate insulators have also been studied.[7] Although both ZnO and the gate insulator were formed by spin coating and a relatively low annealing temperature of 230 °C was employed, the devices possessed a field effect mobility of 0.32 cm^2/Vs, a threshold voltage of 0.89 V and on/off ratio of ~ 10^5.

Silicon dioxide (SiO_2), deposited by plasma-enhanced CVD, has been extensively used as a gate insulator for ZnO TFTs as the devices generally show excellent electrical performance, with high mobility, on/off ratio and stability. Commercial production of ZnO TFTs has already adopted SiO_2 as the gate insulator. A disadvantage, however, is that the processing takes place in a high vacuum system at an elevated temperature. A notable recent achievement by Wu et al.[5,6] is the low-temperature solution processing of printable indium-gallium-zinc oxide TFTs at 150 °C. Relatively high mobilities (> 0.8 cm^2/Vs) were obtained, although an additional passivation layer was required to achieve high on/off ratios and low leakage currents.

Perhydropolysilazane (PHPS) offers an attractive, low-temperature route to the preparation of SiO_2 thin films. This precursor polymer is composed of a network of Si-N, Si-H and N-H chemical groups; solution processing can be conveniently used to convert the material into either dense Si_3N_4 or SiO_2 films, depending on the precise processing conditions. For example, Matsuo et al.[11] have developed SiO_2 films having a density of 2.1-2.2 g/cm^3, a refractive index of 1.45-1.46 and a dielectric constant of 4.2 using PHPS deposited onto a Si substrate. These parameters are comparable to values for vacuum-processed SiO_2 prepared at a high reaction temperature (density of 2.0-2.3 g/cm^3, refractive index of 1.46 and dielectric constant of 3.9). In addition, this study demonstrated that PHPS can be transformed into SiO_2 by heat treatment at 450 °C, but the addition of a catalyst to the PHPS can reduce the processing temperature (300-350 °C). Much research is now being undertaken to optimise the conversion method in order to

[a] School of Engineering and Computing Sciences and Centre for Molecular and Nanoscale Electronics, Durham University, South Road, Durham DH1 3LE, UK.

[b] Research Center for Nano-Materials, DNF Co.Ltd., Daejeon 306-802, Korea.

[c] Department of Advanced Materials Engineering for Information and Electronics, Kyung Hee University, Yongin 446-701, Korea.

[d] IT Convergence Technology Research Laboratory, Electronics and Telecommunications Research Institute, Daejeon, Korea.

† Electronic Supplementary Information (ESI) available: [details of any supplementary information available should be included here]. See DOI: 10.1039/c000000

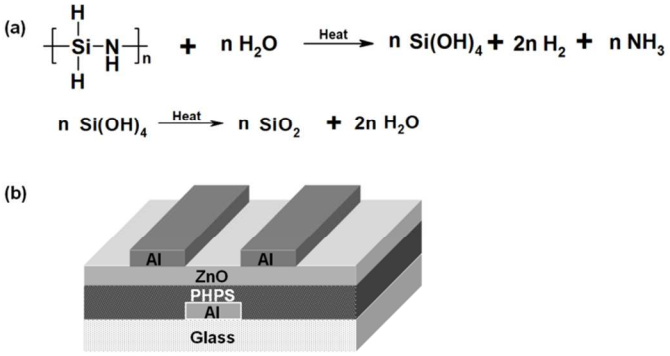

Fig. 1. (a) Conversion of solution-processed PHPS to SiO_2. (b) Schematic diagram of solution-processed, bottom-gate, top-contact ZnO TFTs with cured PHPS insulator.

lower further the processing temperature.[12-16] For example, Bauer et al.[12] introduced moisture during the heat treatment, which had a significant effect on accelerating the reaction, although it still proved difficult to form a fully converted SiO_2 film at temperatures lower than 150 °C.

In this study, a solution-processed SiO_2 gate insulator is prepared from PHPS using spin coating and a low curing temperature of 180 °C. To complete the conversion to SiO_2, an oxygen plasma treatment is used after the curing process. The film properties are examined using atomic force microscopy (AFM), Fourier Transform Infrared (FTIR) spectroscopy and electrical conductivity measurements. We demonstrate that the plasma-treated SiO_2 gate insulator can be used in a bottom-gate TFT architecture to achieve solution-processed ZnO TFTs with excellent electrical performance.

The conversion of PHPS in a high humidity environment is depicted in Fig. 1(a). Ideally, hydrolysis and polycondensation are the main routes to form SiO_2 from PHPS.[12] In these processes, hydrogen and nitrogen from the polymer network react with H_2O, releasing gaseous hydrogen and ammonia, followed by polycondensation by the elimination of water. A schematic diagram of the bottom-gate, top-contact TFT structure used in this study is presented in Fig. 1(b). An aluminium (Al) gate electrode (100 nm thickness) was first defined by thermal evaporation through a shadow mask onto clean glass substrates. PHPS solution (10% in di-n-butylether (DEB), DPS-10, DNF Co. Ltd) was spin-coated at 3000 rpm for 30 sec (as-deposited PHPS), followed by pre-annealing on a hotplate for 5 min at 150 °C (pre-annealed PHPS). The PHPS films were then cured on a hotplate for 1 hr at 180 °C in an Espec SH-641 bench-top type temperature and humidity chamber. The temperature of the environmental chamber was 75 °C with a relative humidity (RH) of 75% (cured PHPS). The final thickness of PHPS after curing was about 200 nm.

Following curing, the films were treated using an oxygen plasma system (Yield Engineering System Inc., YES-R3) for 10 sec at an RF power of 40 W (plasma treated PHPS). Details of the ZnO solution preparation have been described in a previous paper.[17] The ZnO solution was deposited as the active layer (< 20 nm thickness) on PHPS/Al/Glass, before and after plasma treatment, by spin coating for 30 sec at 3000 rpm and annealing in air at 140 °C for 30 min. Finally, Al source/drain (S/D) electrodes, 100 nm thickness, were deposited by thermal evaporation through a shadow mask. The ratio of channel width to length (W/L) was 20 (W = 4000 µm/ L = 200 µm). The morphology of PHPS deposited on Al/glass substrates was measured using a Digital Instruments Nanoman II atomic force microscope (AFM). Chemical structural changes due to plasma treatment of the PHPS films were identified using a Nicolet Nexus FTIR spectrometer.

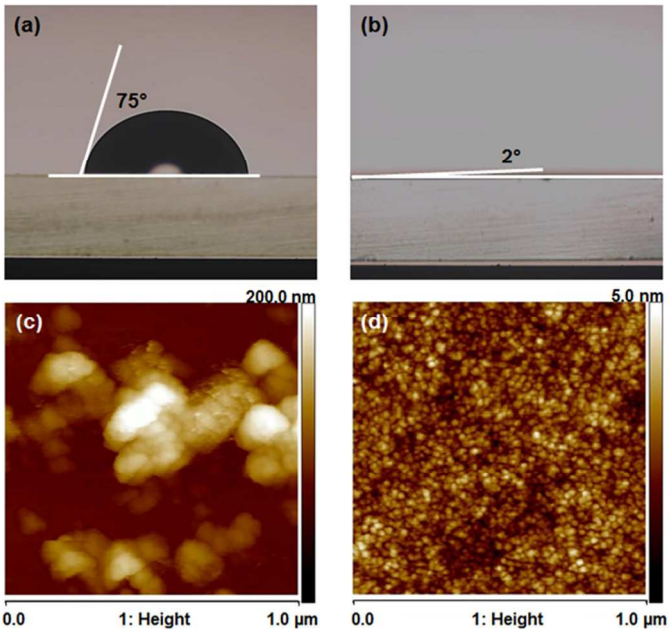

Fig. 2. The contact angles for water measured on (a) cured PHPS, (b) plasma treated cured PHPS film. AFM topography image of ZnO thin film spin-coated onto (c) cured PHPS, (d) cured PHPS film with plasma treatment.

To examine the dielectric properties of PHPS before and after plasma treatment, top Al electrodes with an area of 0.8 x 10^{-2} cm^2 were deposited through a shadow mask by thermal evaporation. The current density, J, versus electric field, E, was measured using a Keithley 2400 SourceMeter. Electrical characterisation of the transistors was undertaken in the dark and in air using a Keithley 4140B pA meter/DC voltage source. The surface morphology and wettability were investigated using an AFM and water drop contact angle measurement system, respectively. The surface wettability and roughness of the insulator layer are directly connected to the device performance of bottom-gate, top-contact TFTs. A rough insulator surface generally provides carrier trapping sites, which leads to poor electrical performance. The arithmetic average roughnesses for cured PHPS and plasma treated PHPS obtained from AFM images are both

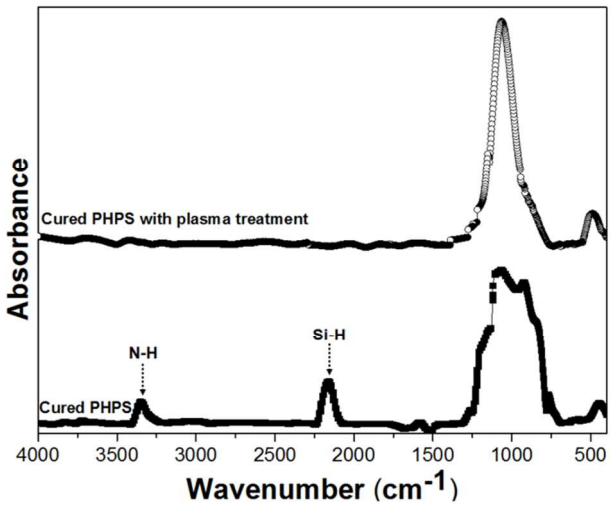

Fig. 3. Comparison of FTIR spectra for cured PHPS and cured PHPS with an oxygen plasma treatment.

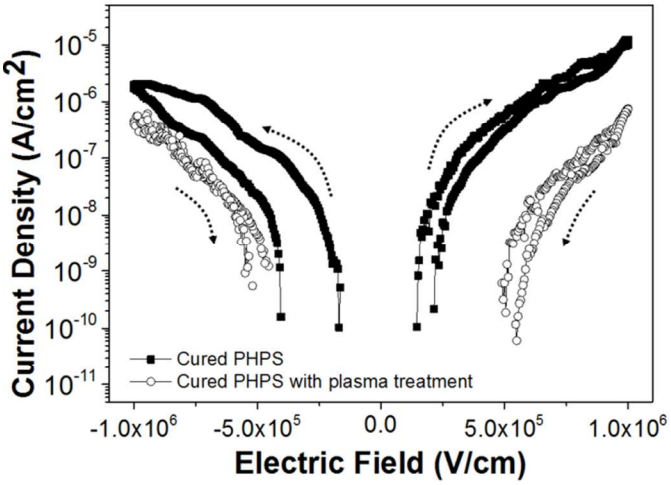

Fig. 4. Change in the current density versus electric field for cured PHPS as a function of the measurement sequence.

approximately 0.23 nm (Fig. S1). This indicates that the PHPS has a smooth surface, and plasma treatment does not cause surface damage.

In bottom-gate, top-contact TFT architectures, the active layer is coated on top of the gate insulator layer, which means that a hydrophilic surface is necessary in order to form an active layer having a uniform surface. Figure 2 shows the profile of a water drop applied to cured PHPS (a) before and (b) after plasma treatment. The hydrophobic cured PHPS surface (contact angle ~ 75 °) is clearly changed to hydrophilic (contact angle ~ 2 °) by the plasma treatment. The effect that this processing has on the subsequent deposition of the ZnO active layer was investigated using tapping mode AFM. Figure 2(c) reveals the distribution of ZnO across a cured PHPS surface. Relatively large grains are evident and it seems unlikely that there would be a continuous channel path between the S and D electrodes. The AFM image in Fig 2(d) shows the surface of a ZnO film on top of a plasma-treated PHPS layer. The distribution of the material is much more uniform and a continuous film can be seen. AFM images contrasting the surface morphologies of the evaporated aluminium, the as-deposited PHPS thin film and the pre-annealed PHPS are provided as Supplementary Information.

Figure 3 depicts the FTIR absorption spectra of cured PHPS films before and after plasma treatment. Further FTIR data, including a table of peak assignments, are provided as Supplementary Information. It is common that SiO_2 networks can be formed by hydrolysis of Si-NH bonds and subsequent formation of Si-O bonds at temperatures above 300 °C.[11, 15, 16] As shown in Fig. 3, the cured PHPS film reveals peaks corresponding to N-H bonds (stretch at 3360 cm^{-1}, bend at 1180 cm^{-1}), Si-H bonds (stretch at 2160 cm^{-1}) and Si-N bonds (stretch at 920 cm^{-1} and 840 cm^{-1} in Si-N-Si) with a weak Si-O bond (rock at 460 cm^{-1}, stretch at 1060 cm^{-1}).[18, 19] This suggests that the PHPS film is only partially converted to SiO_2 by the curing process at 180 °C. However, the spectrum is significantly changed after the oxygen plasma treatment. The bands at 1183 cm^{-1} and 3360 cm^{-1} (N-H) and 2160 cm^{-1} (Si-H) all diminish in intensity, whereas the band at 460 cm^{-1} (Si-O) increases. The Si-N (stretch in Si-N-Si at 840 cm^{-1}) disappear while the Si-O bond (stretch at 1060 cm^{-1}) is enhanced, with a shoulder at 1163 cm^{-1} (stretch in Si-O-Si). The strong absorption of the Si-O band is typical of a SiO_2 network, indicating that the film has been completely transformed from PHPS precursor polymer to SiO_2 following the plasma treatment. The results suggest that the plasma treatment can assist in the formation of a condensed SiO_2 network, thereby allowing low temperature processing.

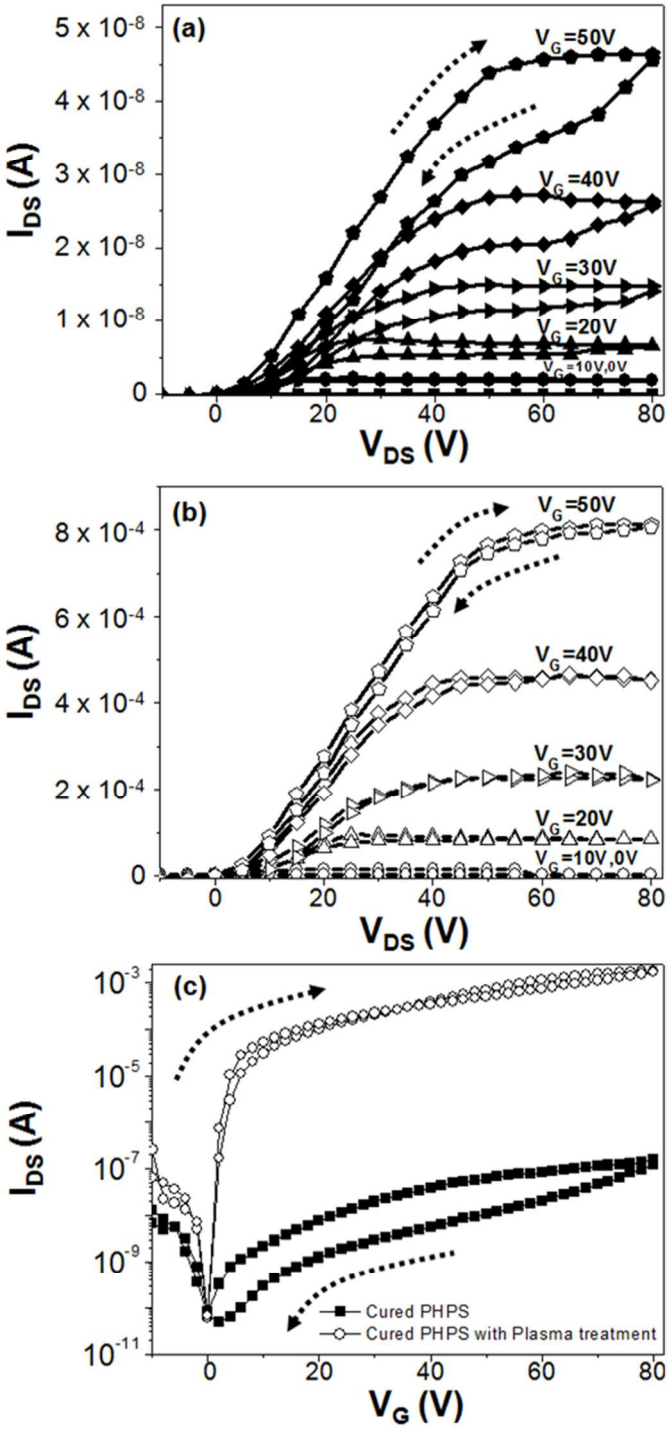

Fig. 5. Output characteristics of ZnO TFTs with (a) cured PHPS and (b) plasma treated cured PHPS insulator. (c) Change in the transfer characteristic of ZnO TFTs depending on plasma treatment.

Figure 4 shows the *J-E* properties of cured PHPS and plasma-treated PHPS sandwiched between Al electrodes. The voltage was swept first from 0 V ~ +20 V ~0 V and then from 0 V ~ -20 V ~0 V (0.02 V/s). It was found that the leakage current decreased after plasma treatment. For example, cured PHPS showed current density in the range 1.1 x 10^{-10} to 1.2 x 10^{-5} A/cm^2 for electric fields between 0.25 and 1 MV/cm. Following the plasma processing, the current density through the thin film was reduced by approximately two orders of magnitude (7.6 x 10^{-7} A/cm^2 at 1 MV/cm). The final

Table. 1. Summary of the electrical performance of ZnO TFTs using cured PHPS, before and after plasma treatment.

	Mobility ($cm^2V^{-1}s^{-1}$)	I_{on}/I_{off} ratio	V_{TH} (V)	SS ($Vdecade^{-1}$)	D_{it} ($eV^{-1}cm^{-2}$)
Cured PHPS	1 x 10^{-2}	~10^2	-1.2	5.5	1.1 x 10^{13}
Plasma treated PHPS	3.2	~10^7	-1.4	0.2	3.6 x 10^{11}

conductivity is comparable to that of the solution-processed insulator (10^{-6} A/cm^2).[20-22]

Solution-processed ZnO TFTs with cured and plasma-treated PHPS insulators were fabricated to investigate the potential of these films as gate insulators in these devices. Figure 5 shows the drain-source current, I_{DS}, versus drain-source voltage, V_{DS} (output characteristics (a) and (b)) and I_{DS} versus gate voltage, V_G (transfer characteristics (c)). The output characteristics of both devices showed typical n-channel operation, with large hysteresis between the forward and reverse V_{DS} scans observed for ZnO TFTs with cured PHPS (Fig 5(a)). Figure 5(c) contrasts the transfer characteristics of ZnO TFTs with cured PHPS and plasma treated PHPS, both measured in air; V_{DS} was fixed at 50 V, and V_G was swept reversibly from -10 V to 80 V. The parameters extracted from the transfer curves are summarised in Table 1. The values of mobility and threshold voltage, V_{TH}, were extracted from the slope of the forward scan and x-intercept, respectively, of a plot of $(I_{DS})^{1/2}$ against V_G. The subthreshold swing, SS, values were extracted from the linear portion of the log I_{DS} vs V_G plot of the forward scan. In addition, the changes in interface trap density values, D_{it}, were calculated using

$$\mathrm{SS} = \frac{qk_BT(N_{ss}t_{ch} + D_{it})}{C_i \log(e)}$$

where N_{ss} is the density of bulk traps and t_{ch} is the thickness of the channel layer.[23] D_{it} was estimated on the assumption that $N_{ss}t_{ch} \ll D_{it}$. The ZnO TFTs based on thermally cured PHPS revealed a mobility of 0.01 cm^2/Vs, on/off ratio, I_{on}/I_{off}, of ~10^2 and V_{TH} of -1.2 V with large hysteresis, as shown in Fig 5(c). However, a marked improvement in the device performance was observed for ZnO TFTs with plasma treated PHPS. The mobility and on/off ratio were increased to 3.2 cm^2/Vs and ~10^7, respectively, and there was negligible hysteresis between forward and reverse scans. In addition, V_{TH} was slightly shifted to -1.4 V. Moreover, Table 1 reveals that the plasma processing provides a significant reduction in D_{it}, suggesting that this process modifies the electronic nature of the interface between the ZnO and the PHPS as well as affecting the bulk of the insulating layer (i.e. increasing its electrical resistance).

We have also taken the opportunity to investigate the variability in the electrical behaviour of individual devices. In our preliminary study, a batch of sixteen devices was fabricated. In the case of the devices based on the cured PHPS, 9/16 structures exhibited working transistor characteristics; the yield improved to 15/16 for devices fabricated with the plasma processing. The average values for the mobility and on/off ratios (values averaged for the working devices) were 6x10^{-3} cm^2/Vs and 5.1x10^2, respectively for the devices based on the cured PHPS and 1.9 cm^2/Vs and 1.5x10^7 for TFTs fabricated using plasma processing.

It is significant that our ZnO TFTs with plasma treated PHPS exhibit a high mobility compared with other reports on ZnO TFTs produced by solution processing at low temperature (processing temperature of 200-300 °C, mobility of less than 0.5 cm^2/Vs).[7, 8, 24, 25] It is known that unreacted groups resulting from incomplete PHPS conversion can be attributed to degradation of electrical properties such as large hysteresis, because they act as carrier trapping centres at the semiconductor/dielectric interface and/or in the bulk of the dielectric.[26-29] Our FTIR studies suggest that these residual groups are completely removed and a SiO_2 network is fully formed following plasma treatment. In addition, ZnO is evenly distributed on the plasma treated PHPS surface, resulting from a change in the surface wettability, as evidenced by AFM.

In summary, a solution-processed SiO_2 gate insulator with good electrical properties has been prepared at the relatively low temperature of 180 °C. Subsequent oxygen plasma treatment of this thermally cured thin film led to a modification of the surface properties and an improvement in its electrical resistance. Solution-processed ZnO/PHPS TFTs with this plasma treatment achieved a mobility of 3.2 cm^2/Vs, V_{TH} of -1.4 V and on/off ratio of ~10^7 with negligible hysteresis. No additional passivation layer between the semiconductor and insulator was needed to achieve this performance. These results suggest that SiO_2 formed from cured PHPS followed by plasma treatment could be a good candidate as the gate insulator material for high performance solution-processed ZnO TFTs.

Acknowledgments

This work was supported by the Industrial Strategic Technology Development Program (10041808, Synthesis of Oxide Semiconductor and Insulator Ink Materials and Process Development for Printed Backplane of Flexible Displays Processed Below 150°C) funded by the Ministry of Knowledge Economy (MKE, Korea).

Notes and references

1. G. Adamopoulos, S. Thomas, D. D. C. Bradley, M. A. Mclachlan and T. D. Anthopoulos, *Appl. Phys. Let.*, 2011, **98**, 123503.
2. J. S. Meena, M. -C. Chu, R. Singh, C. -S. Wu, U. Chand, H. -C. You, P. -T. Liu, H. -P. D. Shieh and F. -H. Ko, *RSC Advs.*, 2014, **4**, 18493.
3. S. Y. Je, B. G. Son, H. G. Kim, M. Y. Park, L. M. Do, R. Choi and J. K. Jeong, *ACS Appl. Mater. Interfaces*, 2014, **6**, 18693.
4. B. -U. Hwang, D. -I. Kim, S. -W. Cho, M. -G. Yun, H. J. Kim, Y. J. Kim, H. -K. Cho and N. -E. Lee, *Org. Electron.*, 2014, **15**, 1458.
5. X.Wu, F.Fei, Z.Chen, W.Su and Z.Cui, *Compos. Sci. Technol.*, 2014, **94**, 117
6. X. Wu, Z. Chen, T. Zhou, S. Shao, M. Xie, M. Song and Z. Cui, *RSC Adv.*, 2015, **5**, 20924
7. Y. Jung, T. Jun, A. Kim, K. Song, T. H. Yeo and J. Moon, *J. Mater. Chem.*, 2011, **21**, 11879.
8. K. Kim, E. Lee, J. Kim, S. Y. Park, K. -H. Lim, C. Shin and Y. S. Kim, *J. Mater. Chem. C*, 2013, **1**, 7742.
9. J. Ko, J. Kim, S. Y. Park, E. Lee, K. Kim, K. -H. Lim and Y. S. Kim, *J. Mater. Chem. C*, 2014, **2**, 1050.
10. J. Hwang , K. Lee , Y. Jeong , Y. U. Lee , C. Pearson , M. C. Petty , and H. Kim, *Adv. Mater. Interfaces*, 2014, **1**, 1400206.
11. H. Matsuo and K. Yamada, *Convertech*, 1995, **23**, 25.
12. F. Bauer, U. Decker, A. Dierdorf, H. Ernst, R. Heller, H. Liebe and R. Mehnert, Prog. *Org. Coat.*, 2005, **53**, 183.
13. T. Kubo, E. Tadaoka and H. Kozuka, *J. Sol-Gel Sci. Technol.*, 2004, **31**, 257.

14. H. Kozuka, M. Fujita and S. Tamoto, *J. Sol-Gel Sci. Technol.*, 2008, **48**, 148.
15. K. -S. Park, P. -S. Ko and S. -D. Kim, *Thin Solid Films*, 2014, **551**, 57.
16. S. -D. Kim, P. -S. Ko and K. -S. Park, S*emicond. Sci. Tech.*, 2013, **28**, 035008.
17. Y. Jeong, C. Pearson, Y. U. Lee, L. Winchester, J. Hwang, H. Kim, L.-M. Do and M. C. Petty, *J. Electron. Materials*, 2014, **43**, 4241.
18. R. M. Almeida and C. G. Pantano, *J. Appl. Phys.*, 1990, **68**, 4225.
19. B. C. Trasferetti, R. V. Gelamo, F. P. Rouxinol, M. A. Bica de Moraes and C. U. Davanzo, *Chem. Mater.*, 2005, **17**, 4685.
20. M. D. Morales-Acosta, M. A. Quevedo-López and R. Ramírez-Bon, *Mater. Chem. Phys.*, 2014, **146**, 380.
21. D. Wee, S. Yoo, Y. H. Kang, Y. H. Kim, J. -W. Ka, S. Y. Cho, C. Lee, J. Ryu, M. H. Yi and K. -S. Jang, *J. Mater. Chem. C*, 2014, **2**, 6395.
22. R. Branquinho, D. Salgueiro, L. Santos, P. Barquinha, L. Pereira, R. F. Martins and E. Fortunato, *ACS Appl. Mater. Interfaces*, 2014, **6**, 19592.
23. D. W. Greve, *Field Effect Devices and Applications: Devices for Portable, Low-Power, and Imaging Systems*, 1st edn., 1998, p. 87.
24. K. S. Jang, D. Wee, Y. H. Kim, J. Kim, T. Ahn, J. W. Ka and M. H. Yi, *Langmuir*, 2013, **29**, 7143.
25. S. Yoo, J.-Y. Yoon, J. Ryu, Y. H. Kim, J.-W. Ka, M. H. Yi and K. -S. Jang, *Appl. Surf. Sci.*, 2014, **313**, 382.
26. S. Chang, Y. -W. Song, S. Lee, S. Y. Lee and B. -K. Ju, *Appl. Phys. Lett.*, 2008, **92**, 192104.
27. R. B. M. Cross, M. M. D. Souza, S. C. Deane, and N. D. Young, *IEEE Trans. Electron Dev.*, 2008, **55**, 1109.
28. T. -D. Tsai, J.-W. Chang, T.-C. Wen and T. -F. Guo, *Adv. Funct. Mater.*, 2013, **23**, 4206.
29. D. K. Hwang, K. Lee, J. H. Kim, S. Im, J. H. Park and E. Kim, *Appl. Phys. Lett.*, 2006, **89**, 093507.