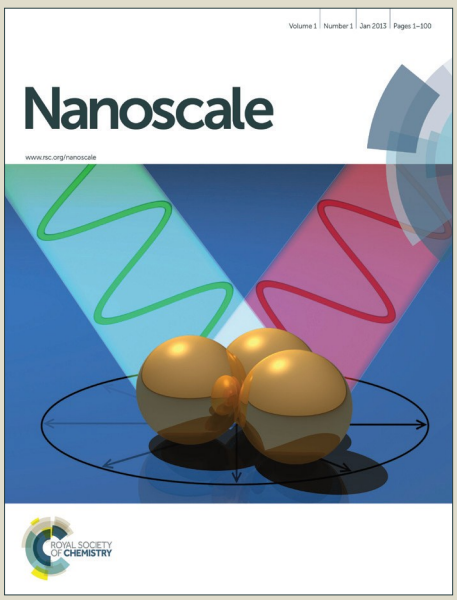
Nanoscale

Accepted Manuscript



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CLEAN GRAPHENE INTERFACES BY SELECTIVE DRY TRANSFER FOR LARGE AREA SILICON INTEGRATION[††]

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Submitted to

Nanoscale

September 2015

Second Revision February 1, 2016

ABSTRACT

Here we present a very fast, selective mechanical approach for transferring graphene with low levels of copper contamination from seed wafers on which it was grown to target wafers for very large scale integration (VLSI) electronics. We found that graphene/copper or copper/silicon oxide delamination paths could be selected by slow and faster separation rates, respectively. Thus graphene can be transferred to a target wafer, either exposed or protected by the seed copper layer, which can later be removed by etching. Delamination paths were identified by SEM and Raman spectroscopy. The sheet resistance of the graphene produced by the two approaches was slightly higher than graphene transferred by PMMA wet-transfer process, indicating reduced impurity doping, and the variation in the sheet resistance values was much lower. Copper contamination levels, quantitatively established by TOF-SIMS, were several orders of magnitude lower than the values for PMMA assisted transfer. In addition, we demonstrated that top-gated transistor devices from our mechanical, delamination transferred graphene exhibited superior transistor behavior to PMMA-assisted wet transfer graphene. The adhesion energy, strength and range of the interactions were quantitatively determined by nonlinear fracture analyses, which suggest that the roughness of the interface between graphene and copper plays an important role with implications for improvements in manufacturing processes.

Introduction

The combination of graphene, the two-dimensional carbon sheet with sp^2 bonding, with silicon technology is widely considered among the greatest prospects for transitioning graphene discoveries from research laboratories into practical electronic applications. Integration of graphene devices with silicon technology can benefit from both the maturity of silicon technology and the outstanding electronic, optical, thermal and mechanical properties of graphene. [1-9] However, the high temperature growth of graphene monolayers is not compatible with silicon processing. [9-11] For these reasons, the controlled transfer of graphene from its growth surface onto target substrates is crucial for developing graphene nanotechnology. The transfer of graphene remains a substantial hurdle and there are no facile processes that enable automated transfer integration with rigid silicon substrates.

Despite the intensive body of research that has been conducted in the past few years on wafer-scale growth of graphene, there are no general and robust approaches for transferring large-area graphene onto silicon wafers. Several methods have been reported for transferring graphene and other two-dimensional (2D) materials onto target substrates including the wet lift-off process using poly(methyl methacrylate) (PMMA) sacrificial layer,[10] the wedge transfer of nanostructure,[12] electrochemical delamination,[13, 14] mechanical delamination with double cantilever beam specimens,[15, 16] and the roll-to-roll transfer of graphene using thermal adhesive. [17, 18] The existing transfer methods, often developed for specific applications and not suited for integration with rigid wafer-scale silicon, suffer from drawbacks such as long process times and the use of reactive chemicals for etching the growth substrate and therefore unwanted contamination and film wrinkling.[19]

The current CVD technique used for growing graphene on metal catalysts is based on a high temperature process (>800 °C). Due to incompatibility of this high temperature process with silicon-based semiconductor workflow, CVD graphene needs to be transferred to another silicon substrate. The most mature technique demonstrated in the literature so far is transferring graphene using PMMA-stamps. The PMMA technique, which has its own merits and can take up to several hours, cannot be used for batch transfer processes and requires a high-temperature step (T > 200 °C) for baking and removing the PMMA stamp from graphene. Here we propose a technique for transferring graphene within few minutes at T < 60 °C (temperature required for baking the epoxy). Importantly, the PMMA based approach is recognized to be a manual method with no clear path for automation unlike the current work where the delamination transfer can be automated and the transfer itself is essentially instantaneous.

In this article, we demonstrate two approaches to low-temperature and scalable direct delamination of graphene from copper films onto silicon substrates with significantly minimal metal contamination on the transferred graphene films. These are developed based on fracture mechanics concepts and selective mechanical delamination, allowing delaminating interfaces selected by controlling the loading rate and direct measurements of the interface adhesion energy.

The CVD growth of graphene on inexpensive and widely available copper foils, while having great potential for roll-to-roll or flexible technology, as shown by multiple papers published by Samsung [17] is not compatible with the silicon CMOS integration process due to the lack of mechanical rigidity of copper foils. On the other hand deposited thin copper films on standard oxidized silicon substrates offer a greater integration possibility for silicon-graphene electronics. The appropriate copper film thickness was determined in our previous work[20].

Graphene was grown on copper thin films that had been deposited on thermally grown silicon oxide by chemical vapor deposition (CVD). The graphene was then bonded to a silicon backing layer by an epoxy in a double cantilever beam (DCB) configuration. A series of experiments conducted at different applied displacement rates revealed two distinct delamination modes. We observed that lower loading rates resulted in direct delamination along the interface between graphene and copper, whereas higher rates gave rise to separation between copper and silicon oxide. The use of separation rate to select a particular delaminating interface had a reliability of about 70%; but once this was achieved, the transfer of graphene on any individual sample was complete. The adhesion energy of the graphene/copper and copper/silicon oxide interfaces was 1.54±0.07 J/m^2 and 1.74±0.14 J/m^2, respectively. The strength and range of the adhesive interactions between graphene and copper film and copper and silicon oxide were determined by nonlinear fracture mechanics concepts. The copper ion contamination on graphene obtained by the direct delamination method was measured by secondary ion mass spectroscopy (SIMS) and was as low as 10^{10} atom/cm^2, nearly 3 orders of magnitude smaller than what was measured for graphene transferred by wet PMMA-assisted process. This low concentration of copper contamination is crucial for achieving high performance graphene devices and reducing contamination for future back-end-of-the-line integration with silicon devices.[21]

EXPERIMENTAL

Graphene Deposition

The graphene synthesis procedure was carried out in an AIXTRON BM CVD system with a cold-wall chamber and a substrate and a showerhead heater setup at ~900 °C. The growth substrates consisted of approximately 900 nm e-beam deposited copper film on commercially

available 300 nm thermally grown silicon oxide on a silicon (100) wafer. The graphene growth process includes 2 minutes of annealing (H_2 ambient, flow rate 1000 sccm, pressure 25 mbar) and 5 min of growth (CH_4 ambient, flow rate 10 sccm).

Graphene Characterization

The quality of graphene grown on copper film by CVD was verified by SEM, Raman mapping, and AFM. The SEM image (Fig. S2a) identifies relatively small copper grains (about 10 μm), resulting from the high temperature growth conditions (approximately 900 ˚C) and slow cooling to room temperature. In addition, ridges within the copper grain can be observed. This ridging only occurs when graphene is present and has an RMS roughness of 10-15 nm, similar to that noted for graphene grown on copper foil.[22] Interestingly, although graphene was present, it is not wrinkled in this image. This should not be taken to imply that the mechanical transfer of the graphene removes wrinkling. However, because the epoxy conforms so well to the morphology of the graphene-coated copper film, it is unlikely that any additional wrinkling was induced by this transfer process. The Raman mapping data (Fig. S2b) for the ratio I_{2D} / I_G of the intensities of the 2D and G bands was greater than 2.6, thereby confirming the presence of high quality, monolayer graphene on the copper film. The AFM was used to examine (Fig. S2c) the surface roughness following graphene growth. The RMS roughness was approximately 60 nm over 50×50 □m.

Delamination Experiment

The graphene coated wafers were cut into 1×4 cm strips and bonded to bare silicon (100) strips of the same size using an epoxy (Fig. S3). The specimens were separated in a universal testing machine at various applied displacement rates (Fig. S1). Details of the graphene transfer

diagnostics and nonlinear fracture analyses are provided in Figure S4 and the section "Finite Element Analysis.

Sheet Resistance

The two- and four-probe structures were fabricated by coating the delaminated graphene with 200 nm thick PMMA film (MicroChem 450-PMMA A4) and e-beam lithography. The graphene channels were isolated by oxygen plasma etching (200 mBar, 50 W) for 50 seconds. The source/drain pads of 3 nm of Ti and 47 nm of Au were deposited by electron-beam metal deposition followed by a lift-off process (Fig. S8).

Transistor Device Characterization

After the graphene was transferred onto epoxy on silicon substrates via the dry transfer technique, drain and source contacts were formed on the graphene by e-beam deposition of 6-nm Ti and 100-nm Au on graphene through a shadow mask. An ionic liquid, 1-Butyl-3-methylimidazolium tetrafluoroborate ($BMIMBF_4$) (98.5% from Fluka), was employed as a top gate method to probe the transistor behavior of the graphene channel on a Cascade® probe station at ambient with Agilent® 4156 analyzer. As a reference, an equivalent transistor device was made from PMMA-assisted graphene channels.

Copper Contamination

The samples were analyzed with a commercial ION-TOF TOF.SIMS [23] instrument configured with a 30 keV Bi^+ analysis ion beam and 1 keV O_2^+ sputtering ion beam. The sputter beam was rastered over 350×350 μm and the analysis beam over 200×200 μm to eliminate crater-edge effects in the collected ions.

By collecting a profile from a reference Cu thin film, a reference intensity of Cu^+ counts with a known concentration was obtained which was later compared with the transferred

graphene films which have trace Cu contamination by the external reference standard method.[23] Using Equation (1), the metal concentration of the analyzed sample (C_A) with respect to the metal concentration of the reference sample (C_R) is calculated:

$$\frac{I_A}{I_R} = \frac{C_A}{C_R} \quad (1)$$

Where I_A is the intensity of secondary ion signal of the analyzed sample and I_R is the secondary ion signal of the reference sample, and that the signal is from the same ion species (Cu^+ in this case). Given the Cu^+ depth profiles, the Cu^+ secondary ion signal intensity corresponding to the graphene layer is fitted at the precise depth. [23, 24]

Results and Discussion

The graphene was grown on 1×4 cm strips using a previously reported CVD growth technique.[8] Each strip was bonded to a bare silicon strip of the same dimensions using a low viscosity epoxy (EP30, Master Bond, Inc.) (Fig. S3), which was cured at 100 °C for two hours. These silicon/copper/graphene/epoxy/silicon laminates were then delaminated in a double cantilever beam configuration (Fig. S1) under displacement control while the load and crack length were measured. A series of experiments were conducted over a range of applied displacement rates. Examples of the fracture surfaces for applied displacement rates of 20, 34, 42 and 50 μm/s are shown in Figure 1a. Direct delamination (Fig. S1a) of graphene from copper was achieved for all the samples tested at the lowest displacement rate. On the other hand, all the samples that were tested at the highest rate completely delaminated along the interface between the copper and silicon oxide (Fig S1b). In this case, the graphene layer can be exposed by

etching away the copper film. We observed that at 34 μm/s, delamination along the graphene/copper interface was dominant, with patches of copper remaining on the graphene. When the loading rate was increased to 42 μm/s, delamination initiated along the graphene/copper interface and then branched to the copper/silicon oxide interface in all samples. The presence of graphene on the epoxy was confirmed by Raman spectroscopy (Fig. 1b) at 20, 34 and 42 μm/s (spots a-c). Of course there was no graphene on the copper that had separated from the silicon oxide (see spots d and e).

Two load-displacement responses of specimens delaminating along the interface between the copper and silicon oxide at an applied displacement rate of 50 μm/s are shown in Figure 2a. In the first case (1), the displacement was applied continuously until the delamination had propagated to the end of the specimen. The load increased to approximately 3.1 N until the delamination initiated, causing the load to drop as the delamination grew. In the second case (2), the initial crack was much longer, which led to a lower initial slope or stiffness (2-1) in the response. However, this time, the specimen was unloaded after a small amount of delamination and then reloaded (2-2). The loading/unloading cycle was repeated (2-3) it allows for several measurements of the adhesion energy to be obtained from with atomically sharp cracks. It is interesting to note how consistent the adhesion energy, which controls the decaying load response, was between cases 1 and 2 as well as within case 2.

The resistance to delamination for both cases was captured in Figure 2b by the J-integral as a function of the growth in delamination Δa. The latter was determined by the stiffness of the load-displacement response using simple beam theory, which properly modeled the slope of the load-displacement response. It was also used to determine the J-integral through $J = \frac{12a^2P^2}{Eb^2h^3}$

using the measured load P and delamination length a at any time. The Young's modulus E was taken to be the in-plane value (129 GPa) for the Si(100) orientation of the silicon strips. The width w and thickness h of the silicon strips were, respectively, 10 mm and 520 μm (nominal). The resistance to delamination rose steeply before transitioning to a steady state value of 1.74 ± 0.14 J/m^2.

A more detailed numerical stress analysis was conducted to determine the strength and range of the interaction between copper and silicon oxide (see Supplementary information for finite element analysis). The analysis considered the linearly elastic behavior of the silicon and silicon oxide (Table S1). The elastic-plastic behavior of the copper was determined from an indentation experiment where a bilinear relation was established for the stress-strain behavior. The behavior of the epoxy was modeled as being elastic-plastic with strain hardening following the approach outlined elsewhere.[22] The interaction between the copper and the silicon oxide was represented by a bilinear traction-separation relation (Fig. S4a) whose parameters are summarized in Table 1. The area underneath the traction-separation relation is the intrinsic adhesion energy, which turned out to be the steady state adhesion energy obtained from beam theory above. This level of adhesion energy provided good agreement with the descending portions of load-displacement responses of the specimen (Fig. S4b). The fact that the intrinsic and steady state adhesion energy was the same indicated that the amount of plastic dissipation from the copper and epoxy was negligible. A parametric analysis revealed that an adhesion strength of 5 MPa provided the best fit to the load-displacement response (Fig. S4b) of the first cycle, further confirming the absence of significant plasticity effects because the 25 MPa yield strength of the copper. The corresponding interaction range was 696 nm. The strength and interaction range had to be modified to 1 MPa and 3.48 μm in order to capture the load-

displacement response of the second cycle. The interaction between silicon and copper is known to be weak as indicated by the use of adhesion promoting layers for copper and silicon in microelectronics packaging. The interaction range is relatively long and clearly contributed to the adhesion energy being much higher than is usually attributed to van der Waals forces, suggesting that other interaction mechanisms were at play. An AFM image of the silicon oxide fracture surface is shown in Figure S5. The nano scale features, which are reminiscent of caldera, were formed during the high temperature deposition of the graphene.[24] From energy dispersive x-ray spectroscopy (EDS) analysis, no signs of copper were found on the fracture surface. This indicates that, in spite of the roughness, the copper cleanly separated from the silicon oxide. The RMS roughness of the fracture surfaces was approximately 5.15 nm, which is two orders of magnitude smaller than the interaction range and an unlikely contributor to the intrinsic toughness. Other interactions and/or roughness effects will need to be considered in future studies.

The two fracture surfaces of a specimen are shown (Fig. 2c) alongside a ruler for scale. The delamination ran from right to left, leaving a region of bare silicon (right) and a region copper on graphene and epoxy (left) on the upper fracture surface and a region of graphene on copper (right) and thermally grown silicon oxide (left) on the lower fracture surface. The inset is a magnified SEM view of the small transition region on the upper fracture surface where the delamination initiated along the graphene/copper interface (dark region) before branching down to the interface between copper and the thermally grown silicon oxide layer. The dark region was due to the presence of monolayer graphene on the epoxy as confirmed by the Raman ($\lambda = 488nm$) spectrum (Fig. 2e) with a deconvoluted intensity ratio I_{2D} / I_G of 1.9 between the

2D and G bands. The SEM image also reveals the grain structure of the copper with grains ranging from 10 to 50 μm.

The details of the circumstances surrounding the experiments conducted at the lowest applied displacement rate of 20 μm/s are presented in Figure 3. As discussed above, in this case, the delamination occurred along the interface between graphene and copper, thereby effectively transferring the graphene to the epoxy layer. The load-displacement responses of two of the samples are shown in Figure 3a. In each case, the delamination growth was initially very unstable. Compared to the response shown in Figure 2a, the sharp drop in the load following the peak suggests a sudden event. This may have been due to the fact that the crack had to break through the graphene from the initial blunt crack or bimaterial corner formed by the epoxy terminus and the graphene. As a result of this instability, the resistance curves (Fig. 3b) were also somewhat unusual. In the first case (1), the amount of unstable crack growth was so much that the energy available for further delamination dropped below the steady state value. Subsequent increases in the applied displacement increased the J-integral to the steady state value of 1.54 ± 0.07 J/m^2. In the second case (2), the amount of unstable crack growth was less and the J-integral converged to the same steady state value from above. A more detailed numerical stress analysis was conducted to determine the strength and range of the interaction between graphene and copper. The strength and range of the interactions between graphene and copper were 5 MPa and 616 nm, respectively (Table 2). The value of the adhesion energy was almost twice the value reported previously. [15] In the previous study, the graphene was grown [25] at 725°C using a inductively coupled plasma (ICP), which led to an RMS roughness of 20-30 nm. In the present study, the growth temperature was approximately 900°C and the RMS roughness was 74 nm (Fig. S6). The most likely cause is the difference in the roughness of the copper film in each

case. The method used for depositing copper film (sputtering, e-beam, atomic layer or electrochemical deposition, etc.) and the initial thickness of the copper film may make an even bigger impact on the final roughness of copper. In addition, the gas precursor used for growing graphene was C_2H_2[15], whereas CH_4 was used here. This may also affect roughness in the sense that different precursors may allow lower processing temperatures, thereby reducing roughness. In another report, [26] where the effect of UV/ozone treatment on the graphene/copper interface was considered, the adhesion energy between graphene and copper film was enhanced from approximately 1.1 J/m^2 without treatment to 2 J/m^2 after treatment.

The AFM scans of graphene grown on copper (Fig. S6a) and the fracture surface with graphene on epoxy (Fig. S6b) revealed very similar RMS roughness values because the low viscosity epoxy was able to conform to the copper surface during specimen fabrication. It was even able to follow the smaller ridge-like feature on the copper grains. When graphene delaminated from copper foil, [22] the intrinsic adhesion energy was 6 J/m^2, with a strength of 3 MPa and interaction range of 4 μm. Once again, the amount of plastic dissipation was small (< 7%) and the high toughness was attributed to the RMS roughness (approximately 1.36 μm over 1×1.3 mm), which was the largest of three distinct roughness scales and commensurate with the interaction range. Thus it is surprising that the interaction range of 616 nm obtained in the present study does not appear to correlate with the RMS roughness. At the same time it is not clear what other interaction mechanism has such a range, so this will be a matter for future study.

Images of the fracture surfaces are shown in Figure 3c. The upper fracture surface consists of bare silicon on the right and graphene transferred on epoxy on the left. Correspondingly, the lower fracture surface consists of the graphene that had been deposited on the copper film on the right and bare copper on the left. The boundary between the two regions,

which corresponds to location of the epoxy terminus, is indicated by the red line. The SEM image of the graphene on epoxy (Fig. 3d) indicates how well the low viscosity epoxy (EP 30, Master Bond) was able to replicate the grain structure of the copper. There is no charge accumulation effect on the epoxy surface, suggesting a uniform graphene coverage. A Raman spectrum taken in the same region confirmed the presence of graphene. The intensities of the G and 2D peaks was reversed due to the background spectrum of the epoxy.[27] The deconvoluted peak intensity ratio was 2.1, thereby indicating that monolayer graphene was successfully transferred to the epoxy. An SEM image of the bottom fracture surface that spanned the epoxy terminus is shown in Figure 3e. The slightly darkened region corresponds to the presence of graphene on copper with the underlying grain structure of the copper still visible. The lighter region is bare copper, so this image further emphasizes the transfer of graphene from the seed copper to the epoxy. Raman spectra were taken at spots (a) and (b) on the graphene-coated and bare copper, respectively. The signature of monolayer graphene, G and 2D peaks with an intensity ratio of 1.76, is clearly visible at (a). There were no such peaks at (b), further confirming the successful transfer of graphene.

The experiments have clearly demonstrated that it is possible to cause the sandwich specimens to delaminate along the copper/silicon oxide or the graphene/copper interface. Both scenarios are useful for nanomanufacturing processes. For example, direct separation along the graphene/copper could be immediately incorporated in a multi-step process. On the other hand delamination along the copper/silicon oxide interface allows the copper to protect the graphene during post-transfer processing and fabrication. The graphene/epoxy interface has been shown to be rate-dependent [15, 22] but it was not involved in either of the delamination mechanisms that were observed here. This leaves open the possibility that one or both of the interfaces

(copper/silicon oxide or the copper/graphene) are rate dependent, although the mechanism for such behavior remains to be investigated.

To investigate the electrical properties of the transferred graphene, two and four-probe devices were fabricated and used for measuring the sheet resistance (R_{Sheet}) of graphene. The schematic of the fabrication process is shown in Figure 4 and in more detail (Fig. S8). In the case of the delamination along copper and silicon oxide surface, the copper film was first etched in ammonium per sulfate (APS-100) solution diluted with DI water (1:1) and rinsed with DI water subsequently before the fabrication process. Low-power oxygen plasma was used for isolating the graphene channels and Ti/Au (3 nm/ 47 nm) were deposited as the source and drain contacts. Raman maps (Fig. 4 e-g) and a deconvoluted spectrum (Fig. 4h) taken of the graphene channels confirmed that monolayer graphene was present. Figure 5 compares the R_{sheet} of the graphene, obtained by this technique, to the sheet resistance data reported for graphene transferred by PMMA wet-transfer process and by electrochemical transfer method on flexible substrates. [9, 14] An average sheet resistance of 3.1 kΩ/sq and 4.7 kΩ/sq was observed for graphene obtained by direct delamination from copper and from the graphene/copper stack obtained by delamination from the silicon oxide substrate. This is about 1.5 and 2.5 times larger than the value reported for graphene transferred with PMMA layers. This could be due to reduced impurity contamination from the dry transfer process or the larger roughness of mechanically transferred graphene (RMS~ 70 nm) that causes stronger carrier scattering. On the other hand, the variation of the sheet resistance of the mechanically-delaminated graphene is ~3-5 times smaller compared to the standard PMMA-assisted technique, suggesting that the transferred monolayer possesses more uniform electrical properties. Note that contamination during PMMA assisted wet-transfer can be

reduced by adding a modified RCA* cleaning step. [28] The reason could be lower levels of metal contamination caused by the dry transfer process as mentioned earlier. To validate this hypothesis, the copper contamination left on graphene during different transfer processes was evaluated with time-of-flight secondary ion mass spectroscopy (TOF-SIMS) technique (Fig. 6 and see description of measurements of copper contamination in supporting information). The copper contamination on a silicon sample capped with 300 nm thermally grown silicon oxide which was not exposed to the copper was used as the reference. An area of 200 μm × 200 μm was evaluated for copper contamination on graphene samples transferred by the direct delamination, delamination of graphene/copper and PMMA-assisted techniques. The results shown in Figure 6 show copper contamination on graphene transferred by the PMMA-assisted technique is 4-5 orders of magnitude higher than the reference silicon oxide sample and 2-4 orders of magnitude higher than the contamination level left on graphene transferred by either of the delamination techniques. The ~10^{14}atoms/cm^2 copper contamination of graphene by wet transfer is consistent with previous wet transfer studies on graphene. [19] This suggests that mechanical delamination results in very low copper contamination on graphene and comparable to the reference silicon oxide sample.

Figure 7a shows the charge transport characteristics of a representative transistor fabricated from mechanically delaminated transferred graphene over a range of drain voltages. A symmetric bell-shaped curve (Fig. 7b) of the normalized resistance versus gate bias voltage was extracted from drain current versus gate bias at $V_d = 20$ mV with a nearly zero Dirac voltage and a gate modulation (ON/OFF ratio) greater than three-fold. This indicates minimal external doping of the graphene surface obtained from the mechanical delamination transfer method. On

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the other hand, graphene transistors made from the PMMA-assisted transfer method yielded a suppressed electron branch, reduced gate modulation of about 33%, and a significantly shifted Dirac point due to p-doping (Fig. 7b). The transistor characterization is in agreement with aforementioned sheet resistance measurement and TOF-SIMS results, indicating considerably lower levels of contamination in mechanically delaminated transferred graphene in contrast to the traditional PMMA-assisted transfer method.

CONCLUSIONS

In summary, we demonstrated that it is possible to transfer graphene grown on silicon wafers in two ways by controlling the rate at which peeling occurs. Graphene was grown on copper film on a silicon substrate by CVD and then bonded to a second strip using an epoxy. Delamination occurred along the graphene/copper interface when the separation rate was 20 μm/s. As the separation rate was increased, there was increasing evidence of delamination along the copper/silicon oxide interface and at 50 μm/s, delamination was entirely between copper and silicon oxide. Thus it is possible to transfer graphene directly to a polymer substrate or to leave it protected by the copper layer, which could be removed by etching at a later stage in processing. In both cases, the high quality of the transferred monolayer graphene was confirmed by SEM and Raman spectroscopy. Furthermore, it was determined that the sheet resistance of the graphene in both cases was higher than when graphene is transferred to PMMA by wet etching and the variation in the sheet resistance values was much lower, both attributed to reduced impurity and residue contamination. Quantitatively, copper contamination levels as determined by TOF SIMS in both cases were orders of magnitude lower than the values for PMMA assisted transfer.

The adhesion interactions between graphene and copper and copper and silicon oxide were represented by traction-separation relations in nonlinear fracture analyses of the delamination experiments. The adhesion energy of the graphene/copper and copper/silicon oxide interfaces were 1.54 and 1.74 J/m^2, respectively. In both cases, the strengths were the same at 5 MPa but the interaction range of the graphene/copper interface was 616 nm as opposed to 696 nm for the copper/silicon oxide interface. Such values are not commensurate with Van der Waals interactions, as might be expected, so further examination is required to identify the separation mechanism, which is likely to involve the roughness of the graphene/copper interface.

The RMS roughness of the interfaces produced in this study was 70 nm. Minimizing this roughness by novel processing steps or choices of other seed metals, particularly platinum, would increase the smoothness and uniformity of the transferred graphene. It would also reduce the adhesion energy, thereby providing a wider margin in separation rates. The dry transfer method developed in this work for graphene is expected to be applicable to other two-dimensional materials including hexagonal boron nitride and transitional metal dichalcogenides.

Acknowledgements

The authors gratefully acknowledge the financial support of this work by the National Science Foundation through Grant No. EAGER 1444398. This work is also based upon work supported in part by the National Science Foundation under Cooperative Agreement No. EEC-1160494. Any opinions, findings and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the National Science Foundation.

Footnotes

[††]Electronic supplementary information (ESI) is available.

Tables

Table 1. Values of the parameters in the traction-separation relations associated with the interface between copper and silicon oxide

	TSR 1	TSR 2
Γ_{ss} (J/m^2)	1.74	1.74
K (MPa/mm)	10^6	10^6
σ_0 (MPa)	5	1
δ_n^c (nm)	696	3480

Table 2. Values of the parameters in the traction-separation relation associated with the interface between graphene and copper

	TSR 1
Γ_{ss} (J/m^2)	1.54
K (MPa/mm)	10^6
σ_0 (MPa)	5
δ_n^c (nm)	616

Supporting Information Available

The following information is available for readers:

- Delamination modes of the double cantilever beam specimen at different rates
- Quality of graphene grown on copper film
- Fabrication of double cantilever beam samples
- Finite element analysis
- Morphology of silicon oxide
- Morphology of graphene on copper and graphene on epoxy
- Raman response of pure epoxy and graphene on epoxy
- Procedures for device fabrication with transferred graphene or graphene/copper

This material is available free of charge via the Internet

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Figures

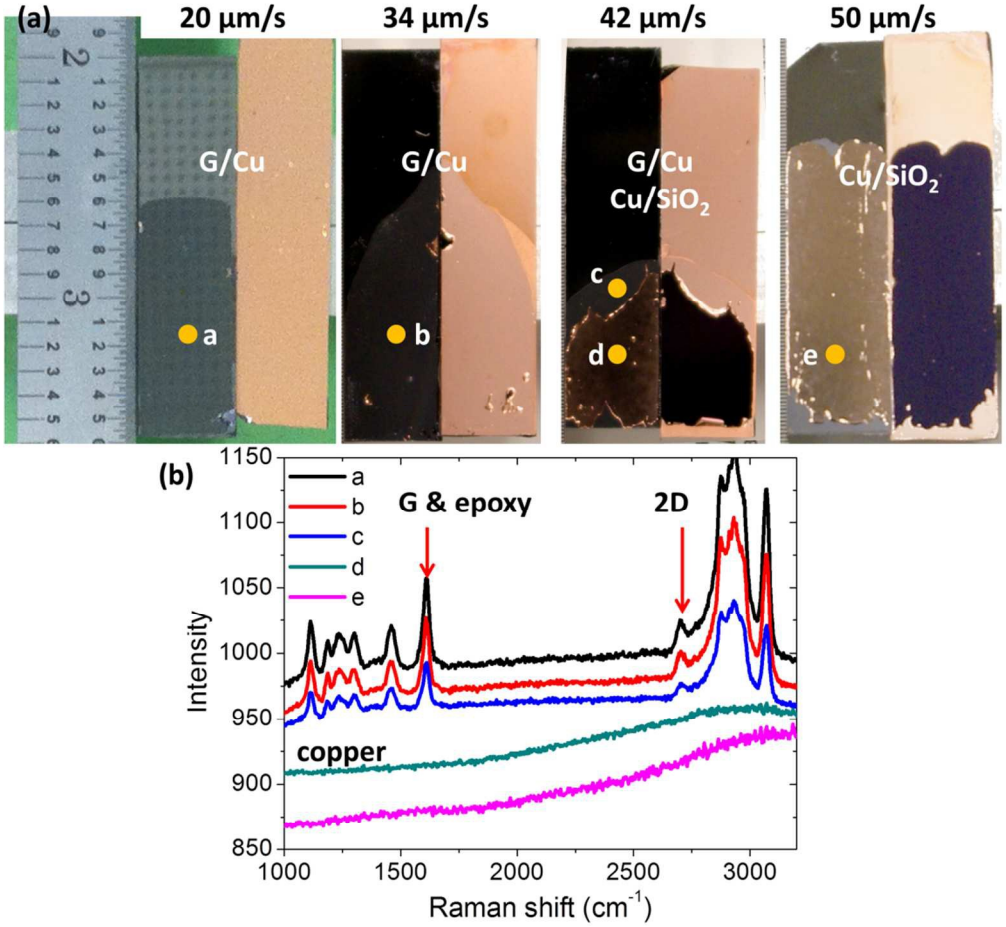

Figure 1. Low resolution images of the fracture surface and associated Raman spectra: (a) rate dependence of the fracture modes and (b) Raman spectra. Note that the pattern on the bare silicon portion of the fracture surface (20 µm/s) is a reflection of ceiling tiles.

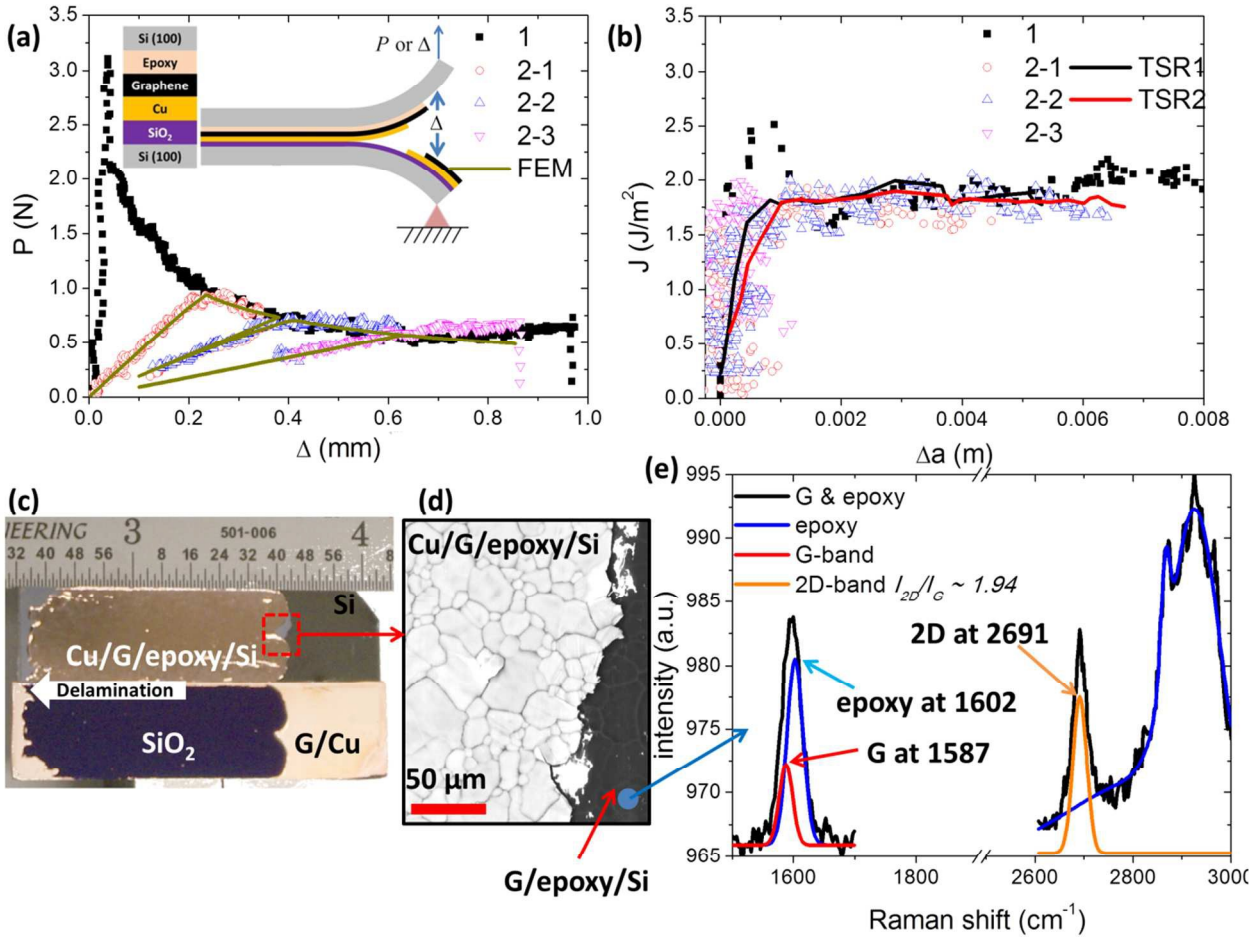

Figure 2. A summary of results obtained at an applied loading rate of 50 μm: (a) Measured and simulated force-displacement responses, (b) Measured and simulated delamination resistance curves for the copper/silicon oxide interface, (c) Low resolution images of the fracture surfaces, (d) high resolution SEM image of the boxed region in (c) and (e) Raman spectrum from the spot in (d) with background data and deconvoluted signals for pure graphene and epoxy.

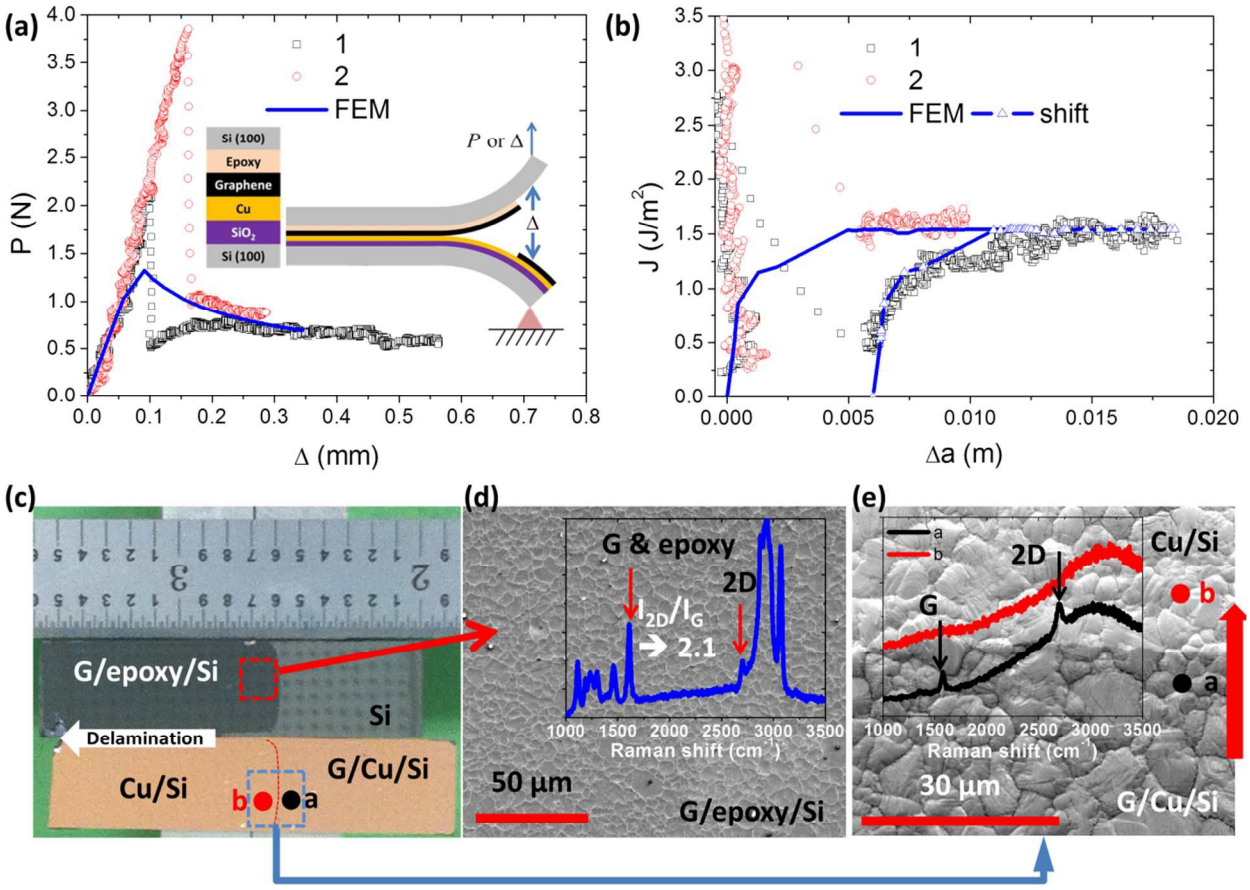

Figure 3. A summary of results obtained at an applied loading rate of 20 μm: (a) Measured and simulated force-displacement responses, (b) Measured and simulated delamination resistance curves for the graphene/copper interface, (c) Low resolution images of the fracture surfaces, (d) high resolution SEM image of and Raman spectrum from the red boxed region in (c) and (d) high resolution SEM image of and Raman spectra from the blue boxed region in (c). Note that the pattern on the bare silicon portion of the fracture surface (c) is a reflection of ceiling tiles.

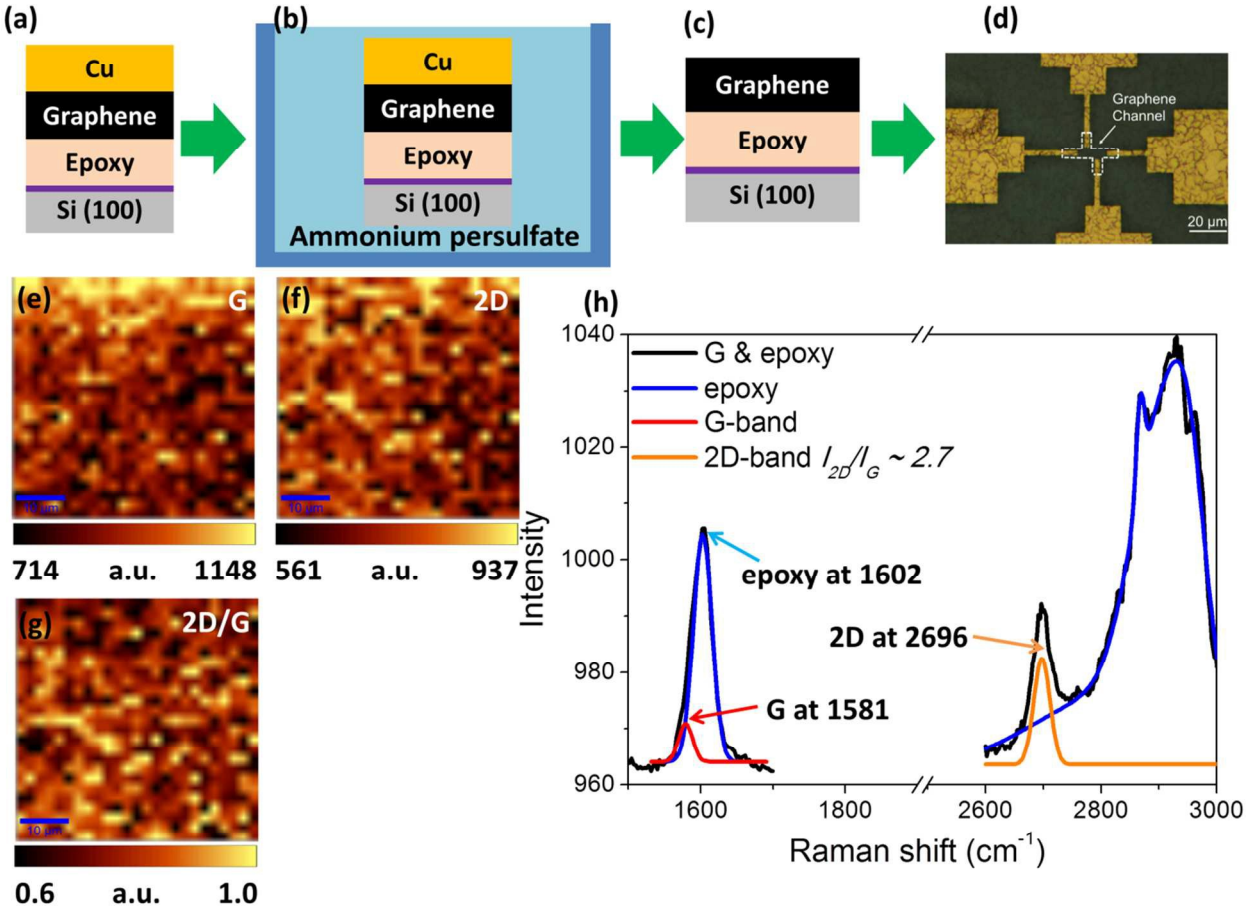

Figure 4. Procedures for device fabrication and surface characterization: (a) graphene and copper transferred to epoxy due to delamination between copper and silicon oxide, (b) copper is etched away in an ammonium persulfate solution, (c) remaining graphene on epoxy or directly transferred graphene on epoxy by delamination between graphene and copper, (d) a device with a graphene channel, (e) Raman G peak maps over 50×50 μm regions, (f) Raman 2D peak maps over 50×50 μm regions of the on the graphene channel, (g) a map of the ratio of the intensities (I_{2D}/I_G), which is less than one due to the presence of a strong epoxy peak at 1602 cm^{-1}, and (h) deconvoluted G and 2D peaks that exhibit a 2.7 intensity ratio proving the presence of monolayer graphene on epoxy.

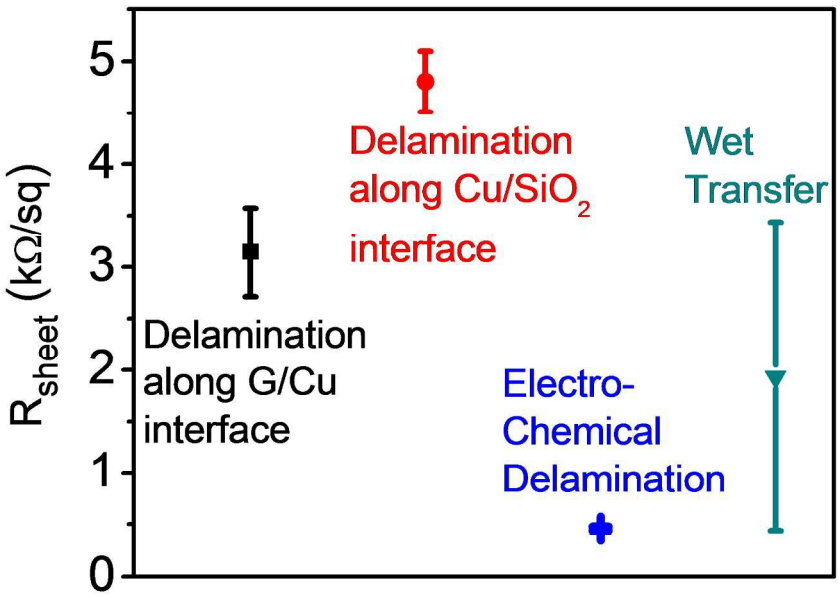

Figure 5. The sheet resistance of graphene transferred by mechanical delamination, PMMA-assisted wet transfer and electrochemical delamination.

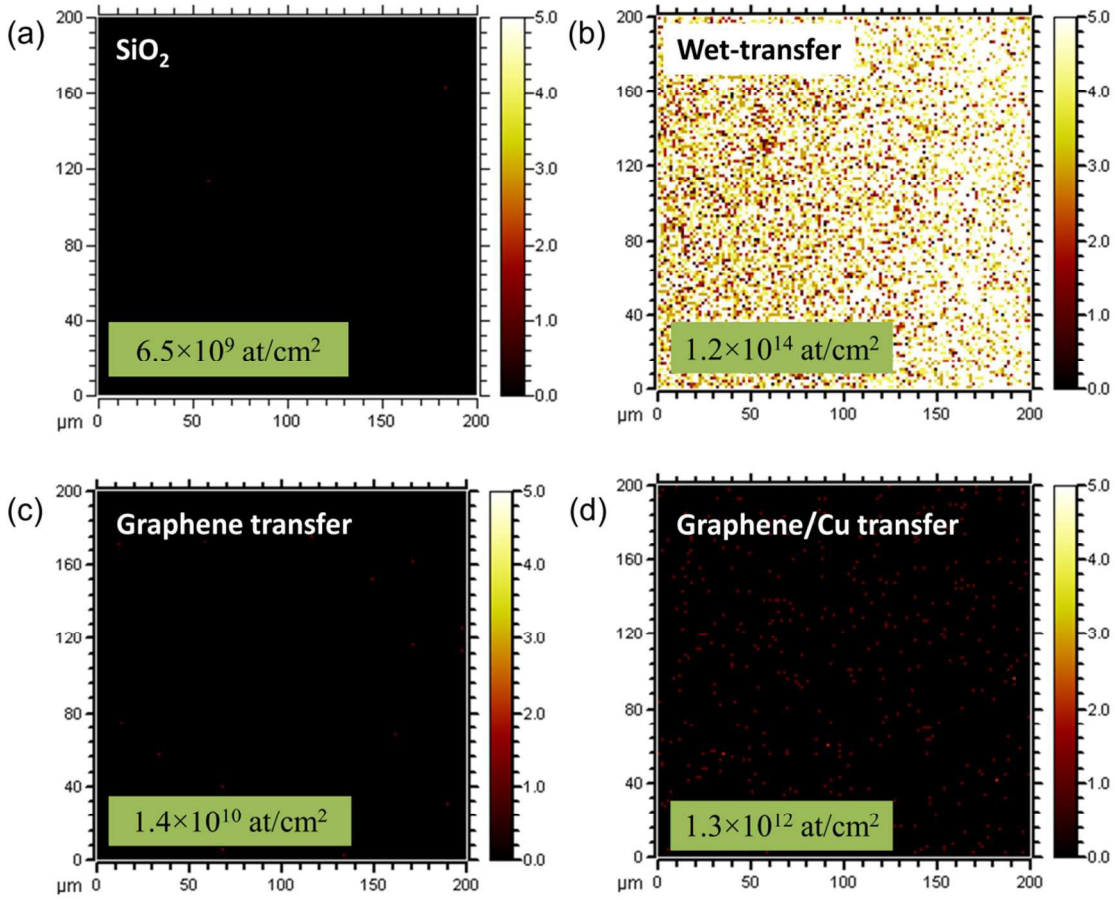

Figure 6. TOF-SIMS analyses (200 ×200 μm) of copper contaminants on: (a) silicon oxide, (b) PMMA-assisted transferred graphene on silicon oxide, (c) directly transferred graphene, and (d) directly transferred graphene and copper, which was etched away.

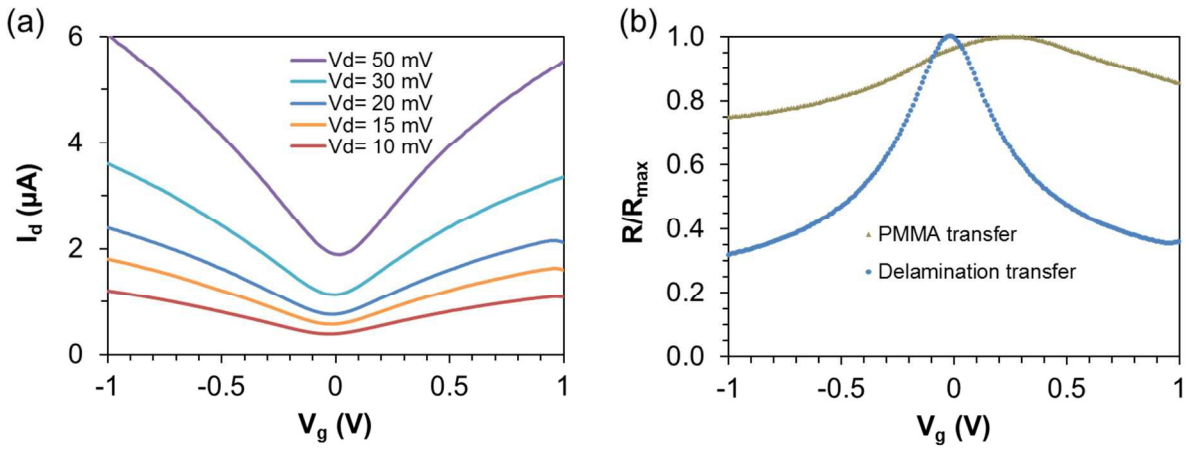

Figure 7. The electrical characterization of a) drain current versus gate voltage curves of an ionic liquid gated transistor made from mechanically delaminated transferred graphene channel. The Dirac point is at almost zero voltage; b) total channel resistance over maximum channel resistance versus gate bias voltage from two ionic liquid gated transistors, one with mechanical delamination and the other with PMMA transferred graphene. A symmetric bell-shape curve with ON/OFF ratio ~3.14 was observed on mechanical delamination transferred graphene, whereas PMMA-assisted graphene channel exhibited a reduced gate modulation ~1.33.