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Journal Name

ARTICLE

Two-dimensional molybdenum disulphide nanosheets covered metal nanoparticle array as floating gate in multi-functional flash memories

Received 00th January 20xx,
Accepted 00th January 20xx

DOI: 10.1039/x0xx00000x

www.rsc.org/

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Semiconducting two-dimensional materials have appeared to be excellent candidates for non-volatile memory application. However, the limited controllability of charge trapping behaviors and lack of multibit storage study in two-dimensional based memory devices require further improvement for realistic application. Here, we report a flash memory consisting of metal NPs-molybdenum disulphide (MoS₂) as a floating gate by introducing metal NPs (Ag, Au, Pt) monolayer underneath the MoS₂ nanosheets. Controlled charge trapping and long data retention have been achieved in metal (Ag, Au, Pt) NPs-MoS₂ floating gate flash memory. This controlled charge trapping is hypothesized to be attributed to band bending and built-in electric field ξ_{bi} between the interface of metal NPs and MoS₂. The metal NPs-MoS₂ floating gate flash memories were further proved as multibit memory storage device possessing 3-bit storage capability and a good retention capability up to 10⁴ s. We anticipate these findings would provide scientific insight for the development of novel memory devices utilizing atomically thin two-dimensional lattice structure.

Introduction

The memory for internet of things (IoT) desires a versatile distinctiveness such as wear-ability, flexibility, multi-functionalities including tunable electrical properties and stability in outdoor environments. Flash memory coupled with simple device architecture and functional materials with good flexibility can be a gorgeous candidate for IoT memory. Flash memory transistor is one kind of the basic element in the design of a large-scale integrated circuit.¹⁻³ Integration of multi-functionalities including controlled charge trapping and multi-bit storage into floating gate flash memory platforms have been considered as an alternative solution for the future scaling down the logic circuits beyond the Moore's law. Control over charge trapping can be understood as acquiring large range of tunable threshold voltages (V_{th}).^{4,5} To construct an integrated circuit, it would be anticipated to have large range of controllable V_{th} to implement logic function.⁶ On the

other hand, storage density is one of the issues. Is it possible to obtain high data density with rapid scaling down of logic circuits? Low-cost memory architecture for much cheaper solid-state drives with improved storage density is the most preferable way for IoT.⁷ Creating multibit data storage memory device is one of such efforts to obtain a higher storage density.⁸⁻¹¹

To obtain a wide range of controllable V_{th} to implement the logic function with multi-bit storage functionalities, two dimensional (2D) materials are one of the choices. On this aspect, graphene has been used with proper energy band engineering.⁴ However, to overcome the limitation of zero-bandgap graphene, the semiconducting nature of MoS₂ offers several attracting properties such as excellent electrical properties, high flexibility and transparency.¹²⁻¹⁹ 2D molybdenum disulphide (MoS₂) exhibits a conversion from 1.3 eV indirect band gap for bulk to 1.8 eV direct band gap for a monolayer.¹⁵ A number of reports have used MoS₂ in non-volatile memory devices including a charge trapping layer, a field-effect transistor (FET) channel and active layer.^{12,20-22} The observed large gate hysteresis under electrical modulation demonstrates that MoS₂ can be employed as a floating gate for flash memory device operation. However, the tunneling injection of carriers is unipolar in which the devices exhibits asymmetry gate characteristics with superior trapping of holes and poor trapping of electrons.¹² The tunability of charge trapping in MoS₂ based flash memory is still hindered largely by the limited control over energy band engineering of MoS₂. The poor controllability over charge trapping behaviors in the

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Electronic Supplementary Information (ESI) available: Energy-dispersive X-ray spectroscopy (EDS) spectra of the metal NPs, SEM image of MoS₂ on Au NPs, erasing operations of metal NPs-MoS₂ memory device, transfer characteristics of the standard FET devices and Ag NPs devices under programming operation, tapping-mode AFM height image of fabricated MoS₂ film for pristine MoS₂ flash memory, gate signals used for programming the Au NPs-MoS₂ and Pt NPs-MoS₂ flash memories, data levels recorded for 100 sequential cycles. See DOI: 10.1039/x0xx00000x

MoS₂ memory devices requires further improvement for the realistic application.

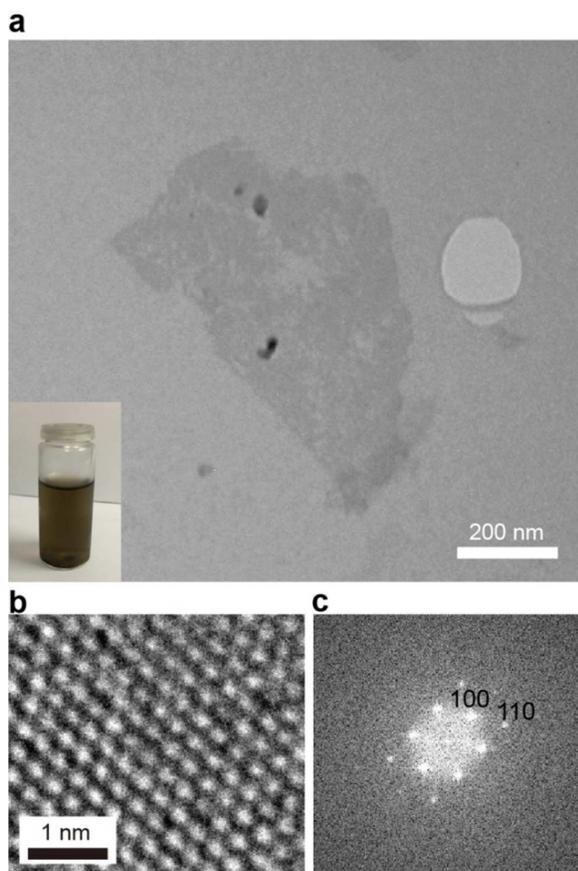


Figure 1. (a) Low magnification TEM image of a typical MoS₂ nanosheet. Inset: Photograph of the electrochemical intercalated MoS₂ nanosheets solution. (b) HRTEM image of single-layer MoS₂ nanosheet. (c) Corresponding fast Fourier transform (FFT) of HRTEM image.

On the other hand, noble metal NPs with chemical stability and high work function have traditionally been the popular candidates for charge trapping in flash memory.²³⁻²⁵ To obtain controlled charge trapping, here we introduce a novel structure consisting of metal NPs (Ag, Au, Pt) of different work function underneath the MoS₂ nanosheets by a simple solution-based method. As additional trapping sites, metal NPs have been used to tune the Fermi level of MoS₂ and to achieve the band bending between the interface of metal NPs and MoS₂. The energy level has effectively been modulated because the charge transfer between the metal NPs and MoS₂ nanosheets is quite significant due to the atomic thickness of the 2D nanoflakes. Such a metal NPs-MoS₂ nanosheets are utilized as floating gate in flash memory which exhibit higher controllability of charge carriers trapping than pristine MoS₂ floating gate alone. The flash memories based on Pt NPs-MoS₂, Ag NPs-MoS₂ display enhanced trapping of holes or electrons respectively while Au NPs-MoS₂ based flash memory shows improved trapping of both holes and electrons. Surprisingly, a longer retention time is also observed in metal NPs-MoS₂ based memory devices. The built-in electric field originated at the interface of metal NPs and MoS₂ nanosheets are

responsible for the efficient charge trapping control and stable retention. Furthermore, long retention of charge carriers and reversible modulation of trapped charge carriers of this structure enable the demonstration of multibit memory device with reliable 3-bit data states. The flash memories presented here show controllable charge trapping and multibit storage that are necessary parameters for further scaling down of logic circuit.

Results and discussion

The controllable electrochemical lithiation process was used to prepare the single-layer MoS₂ nanosheets.²⁶ The low magnification transmission electron microscope (TEM) image in Fig. 1a shows the morphology of a typical MoS₂ nanosheet. The high resolution transmission electron microscope (HRTEM) image of the basal plane of the MoS₂ nanosheets with its corresponding fast Fourier transform (FFT) is displayed in Fig. 1b and 1c. The hexagonal lattice structure with a lattice spacing of 2.7 Å attributed to the (100) planes.²⁷

Recently, the reported methods to introduce metal NPs to the surface of MoS₂ nanosheets are usually through dispersible template-based wet-chemical synthesis.²⁸⁻³⁰ However, the repeated purification process, low yield rate and poor morphology of as-synthesized metal-MoS₂ nanosheets are not compatible with the memory device fabrication. Herein, we present extremely simple stacked structure in which the aqueous MoS₂ sheets solution with proper concentration are directly drop-casted onto the surface of metal NPs monolayer to form metal NPs-MoS₂ floating gate. The transmission electron microscopy (TEM) image of citrate-reduced spherical metal NPs (Ag, Au, Pt) are shown in the inset images of Fig. 2a to 2c. The NPs have a uniform size with average diameter of 5 nm. Energy-dispersive X-ray spectroscopy (EDS) spectra of the NPs (Fig. S1) allow the determination of the chemical composition of the samples. Citrate-reduced metal NPs are attached under electrostatic force onto 3-aminopropyltriethoxysilane (APTES) modified substrate. The metal NPs monolayer film were characterized by field emission scanning electron microscope (FE-SEM) and the images of high quality metal NPs array are shown in Fig. 2a to 2c. The metal NPs are well-dispersed on the substrates without agglomeration due to the repulsive force between each nanoparticle.³¹ Fig. 2d to 2f show AFM images of MoS₂ sheets, covered on the top of the metal NPs monolayer. The MoS₂ sheets fully cover the metal NPs array without deteriorating the surface roughness promising a good interface quality for the device fabrication. The SEM image of MoS₂ on Au NPs is shown in Fig. S2. Fig. 2g show the fabrication details of Metal NPs-MoS₂ floating gate flash memory. Silicon wafers with 100 nm thick SiO₂ layer serve as gate electrode and blocking oxide. After construction of the metal-MoS₂ floating gate, another thin layer of 5 nm aluminum oxide (Al₂O₃) was atomic layer deposited as tunneling oxide. Finally, p-type semiconductor (pentacene) and 30 nm of Au source-drain electrode were thermally evaporated on the top of Al₂O₃.

First, we measure the transfer characteristics curves acquired after programming operation under a fixed drain-source

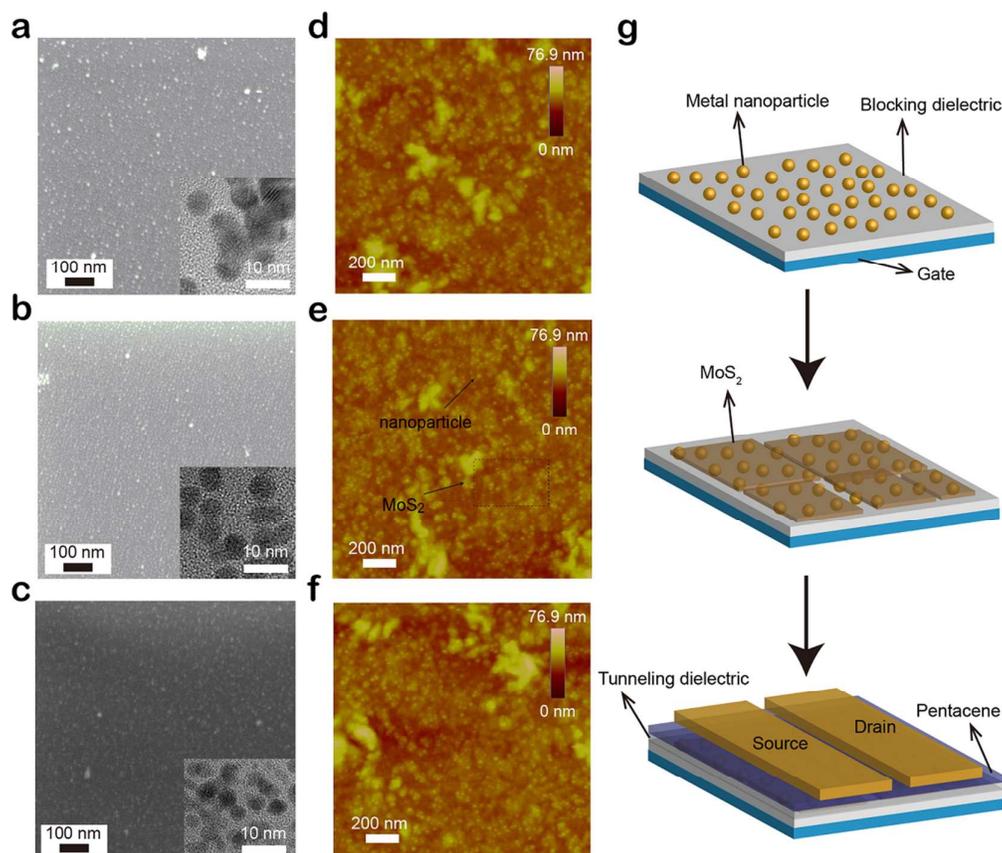


Figure 2. FE-SEM images of self-assembled 5 nm (a) Ag NPs monolayer, (b) Au NPs monolayer and (c) Pt NPs monolayer. Inset: HR-TEM images of corresponding metal NPs. Tapping-mode AFM image of MoS₂ nanosheets self-aligned on the (d) Ag NPs monolayer, (e) Au NPs monolayer and (f) Pt NPs monolayer. (g) Schematic diagram depicting the basic fabrication process of metal NPs-MoS₂ floating gate flash memory.

voltage (V_{DS}) of the flash memory based on pristine MoS₂ floating gate. To confirm the effect of charge trapping in MoS₂, a standard field-effect device without MoS₂ floating gate has also been fabricated. As shown in Fig. 3a, the initial state of V_{th} shifts around 6 V after positive programming operation of +50 V for 1 s (denoted as ΔV_p) and 7 V after negative programming operation of -50 V for 1 s (denoted as ΔV_n). Erasing operation followed by positive or negative programming operation has been carried out to shift the transfer curve to the initial state. These erasing operations to release holes or electrons are discussed in the Supporting information Fig. S3 to S5. The observed mild memory window is due to the underlying MoS₂ since there is no significant V_{th} shift of the standard device as depicted in the Supporting information Fig. S6 and Fig. S7. Direct tunneling and Fowler-Nordheim tunneling are anticipated to be the ways to program devices instead of channel hot electron/hole injection due to low drift velocity prompted by the low mobility pentacene compared with Si-based transistor.^{32,33} Under a low reverse bias, the direct tunneling dominates the carrier transport because the field-induced band bending is not severe. Due to field-induced band bending under a high reverse gate bias, the Fowler-Nordheim tunneling dominates when the tunneling distance of the charge carriers is further reduced.¹⁸ The symmetry of the observed ΔV_p and ΔV_n in pristine MoS₂ flash memory suggests

that the tunneling of the electrons and holes after positive and negative programming operations is symmetric and MoS₂ could act as trapping element of both holes and electrons. This symmetry is due to the similar tunneling barrier height for holes and electrons or a comparable effective mass of holes and electrons in Al₂O₃ ($m_h = 0.25 m_0$, $m_e = 0.2m_0$).³⁴ We subsequently measured the memory characteristics of the metal NPs-MoS₂ floating gate flash memories as shown in Fig. 3b to 3d. The V_{th} of initial state, positively/negatively programmed states, ΔV_p and ΔV_n of flash memories based on Ag NPs-MoS₂, Au NPs-MoS₂ and Pt NPs-MoS₂ floating gates are summarized in Table 1. We also fabricated a control device with only Ag nanoparticle as the floating gate. The control device shows smaller ΔV_{th} compared with the Ag NPs-MoS₂ device as depicted in Fig. S8, proving that both Ag nanoparticle and MoS₂ can work as the charge trapping elements. Asymmetric gate characteristics with Ag NPs-MoS₂ and Pt NPs-MoS₂ floating gate are observed. The Ag NPs-MoS₂ flash memory exhibits more prominent ΔV_p and suppressed ΔV_n , indicating a large electron tunneling probability and low hole tunneling possibility. In contrast, Pt NPs-MoS₂ flash memory shows narrower ΔV_p while wider ΔV_n , suggesting an enhanced trapping ability of holes to provide sufficient gate-field screening after negative programming operation. For the flash memory device based on Au NPs-MoS₂ floating gate, slight

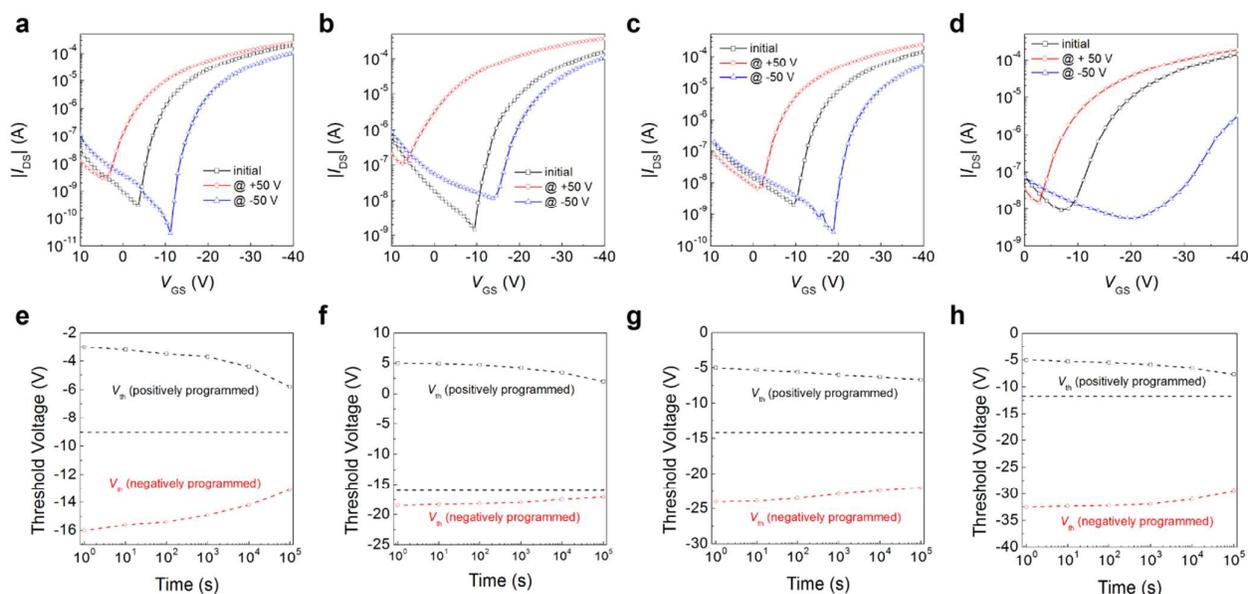


Figure 3. Transfer curves of flash memories based on (a) pristine MoS₂ gate, (b) Ag NPs-MoS₂ floating gate, (c) Au NPs-MoS₂ floating gate and (d) Pt NPs-MoS₂ floating gate at initial state, positively programmed state and negatively programmed state. Retention performance of flash memories based on (e) pristine MoS₂ gate, (f) Ag NPs-MoS₂ floating gate, (g) Au NPs-MoS₂ floating gate and (h) Pt NPs-MoS₂ floating gate. The dotted lines represent the V_{th} value of initial state.

increase in both ΔV_p and ΔV_n can be achieved due to large electrons and holes tunneling current for screening.

The retention capabilities of memory devices are displayed in Fig. 3e to 3h. After the application of gate bias of ± 50 V with pulse width of 1 s, the V_{th} was measured at $V_{GS} = -40$ V and $V_{DS} = -40$ V with respect of elapsed time. Different V_{th} of two states can be defined as V_{th} (positively programmed) and V_{th} (negatively programmed). MoS₂ flash memory exhibits around 45 % charge loss after 10^5 s retention test. Nevertheless, positively programmed state of Ag NPs-MoS₂ flash memory and negatively programmed state of Pt NPs-MoS₂ flash memory could be well maintained up to 10^5 s, indicating that the trapped electron retaining ability of Ag NPs-MoS₂ flash memory and trapped hole reserving ability of Pt NPs-MoS₂ flash memory are significantly enhanced. Additionally, Au NPs-MoS₂ flash memory enables a relatively unambiguous reading of more distinguishable V_{th} value at both positive and negative programmed states based on 10^5 s retention test data.

Fig. 4a shows the energy band diagram of the memory devices in the flat band state without applied bias and contact between layers. The memory effect of MoS₂ memory device is achieved by trapping/releasing the holes/electrons in valence/conduction band of MoS₂. The holes/electrons injection barrier is the difference between the highest occupied molecular orbit (HOMO)/lowest unoccupied molecular orbit (LUMO) level of pentacene and valence/conduction band of MoS₂. The symmetry of the observed transfer curve shift in pristine MoS₂ memory device after positive and negative programming operations is partially attributed to the similar injection barriers of holes and electrons. The qualitative sketch of the ideal energy-band edge after charge carriers' redistribution of the metal NPs-MoS₂

structures is shown in Fig. 4b to 4d. The work function of Ag, Au and Pt are 4.26 eV, 5.1 eV and 5.65 eV respectively. The reported work function and electron affinity of MoS₂ are 5.1 eV and 4.2 eV.^{28,35} In general, the interface is not in electrical equilibrium when the work function for the metals and MoS₂ are not the same.^{36,37} If the total number of the available charge carriers in the MoS₂ is large enough, charge redistribution occurs between the interface within a reasonable short duration and this flow and redistribution of charge carriers continues until the Fermi levels are aligned.³⁶ In the case of Ag-MoS₂ flash memory, the work function of Ag is smaller than MoS₂ which induces the electron transfer from Ag into MoS₂ through a thin interfacial barrier layer and produces a band bending and built-in electric field, ξ_{bi} , directed from Ag toward MoS₂ layer. The enhanced electron trapping and reserving performance of Ag-MoS₂ floating gate is attributed to the presence of large ξ_{bi} . Thus, electrons are easier to be trapped and kept in the Ag NPs for Ag-MoS₂ structure resulting in the larger ΔV_p and longer retention time of V_{th} (positively programmed). In contrast, the electron transfer occurs from high energy states of MoS₂ to Pt in Pt NPs-MoS₂ floating gate interface because the Fermi level of Pt is lower than that of MoS₂ which induces opposite ξ_{bi} , directed from MoS₂ to Pt. Therefore, the holes are easier to be trapped and retained in the Pt NPs, prompting a large V_{th} shift after negative programming operation eventually enhanced holes retaining property. However, there is no such alignment of Fermi level by band bending in Au NPs-MoS₂ interface since the work function of Au and MoS₂ are almost the same. The mild enhancement of memory windows may be ascribed to the introduction of more Au NPs charge trapping sites. It worth noting that the Au NPs-MoS₂ structure exhibits lower degree

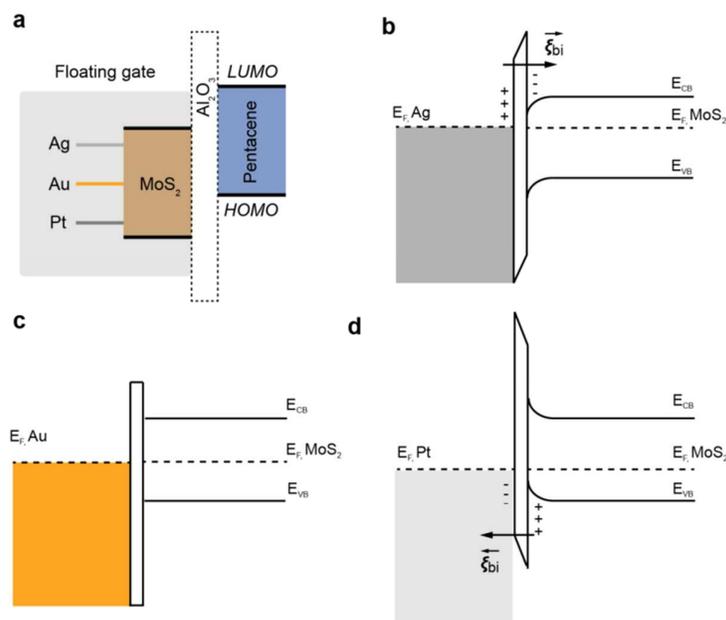


Figure 4. (a) Energy band diagram of flat band state (HOMO: highest occupied molecular orbital, LUMO: lowest unoccupied molecular orbital). Energy band-edge alignment of (b) Ag NPs-MoS₂ structure, (c) Au NPs-MoS₂ structure, (d) Pt NPs-MoS₂ structure (E_F : Fermi energy level, E_{CB} : conduction band edges of MoS₂, E_{VB} : valence band edges of MoS₂, ξ_{bi} : built-in electric field originated from charge carriers flow and redistribution). A thin interfacial layer is inserted between metal and MoS₂ to indicate a nonepitaxial contact.

Table 1. Threshold voltage of initial states, positively programmed states and negatively programmed states, memory windows after positively programming operation and negatively programming operation and charge trapping rates of flash memories.

	V_{th} (initial) (V)	V_{th} (positively programmed) (V)	V_{th} (negatively programmed) (V)	ΔV_p (V)	ΔV_n (V)	(dN_e/dt) ($\text{cm}^{-2} \text{s}^{-1}$)	(dN_h/dt) ($\text{cm}^{-2} \text{s}^{-1}$)
MoS ₂	-9	-3	-16	6	7	1.29×10^{12}	1.5×10^{12}
Ag NPs-MoS ₂	-14	5	-18.5	19	4.5	4.09×10^{12}	9.7×10^{11}
Au NPs-MoS ₂	-14	-5	-24	9	10	1.94×10^{12}	2.15×10^{12}
Pt NPs-MoS ₂	-12	-5	-32.5	7	20.5	1.5×10^{12}	4.41×10^{12}

of enhancement in both V_{th} shift and data retention compared with Ag NPs-MoS₂ and Pt NPs-MoS₂ floating gates even though it has improvement in both sides. Hence it is believed that the band bending and ξ_{bi} are essential for efficient charge trapping and data retention capability. To gain the in-depth understanding on the influence of metal-MoS₂ floating gates on the memory device performance, the dynamic charge trapping rate of the devices are also discussed here. The holes and electrons trap density is estimated by the equation $N = C_{ox}\Delta V/e$, Where the C_{ox} is the capacitance of the SiO₂, ΔV is the V_{th} shift and e is the fundamental unit of charge. The holes and electrons trapping rate are then estimated from $(dN/dt) = (C_{ox}/e)(dV_{GS}/dt)$ by using $dV_{GS}/dt \sim \Delta V/\Delta t$.¹² The holes/electrons trap rates of the memory devices are summarized in Table 1. We note that holes trapping rate in Pt NPs-MoS₂ flash memory and electron trapping rate in Ag NPs-MoS₂ flash memory is relatively fast compared with pristine MoS₂ memory device. The charge trapping rate varies, suggesting that the energy level of the trap sites differs noticeably due to metal-MoS₂ structures as floating gates. With the controlled charge trapping and better retention properties, metal NPs-MoS₂ floating gate flash memories are

used for demonstrating multibit storage ability. The flash memory need to have at least 2^n discrete data levels to achieve n-bit storage capability.⁷ Here, we use different V_{GS} signal to set the multilevel states in which the resetting operation is first utilized to relief all the trapped charge carriers with the same polarities to reset the memory devices to the initial state and the second programming pulse set the memory devices to the new charging state. The resetting and programming pulses have unlike polarities and amplitudes. Such a combination results in various densities and polarities of trapped charge carriers eventually creates multilevel data storage. Due to the ambipolar trapping of both holes and electrons, the resetting operations of metal-MoS₂ memory devices are composed of two pulses which are much complicated than the memory devices with the unipolar trapping of either holes or electrons.^{9,38} The resetting operation of metal NPs-MoS₂ memory devices are summarized in Table 2 in which the first pulse is used to reach the saturated V_{th} shift in negative or positive direction and second pulse shifts the saturated transfer curve to "0" state. Fig. 5 outlines eight gate signals for Ag NPs-MoS₂ memory devices.

The gate signals for Au NPs-MoS₂ and Pt NPs-MoS₂ memory devices are shown in Fig. S9 and S10, respectively.

Fig. 6a to 6c shows the 10⁴ s retention test data of metal NPs-MoS₂ flash memories with 8 data levels. It is anticipated that these 8 levels are distinguishable within the 10⁴ s time duration after initial programming. Thus, the flash memories based on metal NPs-MoS₂ floating gates architecture with 8 data storage levels enable a 3-bit storage capability. Previously Chen et al. reported multibit data storage capability of plasma treated MoS₂ transistors where MoS₂ acted as the semiconductor layer.³⁹ Our solution processed metal NPs-

MoS₂ floating gate holds a significant potential for large area fabrication and can be compatible with various semiconductor structures.

Endurance performance has been examined to clarify the memory functionality resulted from trapping/detrapping of charge carriers as shown in Fig. S11. The metal NPs-MoS₂ floating gate flash memories is periodically set into 8 data states by repeatedly applying 8 resetting and programming gate signals as depicted in Fig. 5, S9 and S10. The device displays highly reproducible memory behavior with

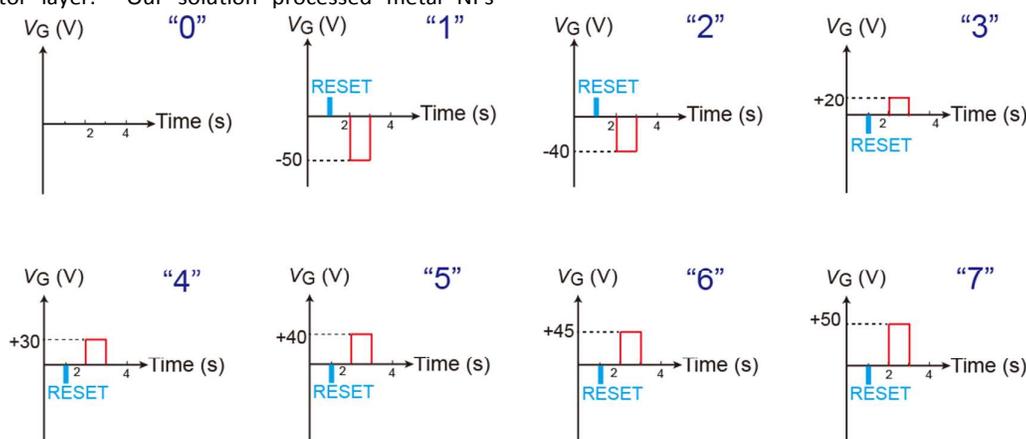


Figure 5. V_{GS} signals used for programming the flash memories into 8 data states ("0" to "7") in Ag NPs-MoS₂ flash memories.

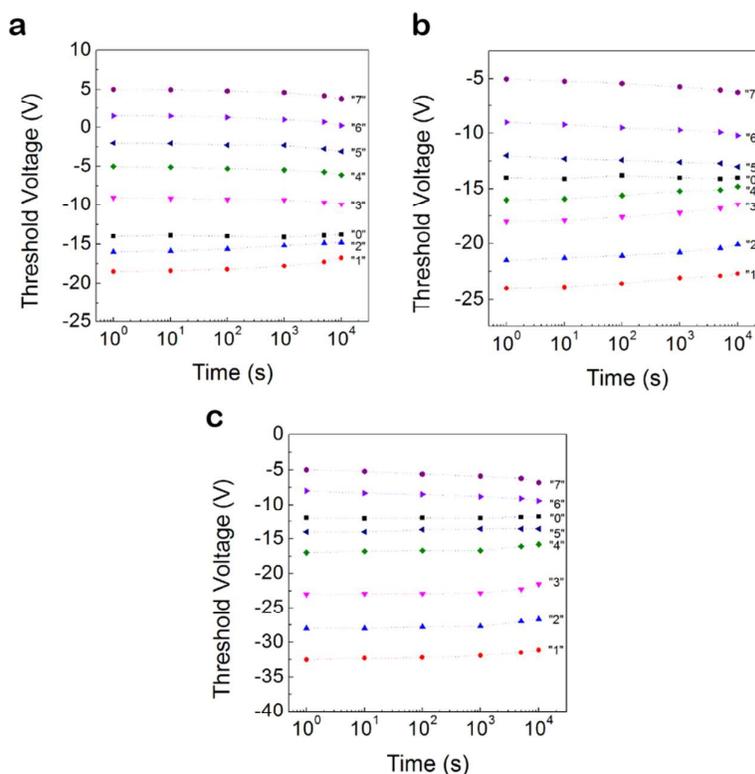


Figure 6. Retention Characteristics of 8 well-discernible data states of flash memories based on (a) Ag NPs-MoS₂ structure, (b) Au NPs-MoS₂ structure and (c) Pt NPs-MoS₂ structure.

Table 2. Resetting operation of flash memories.

	Reset pulses for positively programmed states	Reset pulses for negatively programmed state
MoS ₂	+50 V, 1 s" + "-50 V, 1 s"	"-50 V, 1 s" + "+50 V, 1 s"
Ag NPs-MoS ₂	+50 V, 1 s" + "-60 V, 5 s"	"-50 V, 1 s" + "+35 V, 1 s"
Au NPs-MoS ₂	+50 V, 1 s" + "-50 V, 1 s"	"-50 V, 1 s" + "+50 V, 1 s"
Pt NPs-MoS ₂	+50 V, 1 s" + "-30 V, 1 s"	"-50 V, 1 s" + "+60 V, 5 s"

8 well-separated data storage levels after more than 100 cycles without degradation.

Experimental

Materials. Auric acid (HAuCl₄·3H₂O), silver nitrate (AgNO₃), chloride platinum acid (H₂PtCl₆·6H₂O), sodium borohydride (NaBH₄), trisodium citrate (Na₃Ct), 3-aminopropyltriethoxysilane (APTES) and pentacene (sublimated grade) were obtained from Aldrich. All chemicals and solvents were used without further purification.

Preparation of Ag, Au, Pt NPs. The Ag NPs colloidal solution was prepared by drop-wise adding AgNO₃ solution (1 mM in 2 mL) into mixed reductant solution (2 mM NaBH₄ and 4.28 mM Na₃Ct in 48 mL). The reductant solution were mixed and heated to 60 °C for half an hour with vigorous stirring to obtain a homogeneous solution in the dark before use. After added the AgNO₃, the temperature was further raised to 90 °C and the pH was adjusted to 10.5. The Au NPs was prepared through quickly adding the ice-cold 0.6 mL NaBH₄ (0.1 M) into 20 mL mixed solution of 0.25 mM HAuCl₄·3H₂O and 0.25 mM Na₃Ct. The Pt NPs colloidal solution was prepared by quickly adding 0.2 mL NaBH₄ (50 mM) into 40 mL mixed solution of 0.4 mM H₂PtCl₆ and 1 mM Na₃Ct.

Preparation of metal-MoS₂ floating gates. Silicon substrate with 100 nm SiO₂ was dipped in a solution of APTES (12.5 μL of APTES in 10 mL toluene) for 45 min at room temperature. Excess and non-reacted APTES molecules were then removed by washing in toluene for several times and dried by nitrogen gas. Finally, the functionalized substrate was immersed into metal aqueous colloidal solution overnight to form metal NPs monolayer. The 0.2 mg ml⁻¹ aqueous solution of suspended MoS₂ nanosheets was ultrasonicated in ice-cold water and centrifuged at 5,000 rpm to remove the aggregated nanosheets before use. The supernatant was directly drop-casted onto the metal NPs array and dried in the oven at 50 °C overnight.

Device Fabrication. A 40 nm thick pentacene were thermally deposited as the p-type semiconductor layer at a rate of 0.1 Å s⁻¹ under the base pressure of 2 × 10⁻⁶ Torr. After that, 30 nm thick gold electrodes (source and drain) were thermally evaporated through a shadow mask with a channel length (*L*) of 50 μm and width (*W*) of 1000 μm. Al₂O₃ layers were deposited using a Savannah 100 ALD system with a substrate temperature of 80 °C.

Characterization. The existence and size distribution of metal NPs and MoS₂ nanosheets were verified by high resolution transmission electron microscope (HRTEM, JEOL, JSM-2100 F) coupled with energy dispersive X-ray spectroscopy (EDS). Metal NPs monolayers were confirmed by a field emission scanning electron microscope (FE-SEM, JEOL JSM-6335F). The metal-MoS₂ floating gates were measured using atomic force microscope (AFM, VEECO Multimode V). The electrical characteristics of all the devices were measured using a Keithley 2612 source meter at room temperature in ambient conditions. The thicknesses of the deposited layers were measured using the ellipsometer.

Conclusions

We have successfully achieved multi-functionalities including controlled charge trapping and multi-bit storage in metal (Ag, Au, Pt) NPs-MoS₂ floating gate flash memory. The metal NPs-MoS₂ floating gate is a simple stacked structure in which the aqueous MoS₂ sheets solution with proper concentration is directly drop-casted onto the surface of metal NPs monolayer based on solution-processed method. As additional trapping sites, metal NPs tunes the Fermi level of MoS₂ eventually achieving band bending and built-in electric field ξ_{bi} between the interface of metal NPs and MoS₂. The ξ_{bi} induces easier trapping and longer retention of holes or electrons and a tunable charge trapping behavior could be obtained. With the controlled charge trapping and better retention properties, metal NPs-MoS₂ floating gate flash memories serve as multibit memory devices possessing 3-bit storage capability and a good retention capability up to with 10⁴ s. We foresee that our findings will influence MoS₂ and other 2D materials for nanoelectronic applications. The controlled charge trapping, long data retention capability, multilevel data storage and simple fabrication method of our metal NPs-MoS₂ flash memory allows the integration of arithmetic, demodulating and memory functions in the same physical space. The presented device architecture could be further developed for future high-performance computing, information storage and communication applications.

Acknowledgements

We thank Mr. T. F. Hung for the SEM & TEM images. This work was supported by the Strategic Research Grant of the City University of Hong Kong (Project No. 7004198). H.Z acknowledges MOE under AcRF Tier 2 (ARC 26/13, No.

MOE2013-T2-1-034; ARC 19/15, No. MOE2014-T2-2-093), AcRF Tier 1 (RGT18/13, and RG5/13), NTU Start-Up Grant (M4080865.070.706022) and NTU-HUJ-BGU Nanomaterials for Energy and Water Management Programme under the Campus for Research Excellence and Technological Enterprise (CREATE), that is supported by the National Research Foundation, Prime Minister's Office, Singapore.

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