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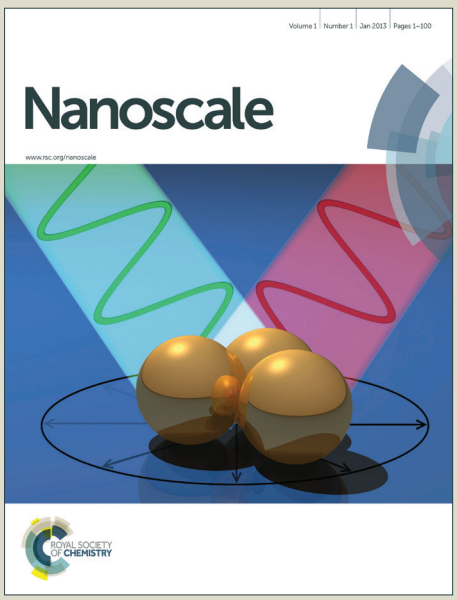

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ARTICLE TYPE

Ultralow-power Non-volatile Memory Cells based on P(VDF-TrFE) Ferroelectric-gate CMOS Silicon Nanowire Channel Field-Effect Transistors

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Nanowire-based ferroelectric-complementary metal-oxide-semiconductor (NW FeCMOS) nonvolatile memory devices were successfully fabricated by utilizing single n- and p-type Si nanowire ferroelectric-gate field effect transistors (NW FeFETs) as individual memory cells. In addition to having the advantages of single channel n-and p-type Si NW FeFET memory, Si NW FeCMOS memory devices exhibit a direct readout voltage and ultralow power consumption. The reading state power consumption of this device is less than 0.1 pW, which is more than 10^5 times lower than the ON-state power consumption of single-channel ferroelectric memory. This result implies that Si NW FeCMOS memory devices are well suited for use in non-volatile memory chips in modern portable electronic devices, especially where low power consumption is critical for energy conservation and long-term use.

1. Introduction

Non-volatile memory chips are indispensable in modern portable electronic devices, and ferroelectric memory has great potential for use in such applications. Building ferroelectric memory with low power consumption is especially critical for conserving energy and for the long-term use of such devices. Ferroelectric memory based on ferroelectric-gate field effect transistor (FeFET) has many desirable features over conventional memory, including non-destructive readout operation, small cell size, low-voltage operation and non-volatility. In particular, the physical movement of atoms in the ferroelectric layer in response to an external field happens to be extremely fast with a finite energy barrier for ionic displacement within crystal structure of ferroelectric materials, and only requires an electric field to induce the polarization of ferroelectric layer. This allows ferroelectric memory to work at very low power and with high-speed programming/erase states.[1-3]

Nanowires (NWs) as conducting channel in FETs have gained attention over the past decade because of their unique physical properties.[4] The small dimension and high crystallinity of NWs enable to realize NW-based FETs and it exhibits enhanced field-effect mobility (μ_{eff}), subthreshold swing (*S.S*), and operation voltage.[5-8] Due to the superior carrier transport properties, it can be utilized in various applications, especially for NW FeFETs.

Many reports have suggested that NW FeFETs exhibit higher performance, specifically longer retention time and better endurance when compared to thin-film based FeFET memory.[9-12] The superior mobility and small size of CNTs and graphene ribbons has been exploited in order to replace recent Si technology in device operation speed.[13,14] However, graphene-ribbon based FeFETs suffer from a very low on/off ratio due to semi-metallic behavior and high leakage current caused by scattering from various sources, such as charged impurities and atomic defects/ripples.[15,16] Also, the difficulty in selecting metallic or semiconductor CNTs continue to limit their use in ferroelectric memory applications.[17] So far, in terms of transport properties, Si is still the best candidate for use as a conducting channel.[6,7]

The difficulty in obtaining a good interface between oxide ferroelectric materials (e.g. Lead Zirconate Titananium-PZT, Bismuth Titanium Oxide-BTO) and Si conducting channels lies in the buffer layer between the ferroelectric material and the Si, which leads to an increase in the depolarization field and working voltage of Si-based FeFET memory.[1,18] Organic ferroelectric material poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) for nonvolatile memory devices has been exploited by many research groups, not only because of its light weight, flexibility, solution-based wide-area application, and simple, low-cost fabrication, but also because a buffer layer may be omitted owing to its low-temperature processing capability.[2,19-22]

A single NW FeFETs for high-performance ferroelectric memory devices have been well studied.[9-12] Due to the ON and OFF states being determined by a difference in current through the conducting channels, the reading power consumption is at a maximum in the high conductance state (ON), which can be 10^2 to 10^5 times higher than in the low conductance state (OFF).[9-12] Furthermore, complementary metal oxide semiconductor-(CMOS) based logic devices involving n-type and p-type field-effect-transistors (FETs) are used almost exclusively in analog and digital circuits because of their simplicity, noise immunity, and low-static power consumption. Since one transistor of the pair is always off, the reading state's power consumption is extremely low because of the readout voltages. By taking advantage of low power consumption, high-speed at programming/erase states of single channel FeFETs memory, and

low power consumption for reading states in the CMOS structure, the production of high performance and ultralow power memory can be expected.

In this study, nanowire-based ferroelectric CMOS (NW FeCMOS) memory devices were produced by combining a single n- and a p-type Si NW FeFETs. The newly developed memory devices can be operated with ultralow static power dissipation and reading state power consumption, much lower than that of typical single-channel NW FeFETs memory devices. The interfacial layer problem was overcome by incorporating P(VDF-TrFE) as a ferroelectric-gate through a low temperature fabrication process, having chosen Si as the best candidate in terms of transport properties and an omega-shaped ferroelectric gate for enhancing device performance. By optimizing the doping concentration of the Si NW, the NW FeCMOS memory cells exhibit excellent memory characteristics with ultralow ON and OFF reading-state power consumption, a direct readout voltage with a voltage modulation between the ON and OFF states exceeding 10^4, and a retention time of over 5×10^4 sec while maintaining a V_{ON}/V_{OFF} ratio higher than 10^3.

2. Experimental

Synthesis of n- and p-type Si NWs: The n- and p-type Si NWs used in this study were grown on Si (100) substrates with Au catalysts using a vapor-liquid-solid method, as reported in detail by T. Koo *et al*.[23] In this experiment, n- and p-type Si NWs were doped with phosphorus or boron directly during growth. The silane (SiH_4)/phosphine (PH_3) gas ratio was varied from 4,000:1 to 10,000:1 for n-type Si NWs, whereas the boron-doped p-type Si NWs were grown with a silane (SiH_4)/diborane (B_2H_6) gas ratio varied from 3,000:1 to 6,500:1.

Si NW FeCMOS memory device fabrication and characterization: Single crystalline Si NWs with a typical diameter of 50-70 nm were first dispersed via ultra-sonication in isopropanol and then transferred onto a silicon substrate by dropping a liquid suspension of the Si NWs using a pipette. A heavily doped p-type Si substrate (0.005 Ω cm) was employed as a back gate with a 100 nm thick, thermally-oxidized SiO_2 top layer as a gate oxide layer. Source and drain electrodes were patterned on the nanowire following standard photolithography. Prior to deposition of the metal electrodes, the samples were immersed in a buffered 1% hydrofluoric acid solution for 15 sec to remove the native oxide layer formed on the surface of the Si NWs during processing.[23] The electrodes were subsequently deposited by electron-beam evaporation as follows to form Ohmic contacts: 80 nm thick Ti and 50 nm thick Au electrodes for n-type Si NWs, and 80 nm thick Ni and 50 nm thick Au electrodes on the p-type Si NWs. After a final lift-off process the single NW FETs were ready for the incorporation of the ferroelectric material. The 200-nm thick P(VDF-TrFE) ferroelectric layer was prepared by mixing P(VDF-TrFE) at 0.08 wt% in a solvent (2-butanone). Prior to deposition on the Si NW FETs, the samples were treated for 2 minutes in oxygen plasma. The P(VDF-TrFE) solvent was then coated onto the Si NW FETs by spin coating (1 min at 1000 rpm). Finally, thermal annealing (2 hours at 80 °C and 2 h at 130 °C in air) of the samples was carried out to form β-phase dominant P(VDF-TrFE).[24,25] The single n- and p-type Si NW FeFETs were then electrically connected to form a single-cell Si NW FeCMOS memory device. The electrical characteristics of the devices were measured in air using a probe station with a Keithley SCS-4200 system.

3. Results and Discussion

Operating mechanism of the Si NW FeCMOS inverter

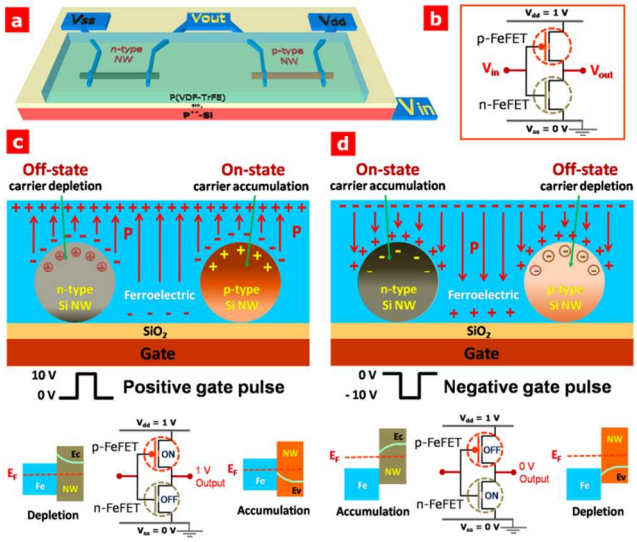

Fig. 1 Si NW FeCMOS memory device and operating mechanism. (a) A schematic view of the Si NW FeCMOS memory device based on n- and p-type Si NW FeFETs. (b) The circuit of a Si NW FeCMOS. The Si NW FeCMOS memory device operating mechanism with a back-gate pulse voltage at (c) +10 V and (d) −10 V, with V_{dd} set to 1 V.

The schematic diagram of the back-gate n- and p-type NW FeFET-based FeCMOS memory cell device and the corresponding circuit diagram are depicted in Fig.1a and b. The operating mechanism of the NW FeCMOS memory cell is proposed and shown schematically in Fig.1c and d. Unlike conventional thin-film-based FeCMOS devices that operate in either inversion or enhancement channel mode,[26,27] the Si NW FeCMOS device works in depletion-accumulation mode. Instead of using the ferroelectric layer as the back-gate dielectric layer, here the ferroelectric P(VDF-TrFE) is used as a top gate by forming an omega-shaped gate on top of the Si NWs. When a positive V_g pulse is applied to the back gate, a positive electrostatic field gradient from the gate to air will be induced, and thus the polarization direction of ferroelectric film points upward. Therefore, the electronegative fluorine anions (F^-) in the P(VDF-TrFE) layer are distributed on the nanowire surface, while the protons (H^+) gather at the P(VDF-TrFE)-air interface upon polarization. After the back-gate voltage pulse is removed, the remnant polarization of the P(VDF-TrFE) introduces a negative field effect, and further induces an equal amount of positive space charges within the nanowires. The negative polarization potential of the ferroelectric layer should bend the Si NW conducting channel band upward, bringing the valence band of the p-type Si NWs close to the Fermi level, which causes an

accumulation of holes, thus enhancing the conductance and allows the p-type Si NW FeFET to operate in an ON (low resistance) state. On the other hand, bringing the n-type Si NW conduction band away from the Fermi level will cause depletion of electron in the NWs, and thus decreasing the conductance of the n-type Si NW FeFET. In this particular case, the n-type Si NW FeFET operates in an OFF (high resistance) state; therefore, the Si NW FeCMOS readout state of 1 V is observed because of the output and V_{dd} connecting through the ON state of the p-type Si NW FeFET. Conversely, when a negative pulse at the back-gate is applied, the positive polarization potential of the ferroelectric layer bend the Si NW conducting channel band downward, bringing the p-type Si NW valence band away from the Fermi level and depleting holes in the NWs, causing the p-type Si NW FeFET to operate in an OFF state. At the same time, bringing the n-type Si NW conduction band close to the Fermi level causes an accumulation of electrons in the NW, and causes the n-type Si NW FeFET to operate in an ON state. Thus, a Si NW FeCMOS output of0 V is observed because of a grounding of the output and V_{ss} through an ON state in the n-type Si NW FeFET.

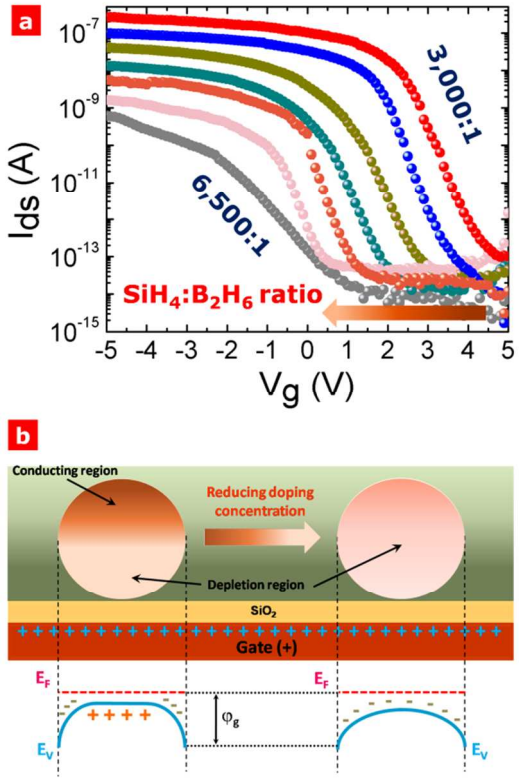

Fig. 2 Negative shift of the threshold voltage of p-type Si NW FETs. (a) I_{ds}–V_g transfer characteristics of p-type Si NW FETs at different doping concentrations [Silane (SiH_4)/ diborane (B_2H_6) gas ratios of 3,000:1 to 6,500:1]. (b) A schematic view of a simplified depletion model for p-type Si NW FETs at different doping concentrations and a constant positive gate voltage.

The charge-trapping of carriers on the conducting channel-ferroelectric layer interface and the depolarization field both contribute to short retention times in FeFET-based memory.[1,2] According to Ma *et al.*,[1] the depolarization field is dependent on remnant polarization P_r. For a nanowire FeFET, the electric field created from the remnant polarization of the ferroelectric layer should be large enough to induce the OFF state in the conducting nanowire channel of the FET. This means that the remnant polarization must create an electric field larger than the back-gate static electric field, which induces the threshold voltage of the NW FET without the ferroelectric-gate layer. Here, our strategy was to obtain a long retention time for the memory by reducing the threshold voltage of the Si NW FET; this was achieved by varying the doping concentration. When the Si NW FET threshold voltage is reduced, a smaller remnant polarization from the ferroelectric layer is required, thus allowing for a thinner P(VDF-TrFE) layer, which not only reduces the gate voltage necessary to polarize the ferroelectric layer but also reduces the leakage current and charge trapping of carriers at the interface of the conducting channel and ferroelectric layer. The effect of doping concentration on the conductance and threshold voltage of p-type Si NW FETs is shown in Fig. 2a. The transfer characteristics of the drain current versus gate-source voltage (I_{ds}-V_g) of several p-type Si NW FETs at different doping concentrations were obtained by sweeping the gate voltage continuously from +5 to -5 V with drain voltage at 0.1 V. The negative threshold voltage shifted from +5 V to approximately 0 V as doping concentration was reduced. The transconductance (g_m), hole mobility (μ_h) subthreshold swing ($S.S$) and carrier concentrations are estimated from the transfer characteristics of the drain current versus the gate-source voltage (I_{ds}-V_g) by varying SiH_4/B_2H_6 gas ratios (i.e., by varying the doping concentrations). For instance, the average transconductance is estimated to fall between 0.49-93.60 nS, with hole mobility ranging from 2.5 to 478.0 $cm^2\ V^{-1}\ s^{-1}$), subthreshold swing from 84 to 389 mV dec^{-1}, and hole carrier concentrations from 1.55 × 10^{17} to1.29 × 10^{18} h cm^{-3} with doping concentration increasing from 6,500:1 to 3,000:1 SiH_4/B_2H_6. Additionally, the reduction of the ON current from 10^{-7} A to 10^{-9} A was observed when the hole carrier concentration was lowered by decreasing doping concentrations. Note that no variation was observed in nanowire diameter for different doping concentrations.

Fig. 2b shows a schematic view of a simplified depletion model for p-type Si NW FETs with different doping concentrations at a constant positive gate voltage. The dark grey gradient shows the electric field distribution under the application of a positive back-gate voltage, resulting in the depletion of hole carriers in the p-type Si NW. Furthermore, the lowered density of hole carriers readily induces full depletion at the same positive gate voltage. Therefore, reducing the doping concentration leads to fewer hole carriers in the conducting p-type channel Si NWs, resulting in reduced conductance and a negative shift of the threshold voltage of the Si NW FETs. However, further reduction in threshold voltage also deteriorates the performance (conductivity, transconductance, mobility, and the I_{ON}/I_{OFF} ratio) of the FET. To maintain a sufficient I_{ON}/I_{OFF} ratio exceeding 10^5 and to build long retention-time memory devices, the doping concentration was optimized at a 5,500:1 gas ratio of SiH_4/B_2H_6, and threshold voltage of ~1 V. A similar approach was applied with n-type Si NWs; an optimized doping concentration was achieved at a 6,000:1 ratio of Silane (SiH_4)/Phosphine (PH_3),

with a threshold voltage of ~(-1 V), leading to an I_{ON}/I_{OFF} ratio exceeding 10^5 and a long retention time.[28]

To investigate the electrical properties of n-type and p-type Si NWs, Si NW FETs were prepared on the same SiO_2/Si substrate (100 nm thermally oxidized SiO_2 on heavily-doped Si, resistivity at 0.005 Ω cm) using Si as a back gate electrode, where the conducting channel length of the nanowire FETs is ~5 μm, and the diameter of the nanowire ~ 55 nm. (See Fig. S2 in the Supporting Information). For the n-type Si NW FET, g_m of 9.7 nS was extrapolated from the linear region of the I_{ds}–V_g transfer characteristic for V_{ds} = 0.5 V. The field effect electron mobility (μ_e) was 9.9 $cm^2\ V^{-1}\ s^{-1}$) and the *S.S* was 168 mV dec^{-1}. For the p-type Si NW FET, g_m was 14.1 nS, the field effect hole mobility (μ_h) was 7.2 $cm^2\ V^{-1}\ s^{-1}$, and the *S.S* value was approximately 216 mV dec^{-1}. The subthreshold swing values for the n-type and p-type Si NW FETs are small enough to indicate low power consumption and high performance.

For characterization of the devices as memory, the hysteresis behavior of single n- and p-type Si NW FeFETs as a function of the sweep range of gate voltages was investigated, as shown in Fig. 3a and b, respectively. A positive or negative polarization of P(VDF-TrFE) is induced on a Si NW depending on the back gate voltage sweep direction, enabling modulation in channel conductance and threshold voltages. The hysteretic window becomes larger for wider gate-voltage sweep ranges. In these devices, ~4 V hysteresis loop windows for both n- and p-type Si NW FeFETs were observed, with a conductance difference of more than five orders of magnitude between high- and low-conductance states when the back-gate voltage was swept from −10 V to +10 V then back to −10 V for n-type and from +10 V to −10 V then back to +10 V for p-type, with a sweeping step of 0.1 V at V_{ds} = 1 V in an ambient environment.

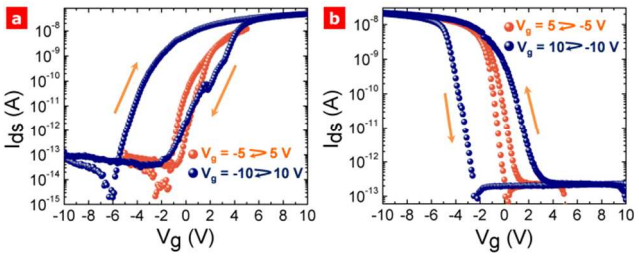

Fig.3 Hysteretic behavior for a (a) n- and (b) p-type back-gate Si NW FeFET in which P(VDF-TrFE) is coated on the NW surface and the gate voltage is scanned from −5 to +5 V, −10 to +10 V and backward for n-type and from 5 to −5 V, 10 to −10 V and backward for p-type. V_{ds} = 1 V.

The retention times of the P(VDF-TrFE)-based Si NW FeFET memory are shown in Fig. 4a for a single channel n-type and in Fig. 4b for a single channel p-type Si NW FeFET at high and low conductance states (*i.e.*, ON and OFF states, respectively). These were measured at V_{ds}= 1 V after the device was switched ON and OFF using −10 V writing and +10 V erasing pulses, respectively, for n-type; and +10 V writing and –10 V erasing pulses, respectively, for p-type with pulse widths of 1 sec. A conductance ratio between the ON and OFF states exceeding $10^5$was observed and remained above 10^3 after 5 × 10^4 sec (~14 hours). It should be noted that at V_{ds}= 1 V the ON current was less than 10 nA while the OFF current was much lower, <0.1 pA, which results in less than 10 nW of reading power consumption in the ON states and less than 0.1 pW of reading power consumption in the OFF states for both n- and p-type Si NW FeFET memory devices.

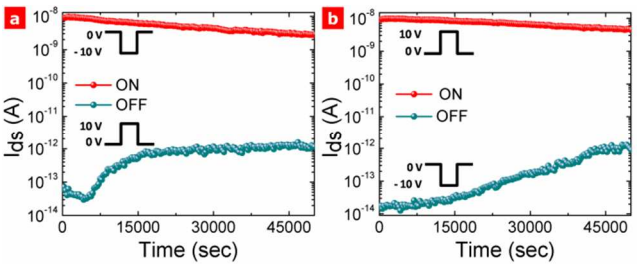

Fig. 4 Memory properties of single n- and p-type Si NW-coated P(VDF-TrFE) FeFET-based memory: retention time evolution of the drain currents of (a) n-type and (b) p-type Si NW FeFET devices. These were measured at V_{ds} = 1 V and V_g = 0 V after the device was switched ON and OFF using −10 V writing and +10 V erasing gate pulses, respectively, for n-type and vice versa for p-type FeFETs, all with pulse widths of 1 sec.

When a single n- and p-type Si NW FeFET are combined to form a single memory cell (i.e., a Si NW FeCMOS), the inverter transfer characteristics and hysteretic behavior are interpreted as the relationship between the output (V_{out}) and input (V_{in}) voltages when input voltage (V_{in}) is swept from –5 V to +5 V, then from –10 V to +10 V and again to the other polarity direction. This measurement was performed on both the Si NW FeCMOS devices with the ferroelectric P(VDF-TrFE) layer coating the NWs as well as a Si NW CMOS inverter without the ferroelectric layer, as shown in Fig. 5b and a, respectively; note the inverter supply voltage (V_{dd}) was 1 V. As can be seen in Fig. 5b, a hysteretic loop window of ~2 V was observed with a voltage ratio of more than 10^4 between the ON and OFF states when the input voltage was swept from −10 V to +10 V and back. A smaller hysteresis window of less than 0.5 V, was observed for the Si NW CMOS inverter (i.e., without the ferroelectric layer, Fig. 5a).We believe that this smaller hysteresis window may be caused by the trapping of chargecarriers at all the SiO_2/Si interfaces, including anyminute SiO_2/Si interfaces on the NW, due to immobile oxide charges or oxide-trapped space charges associated with defects in the SiO_2.[29] Since the large increase in the hysteretic window from <0.5 V to ~2 V is clearly observed only when the P(VDF-TrFE) was incorporated, it can be concluded that the critical contribution to the origin of such pronounced hysteretic behavior should mainly come from the polarization of the ferroelectric layer.

Retention times of the Si NW FeCMOS memory cell for the high- and low-conductance states, *i.e.* ON and OFF states when both p- and n- channels are connected, are shown in Fig. 6. In Fig. 6b retention times are shown for V_{dd} = 1 V and input V_g = 0 V after the device was switched ON and OFF using +10 V writing and −10 V erasing gate pulses, respectively, with a pulse width of 1 sec. The voltage ratio between the ON and OFF states exceeded 10^4 and remained above 10^3 for more than 50,000 sec

(~14 h). Even with a small hysteresis window (i.e., less than 1 V), when sweeping the back-gate voltage from −5 V to +5 V and back (Fig.5b), the ratio of the output voltage modulation between the ON and OFF states exceeded 10^4 and remained above 10^3 for 1.2×10^4 sec (>3 h) as shown in Fig. 6a. Cycle conditions were +5 V writing and −5 V erasing gate pulses with a 1 sec pulse width. This shorter retention time compared to the ±10 V gate pulses could be due to the ferroelectric P(VDF-TrFE) layer not being fully polarized by the ±5 V gate pulses.[10]

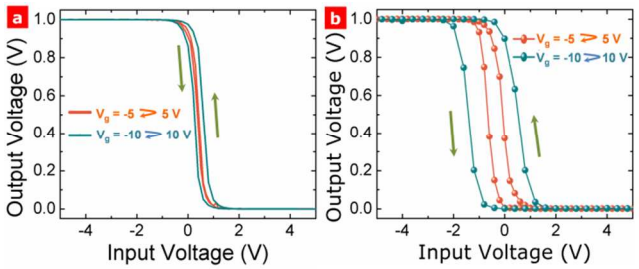

Fig. 5 V_{in}–V_{out} inverter characteristics and hysteretic behavior for a (a) Si NW CMOS and (b) Si NW FeCMOS inverter based on back-gate n-and p-type Si NW FETs and Si NW FeFETs with P(VDF-TrFE) on the NW surface, respectively, as the gate voltage is swept from −5 V to +5 V, then from −10 V to +10 V and backward.

The long retention times and high performance of the Si NW FeCMOS as well as the n- and p-type Si NW FeFET memory devices are due to the rational design of the ferroelectric top gate FET memory structure, the selection of materials, the Si/ferroelectric interface and optimized doping concentrations. These points are detailed in our previous report on nonvolatile memory based on Si NW FeFETs and can be summarized as follows:[30]

The sensitive change in conductance in the depletion-accumulation working mechanism of the nanowire FET-together with the small size and single-crystalline nanowire conducting channel allows NW FeFET devices to work at a higher speed-leads to lower subthreshold swing, and lower operation voltage, which contributes to longer retention times compared to conventional thin-film-channel-based FeFETs, in which the working mechanism is based on the inversion mode.[1,2,10]

An effective and reliable way to modulate the electrical properties of Si NWs was developed by controlling the doping concentration, which is desirable for obtaining extremely low power and long retention-time ferroelectric memory devices.

The low-temperature incorporation of the organic ferroelectric material P(VDF-TrFE) into the device fabrication allows us to avoid the interfacial layer problem that often arises with Si NW FeFET. It also enables higher-performance memory as well as the potential to fabricate the device on flexible substrates for flexible nonvolatile memory applications with a uniform coating and facile control of the thickness of the ferroelectric layer.[1,2,10] Compared to other ferroelectric materials like PZT or BTO, no interfacial layer is formed during the crystallization process of P(VDF-TrFE), making the buffer layer unnecessary. Without the interfacial layer, the charge trapping effect at the interface of the surface of the organic film and the Si NW semiconductor channel is minimized. When direct contact is realized in a FeFET, the data retention time is likely to be much longer than that in a conventional FeFET, because no depolarization field is generated by the buffer layer.

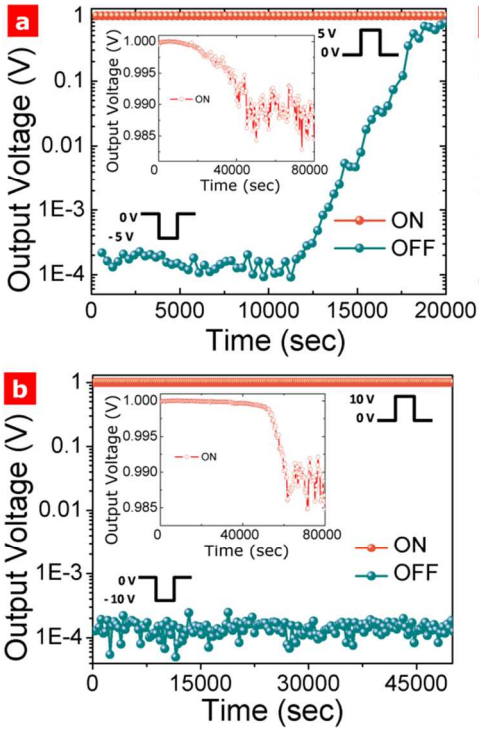

Fig. 6 Retention times evolution of a Si NW FeCMOS memory device. These were measured at V_{dd} = 1 V and input V_g = 0 V after the device was switched ON and OFF using (a) 5 V writing and -5 V erasing gate pulses, (b) 10 V writing and -10 V erasing gate pulses, all with pulse widths of 1 sec. Inset figures are the linear scale of the ON state.

Since there is no buffer layer needed and an omega-shape gate is formed by using the spin-coatable organic ferroelectric material, direct effects of the remnant polarization field of the ferroelectric gate on the surface of the nanowire allow the Si NW FeFET memory to operate at a lower voltage and output a higher I_{ON}/I_{OFF} ratio, thus leading to enhanced transconductance and field-effect mobility compared with omega-shape gate based NW FETs or ferroelectric planar-gate-based FeFETs.[31,32]

Ferroelectric memories based on FeFETs have an intrinsic advantage offering very low programming power consumption over other emergent non-volatile memories including phase-change memory (PCM), resistive random access memory, flash memory based on floating gate FETs, magnetic random access memory (MRAM) and capacitor ferroelectric memory. Furthermore, the ferroelectric memory requires only the gate voltage for the ferroelectric polarization switching. Therefore, the FeFET will show lower programming power consumption than PCM and MRAM if they are on a comparable size scale. This is an attractive alternative to flash memory and other existing non-volatile semiconductor memory technologies.

Furthermore, a CMOS inverter uses complementary pairs of p-type and n-type metal oxide semiconductor field-effect transistors (MOSFETs) and was the primary technology to be implemented in very-large-scale integration (VLSI) chips for both digital and analog signal applications. Two important characteristics of CMOS devices are high noise immunity and low static-power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between ON and OFF states. By taking key advantage of the concept of the CMOS inverter, the Si NW FeCMOS memory studied here, with its direct voltage readout of logic states, has ultralow consumption of static power dissipation and reading state power consumption due to the fact that only a small current less than 0.1 pA flows from the V_{dd} to the ground (V_{ss}), irrespective of whether the output is in a high state or at a low state, i.e. ON and OFF states of a Si NW FeCMOS memory device, since one transistor of the n- or p-type is always at a low conductance state (OFF). Unlike those conventional memory devices based on a single n-type or a single p-type FeFET cell in either NAND or NOR memory array structures where the selected cell logic state (i.e. "ON ≡ 1" or "OFF ≡ 0") is determined by comparing each readout bit with a reference current levels,[33] the reading state's power consumption is at a maximum in the high conductance state (ON) up to 10 nW in the single n- or p-type Si NW FeFETs (Fig. 4a and b) due to the ON and OFF states being determined by the difference in current through the conducting channels. In the case of the Si NW FeCMOS device, the ON and OFF logic states are determined by the difference of the voltages at the output, these can be read directly by other CMOS logic circuits and thus does not need any external sense amplifier or reference current level circuit. As the feature of CMOS logic devices, the power consumption at readout voltage states can be negligible due to the voltage output of FeCMOS will be read by the gate of other FETs. Therefore the reading state's power consumption is determined by the low-conductance currents through the n- or p-type channel when the device is in the ON or OFF state, respectively. Note that the current in the low-conductance state for both n- and p-type Si NW FeFETs is less than 0.1 pA (Fig. 4a and b) when V_{out} is 0 V or 1 V at V_{ds} = 1 V. Therefore, the reading state's power consumption of Si NW FeCMOS can be as low as 0.1 pW, more than 10^5 times lower than the ON state power consumption of a single-channel Si NW FeFET memory cell. This extremely low reading-state power consumption is the lowest yet reported for ferroelectric memory. Therefore, this device structure is very important for portable memory device applications where the power consumption is critical.

For viable memory applications, many memory cells would need to be integrated into a small area, and thus an individual top gate configuration would be desirable. Further reduction of the nanowire diameter is also expected to lower the operating voltage. Moreover, if the P(VDF-TrFE) ferroelectric layer can be patterned only over the conducting channel by exploiting a water-soluble photoresist,[19] soft lithography,[20] nanoimprinting lithography[22] or photolithography with a common photoresist developed by a diluted photoresist stripper,[23] the typical parasitic effects on the electrodes can be minimized. Therefore, further enhancement of memory performance is expected in terms of retention time, offering a great opportunity for viable industrial applications.

4. Conclusions

In summary, Si NW FeCMOS memory cells using single n- and p-type Si NW channels and a P(VDF-TrFE) ferroelectric-gate have been successfully fabricated. The memory device performance is carefully characterized in terms of its electrical transport and retention times. By optimizing the doping concentration of the both n- and p-type Si NWs, the NW FeCMOS memory cells exhibit excellent memory characteristics, even at less than 1 V hysteresis window at ±5 V write and erase gate pulses, with ultralow ON and OFF reading states power consumption and the device has direct readout voltage with a large voltage modulation between the ON and OFF states exceeding 10^4, a long retention time of over 1.2 x 10^4 sec while maintaining an V_{ON}/V_{OFF} ratio higher than 10^3. Our results imply that extremely low-power consumption, high performance and high-density memory devices, as well as suitability for the next generation of ferroelectric memory based on flexible electronics can be expected.

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Notes and references

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