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Large scale fabrication of well-aligned CdS/p-Si shell/core nanowire arrays for photo detectors using solution methods

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We report a facile approach for preparing the vertically aligned, large scale CdS/p-Si shell/core nanowire heterojunction arrays based on successive ionic layer adsorption and reaction depositing. The results indicate that the rectifying characteristics of CdS/Si shell/core nanowire arrays can be tailored by changing the number of SILRA cycles, and the CdS/Si shell-core nanowire heterojunctions have the good photo sensitivity (the ratio of photocurrent to dark current could reach 14.96 at -1V reverse bias) under AM 1.5(1 Sun) illumination. Furthermore, the electron transports mechanism across the CdS/Si nano-heterojunctions is also detailly discussed. This reported CdS/p-Si shell/core nanowire structure offers a generic approach for the integration of new functional materials for photo-electrics applications.

1 Introduction

In recent years, the studies of the core–shell radial hetero-junction nanowires have attracted much attention due to their exhibit unique electronic and optoelectronic properties and promising applications, such as photodetectors,[1,2] soalr cell[3,4] and light-emitting diodes.[5,6] These studies have shown that the core–shell radial hetero-junction nanowires are superior to bulk heterojunction devices since the carrier separation takes place in the radial direction, with carrier collection distance smaller or comparable to the minority carrier diffusion length.[7,8] In addition, recent theoretical investigations have also revealed that coaxial nanowire structures may be useful to improve the carrier collection and overall efficiency of the devices as compared to single-crystal bulk semiconductors. Among various one-dimension semiconducting materials, CdS is an important direct gap semiconductor material with strong visible optical absorption and n-type conducting behavior. Moreover, past studies show that CdS/Si nanowire heterostures possess excellent optoelectronic properties, such as tunabling photoluminescence,[9] broadband light transparency and high electrical conductibility of cadmium sulfide (CdS).[10-12] Therefore, the formation of CdS heterojunction with a group narrow band-gap semiconductor is attractive for the fabrication of band gap engineered devices.[6,13-15]

For the fabrications of CdS nanoheterostructures, there are many work has been published, such as elcectrochemical synthesis[16] and chemical bath deposition (CBD).[12] To our knowledge, there are few reports about the CdS/Si nanowire heterojunction by CBD or pulsed laser ablation.[12,17] However, studies also show that the conventional CBD or pulsed laser ablation method has some drawbacks. For example，In the work of CdS on ZnO based on CBD method, only CdS nanoparticles coated ZnO nanowires were obtained rather than uniform CdS shell layers,[18] and in the work of CdS on Si nanowires using pulsed laser ablation method, the elaborated and expensive equipments are especially needed.[17] Therefore, for the fabrications of CdS/Si nanowire heterojunctions, it is very interesting to search the elaborate synthesis techniques and find how to facilely and inexpensively realize the conformal radial hetero-junction nanowires. In addition, control of the shell thickness is a key step toward the realization of high efficiency nanoelectric devices.

The successive ionic layer absorption and reaction (SILAR) is a solution process,[19] which is analogue of atomic layer deposition (ALD) where the film is built up atom by atom using a self-limiting reaction. Unlike other fabricating process (e.g. vacuum process and laser ablation), SILAR process can usually produce large scale samples and are more low-cost than other fabricating methods. A survey of the literature reported that thickness of CdS shell for Si-CdS nanocrystals can be tuned by the cycles of SILAR.[16] However, up to now, there are few works involved on the fabrications of CdS/Si nanowire arrays (SiNWAs) using the SILAR methods. In particular, the photo-electrical properties and transport mechanism of CdS/Si heterostures NWAs are not understood clearly.

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In this work, we report a facile solution approach to fabricate the CdS/Si radial heterostructure nanowire arrays. The SiNW core and CdS shell were synthesized using simple and cost-effective aqueous solution methods. Both methods are applicable for large-scale synthesis. The large-area vertically aligned p-Si nanowire arrays are fabricated using electroless chemical etching, [20] SILAR processing for growing CdS shell was conducted according to the technique reported elsewhere.[18] The structure and photo-electronics characteristics of the core–shell CdS/Si nanowire junctions are characterized and discussed. Moreover, the related physical mechanisms are also explained based on the energy band diagram and the electron transport mechanism across CdS/SiNWAs.

2 Experiments

2.1 Preparation of SiNWA

SiNWAs on Si substrate were prepared using a previously reported method by metal ion-assisted aqueous electroless etching. Briefly, clean p-type 0.1-1 Ω .cm Si (100) substrates were immersed in aqueous solution of HF(4.8M) and $AgNO_3$(0.02M) for 30min at room temperature. The etched substrates were dipped into a aqueous solution of HNO_3 (30%,W/W) and then rinsed with de-ionized (DI) to remove any residual silver. The surface oxide layer was removed by aqueous HF(10%,W/W) for 10min. Then the substrates were rinsed with DI water and dried under N_2 flow.

2.2 Preparation for CdS/Si nanowires heterostructure

CdS thin films were deposited on SiNWA by SILAR. First, the substrates with SiNWA were immersed in $CdCl_2$ ethanol solution (0.1mol/L) for 5 min, and then clean with ethanol and natural drying. After that, immersed in $(Na)_2S$ aqueous solution (0.1mol/L) for 5 min, and clean with DI water, natural drying. Between each immersion step, the sample was rinsed with DI water for 2min to remove excess ions that were weakly bound to the nanowire surfaces. This immersion cycle was repeated for up to 40 cycles and, after finishing the coating, the samles were dried by N_2 blowing. The CdS coated substrates were annealed in vacuum chamber at 500℃ for 30min because the post annealing could improve the crystallization of CdS (Fig.S1). Finally, a ~150nm Al layer was deposited on the substrate rear side and ~10nm Cu layer (5mm× 5mm) through a shadow mask as the transparent front contact. A Cu layer with 100nm thickness was deposited by evaporation through a bar shaped shadow mask for ohmic electrode. The average active area of the devices was 25mm^2 defined by the area of the transparent Cu electrode.

2.3 Characterization and measurements

Nanoscale surface and cross-sectional morphology of the SiNWA were characterized using a field emission scanning electron microscopy (FE-SEM SUPRA™ 40). The crystallinity of the sample was analyzed by X-ray diffraction (XRD). The detailed microscopic structure and the chemical composition of the Si/CdS core/shell heterostructure were investigated using high-resolution scanning transmission electron microscopes (JEM2200FS operating at 200KV, JEOL). The optical absorption of each substrate was measured by a UV-3600 spectrophotometer with an integrating sphere in the wavelength range of 300–1200nm. The dark density-voltage (I−V) characteristics of the CdS/Si heterojunction were measured using a Keithley 2400 source meter. A solar simulator (Newport) at 100mWcm^{-2} （1 sun Am1.5 G）was used for illumination of the photodiode. We did not use any specific instrument for the purpose and all the measurement are performed at room temperature. For the photo-response measurement, the light was incident on this device geometry from the transparent (Cu film with 10nm thickness) side.

3 Results and discussions

The morphologies and crystalline structures of SiNWA and CdS/Si heterostructure arrays, obtained via a SILAR process, are investigated. The SILAR process is based on the successive surface adsorption of ions and thus proceeds via a layer by layer build up of the film. Figures 1(a) and（b）show the typical surface and cross-section SEM images of the SiNWA and CdS coated nanowire array after 40 cycles of the CdS SILAR process. Fig. 1 (a) clearly displays the formation of SiNWA, which are aligned vertically on the surface of the silicon wafer. The average length of the Si nanowires is about 5 um. It also can be seen that the nanowire arrays are evenly distributed in the mass. The formation mechanisms of nanowires have been confirmed by experiment.[19] Fig.1(b) shows SEM images of CdS coated SiNWA for 40 cycles. It can be seen a little evidence of any morphological changes of the SiNWA upon CdS deposition, such as significant surface roughening of diameter increase. The CdS phase has a lighter contrast than the Si one under SEM. This surface morphology changes were observed for 20 and 30 cycles of SILAR deposition (not shown here).

To elucidate the microscopic structure of the Si nanowire after CdS SILAR cycling, a more detailed investigation was conducted using FE-TEM. Fig. 2(a) shows a low-magnification TEM image of a Si/CdS nanowire. The Si nanowire is uniformly coated with a CdS shell of thickness of ~20nm. Fig. 2 (b) shows a high resolution

image of the Si/CdS cor/shell interface region and Fig.2 (c) is image of the Si/CdS cor/shell interface region and Fig.2 (c) is corresponding fast Fourier transform (FFT) pattern that indicate the polycrystalline CdS shell deposited on the single crystalline Si nanowire. Fig.2(d) is the energy dispersive X-ray spectroscopy (EDS) of the CdS/Si shell-core taken at the marked region, Cd and S atoms were detected in addition to Si, Cd and S to silicon ratio increases as the number CdS SILAR cycles increases(Fig.S2). Several distinguishable X-ray peaks corresponding to crystallographic plane of CdS:(100), (002),（101）, and（112）

peaks are observed in Fig.3. XRD analysis of the CdS/SiNWA clearly indicates CdS phase. In addition, Si (400) peak from the Si nanowire core is also observed (ref. JCPDS card, file no.41-1049). Also, it is observed that the intensity of the main CdS peaks increase as number of SILAR cycles increases. On the basis of the SEM, TEM and XRD data, which show gradual, uniform CdS layers grow on the Si nanowire surfaces, we suggest that the CdS growth occurs by the ion-by –ion growth mode rather than by the cluster growth mode.

The rectifying feature is a very important characteristic that is utilized in many different types of CdS/SiNW-based electronic devices. In this regard, I-V characteristics of CdS/SiNWs were measured at room temperature. Fig. 4(a) shows the I-V characteristics, we investigated correlation between the number of SILAR cycles and electrical property. The inset in Fig. 4(a) shows the schematic diagram of such a measurement system.

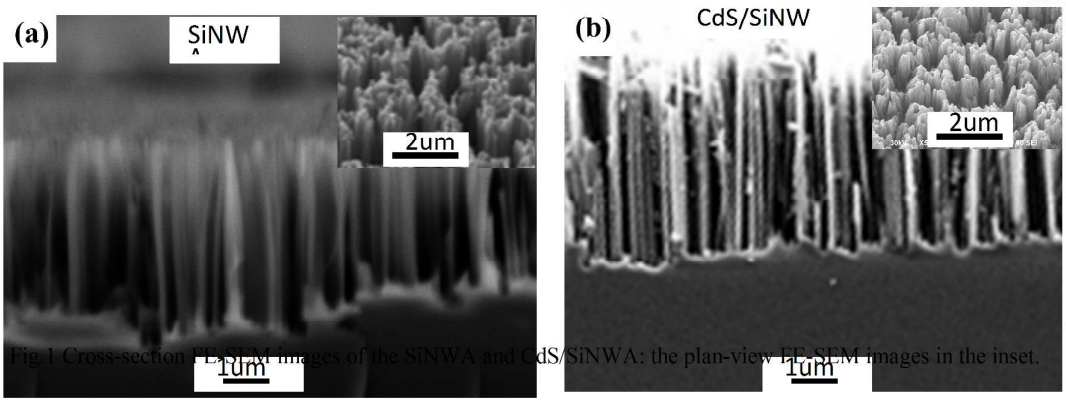

Fig.1 Cross-section FE-SEM images of the SiNWA and CdS/SiNWA: the plan-view FE-SEM images in the inset.

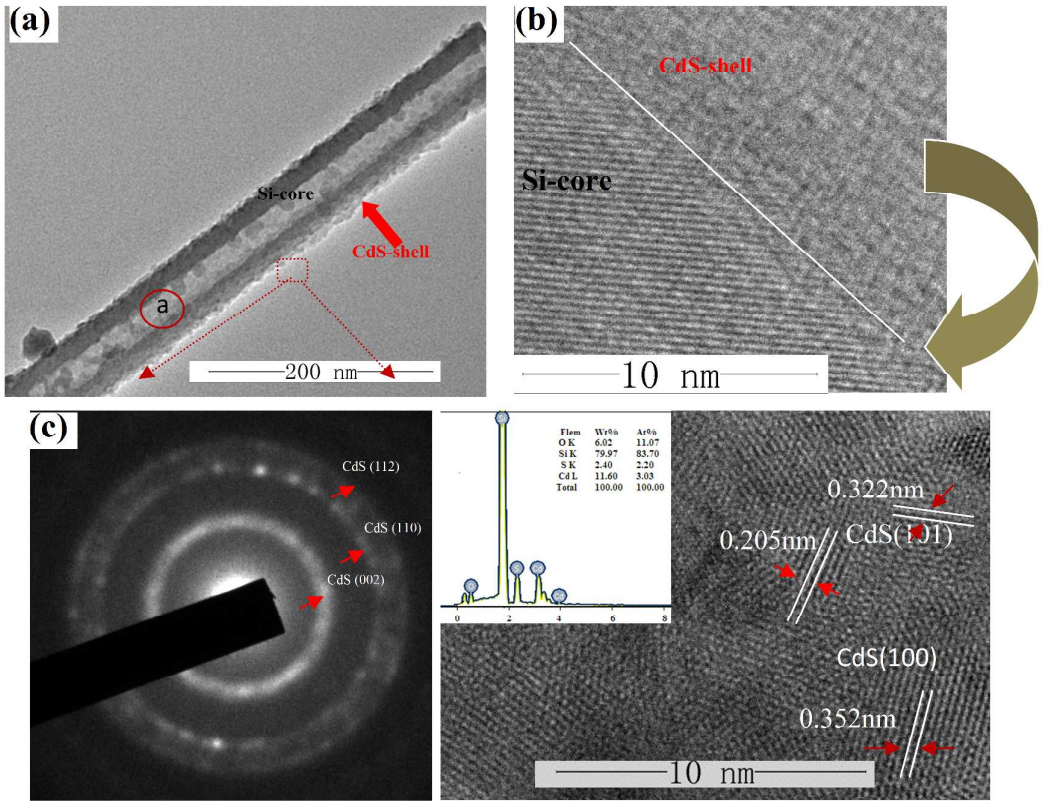

Fig.2 TEM (a) and HRTEM (b) images of the CdS/SiNW core-shell, (c) shows the corresponding SAED patterns, (d) HRTEM images of the CdS shell: EDS spectra of CdS coated SiNWs masked in (a) in the inset.

I-V characteristic c urves show obvious unidirectionality. As expected, the Cd/Si nanowire heterojunctions act as adiodes and exhibit rectifying property at room temperature. With the forward bias, current increases as the applied bias increases. In reverse bias, the current transporting through the junction is close to zero, and the results indicate that these heterostructures have good rectifying characteristic.

We have also measured the I-V characteristics between Cu contacts and CdS, Cu contacts and SiNWs/Si. I-V curves of Cu/CdS have no obviously diode rectification behavior (Fig.S4) and I-V characteristics of Cu/SiNWs/Si/Al and Cu/CdS/SiNWs/Si/Al (Fig. S5 b) confirm further that the present CdS/SiNWs core-shell heterojunctions offer the beneficial effect on rectifying characteristics, that is, effective suppression of recombination activity and enhanced rectifying effect. The results indicate that CdS shell serves as a natural barrier and protects the device from unwanted electricity leakage. These phenomena had been observed in other core-shell structured devices.[21-23] From Fig.4(a), the gradual increasing of current density at forward voltage is observed as increasing of the number of SILAR cycles. Theoretically, the I-V relation for a heterojunction could be described as

$$I = I_0\{\exp\left[\frac{q(v-IRs)}{nKT}\right] - 1\} \qquad (1)$$

Where K is the Boltzmann`s constant, T is the absolute temperature in Kelvin, q is the unit charge of a single electron, n is the ideality factor which describes the diode no-ideal behavior from an ideal diode corresponding to n=1. n=1 when the current transport mechanism in the diode conforms to pure thermionic emission. n=2 when the current transport is dominated by electron-hole recombination current. Rs is the seres resistance of the diode and I_0 is the reverse bias saturation current represented. By rearranging the above equation, the values of n for the CdS/Si heterojunction diodes can be calculated by using a method developed by Cheung et al.[24] where a plot of $\frac{dV}{d(\ln I)}$ vs I can be generated from the forward J-V characteristics in Fig .4 given by

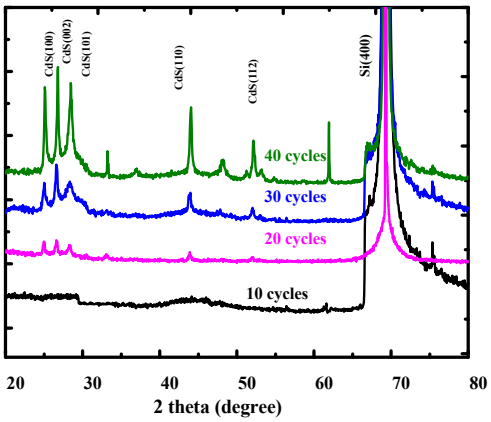

Fig.3 The XRD pattern of the samples with different cycles.

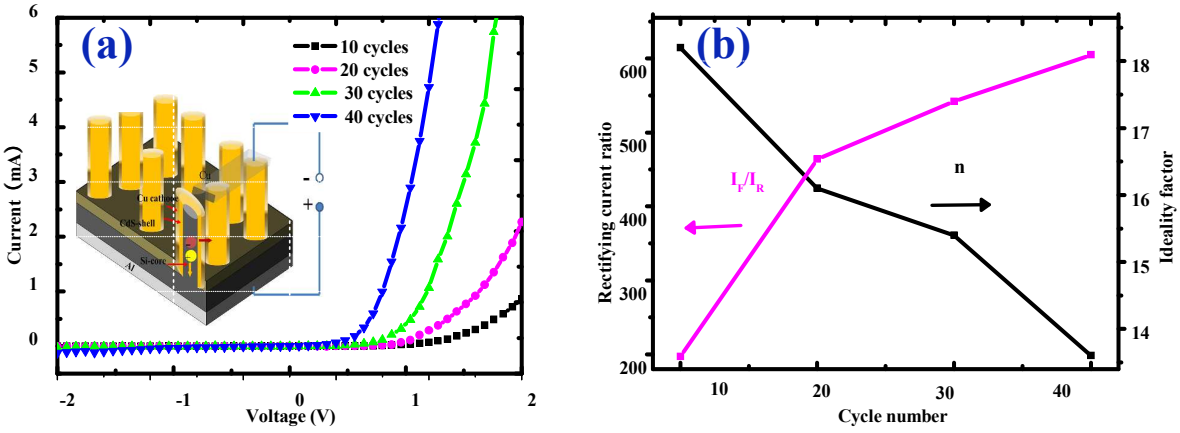

Fig.4 (a) I-V characteristic of CdS/SiNWA, the inset shows the schematic diagram of the detailed structure and electrode configuration on the CdS/SiNWA, (b) rectifying current ratio and ideality factor of the heterojunction diodes with respect to different SILAR cycles.

$$\frac{dV}{dI} = n\frac{KT}{q} + IR_s \qquad (2)$$

Hence form the plot of $\frac{dV}{d(\ln I)}$ vs I given in eqn (2), the value of Rs and n can be determined from the slope and y-intercept of the graph respectively, when n is given by

$$n = \frac{q}{KT}\frac{dV}{d(\ln I)} \qquad (3)$$

Using this approach, the value of n corresponding to the different number of SILAR cycles can be calculated from the forward J-V characteristics as shown in Fig.4(b). The value of n reduces as increasing the number of SILAR cycles (from 18.2 to 13.6). The turn-on voltage is observed to be around 0.5 V for 40 SILAR cycles. In addition, the revised saturated current also reduces as increasing

Our results indicate that the CdS/SiNW heterojunction based on SILAR processing can be used as a rectifying diode. However, the high ideality factors for the diodes in the vicinity 13 to 19 indicate that the diodes are not an ideal one. Since the ideality factor dominated by the image force effect usually does not exceed 1.05.[26] The image force effect alone cannot be used to fully explain the higher than unity ideality factor observed for the diodes. Comparable higher values of n with 23.3 for CdS/Si nanopillar heterojunction diodes have also been reported by Xinjian Li et al based on CBD method.[16] It has been reported that the large leakage current for the as-grown diodes is mainly due to the defect-mediated tunneling effect, caused by the high defect concentration or trap centers in the interfacial layer. [27] The presence of the surface states in the interfacial layer on the surface of SiNWs introduces additional energy states that fall inside the energy bandgap which do not equilibrate the potential drop across the barrier between the CdS and Si, then the short range upward band bending due to the surface

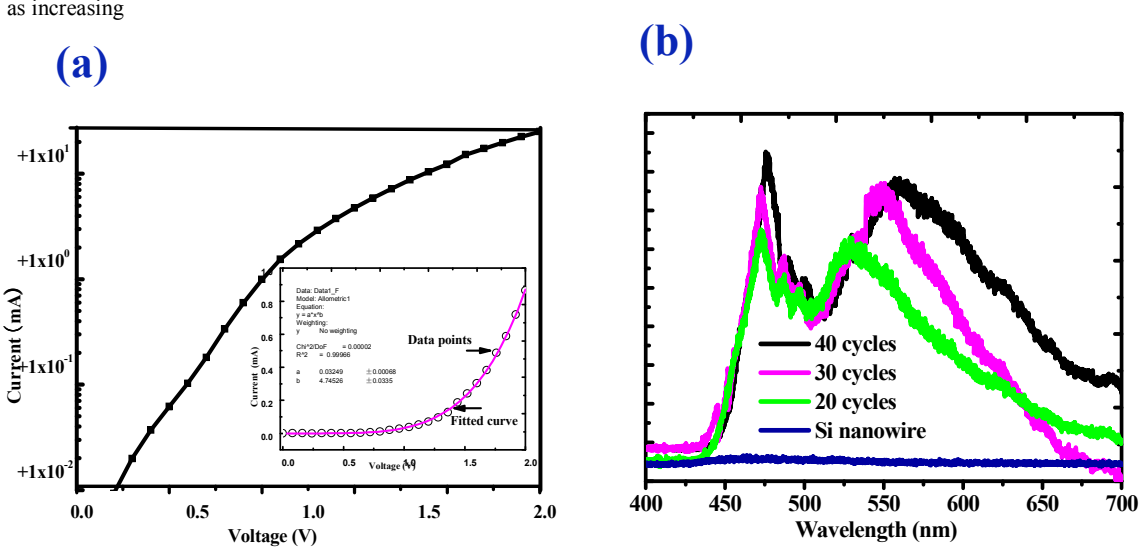

Fig.5 (a) The semilog plot of the I-V characteristic for CdS/SiNWA diodes. The inset shows a fitted I-V curve via the trap-limited model $I \sim V^m$ with m=4.7 and the proportional constant being 0.032. (b) Room temperature PL spectra of SiNWA and CdS/SiNWA with the different SILAR cycles.

the number of SILAR cycles (from 3.5uA to 0.5uA) and the forward –to–reverse rectifying ratio(I_F/I_R) increases as the number of cycles increase at ±2V (from 197 to 605). These phenomena should be due to improved crystallization which may affect the electrical properties because the size and structure are distributed uniformly when the CdS shell is thick by layer to layer.[10] The crystallization is improved as the increase of CdS shell thickness, and these are consistent with the XRD pattern (Fig.3) presented above showing an increase in the polycrystalline peaks with increasing number cycles. In a word, rectifying effect indicates that CdS shell serves as a natural barrier and protects the device from unwanted electricity leakage and increasing the shell thickness can tune and improve the rectifying behavior. Thickness effect of N-type barrier on the rectifying characteristics of ZnO/Si heterojunction diodes have also been reported by S. Mridha based on CBD method.[25]

states in the shell layers and hence influence the I-V rectifying characteristics. On the other hand, the variation of the ideality factor corresponding to the different number CdS cycles indicates that thedifferences of the shell thickness may influence the I-V characteristics.

The charge transport mechanism across CdS/SiNWA was investigated, a simulation on the I-V curve of CdS/SiNWA for 40 SILAR cycles is demonstrated and the result is shown in the inset of Fig.5(a). It is found that the curve could be fitted by a power law $I \sim V^m$, a ruler deduced from the trap-limited model for the charge transport across a heterojunction.[28] This indicates that the carrier transport process in CdS/SiNWA is mainly controlled by the interface defect states acting as carrier traps, just as that in ZnS/Si nanoheterojunctions by other groups. [29]

To verify the presence of the interface defect states, the room temperature photoluminescence (PL) spectrum of the CdS/SiNWs

arrays and SiNWs were measured with fluorescence spectrophotometer using a xenon lamp with an excitation wavelength of 325nm. PL of those nanowire array heterojunctions exhibit double peaks which cover green and red peaks, whereas no peaks obviously appear in SiNWs, which indicates that the PL peaks come from the CdS shells. A strong green band at approximately 500 nm, and a red band at approximately 600nm can be clearly seen as shown in Fig.5(b). The emission bands including the green and red bands all become strong as the number SILAR gradually increase.

The green emission is known as the free excitons recombination between the conduction and valence band where occurs near the fundamental absorption edge of bulk CdS [Fig.S3]. It is well known that CdS shell layers become thick with the number cycles increasing, and the structure crystallinity is improved. Therefore, the free excitons recombination near the fundamental absorption edge becomes strong resulting in the strong green band. When the CdS shell has been gradually changed into thickness during the cycles increase whereas Si core has not been changed, thus the red emission changing should be from the CdS shell which arises from the defects or lattice distortion. On the other hand, the peak at the long wavelength side exhibits red-shift. The crystallization is relatively improved resulting from the increase in the CdS layer, thus concentration of deep defect states decreases, the defects level shifts toward the conduction band, leading to the defect-related emission red-shift, comparable phenomena have also been reported by Guan Wang et al.[10] In addition, the relative intensity also increases as the number SILAR gradually increases. This intensity increases in the red emissions appear to be the result of the increase of defects states which result from the increase of the sulfur vacancies (Vs+) located at the shell CdS layer. These would induce additional radiative pathways for the excitations.[30] This deduction is proven by the EDS spectra (inset of Fig.3). As judged from the molar ration of Cd to S atoms at the surface calculated to be ~3.0:2.2 for CdS/Si NWA with the 40 SILAR cycles. Therefore, the Cd atom is superfluous and large quantities of Vs+ have been formed as the CdS layer increase [Fig.S2].

Fig.6(a) show the I-V characteristics of the CdS/Si core/shell nanowire heterojunctions with 40 SILAR cycles both in the dark and under AM1.5 i.e 100mW cm^{-2} illumination and time dependent photo-response. Several interesting observations were made. First, photovoltaic effect was negligible. Second, it is found that under reverse bias conditions, no significant change in the current takes place after illumination, on the other hand, the current under forward bias increase drastically. However, inset of Fig.6(a) shows the logarithmic scale plot, which shows a obviously increase in photo-current, the ratio of photocurrent to dark current could reach 14.96 at -1V, and 4.55 at 1V. The photo current to dark current ratio in the case of reverse bias is clearly much greater than that in the case of forward bias, this can be explained on the basis of an energy band diagram.

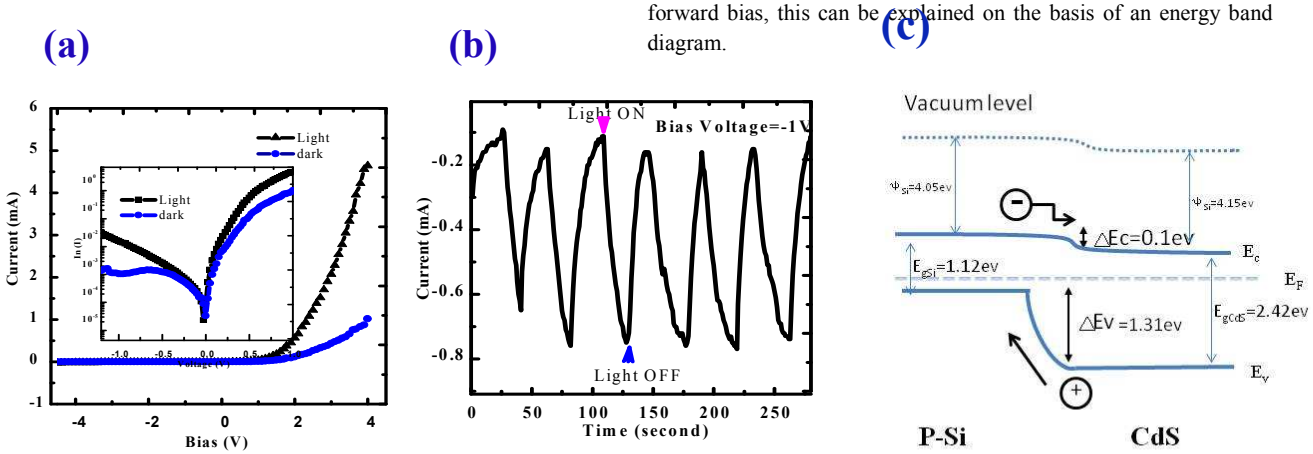

Fig.6(a) I-V characteristics of CdS/SiNWA core/shell heterojunctions under dark and light, the inset shows the logarithmic scale plot of I-V curve. (b) Time dependent photocurrent response of the CdS/SiNWA heterojunction under AM1.5.i.e. 100mWcm^{-2} illumination at bias of –1V. (c) The band diagram for a CdS/Si heterojunction.

An ideal band diagram for a CdS/Si heterojunction is illustrated in Fig.6(c). The valence band offset(ΔE_V) is 1.31ev and that of the conduction band(ΔEc) is 0.1ev. Thus, the energetic barrier for electrons is about thirteen times less than the barrier for the holes, which means that electron injection is more likely than hole injection. Due to the large difference in the valence band offset and conduction band offset, the energetic barrier for electron is much lower than that for holes, we can observe that the holes tend to be confined the Si core and the electrons reside in the CdS shell, thus the electron transporting is based on thermionic emission mechanism. The behavior of I-V curve can be partly explained by band diagram based on the Anderson model.[31]

Under illumination, the electron-hole pairs are generated due to absorption of photons with photo energy higher than the band gap of the semiconductor materials. Clearly in our case the enhanced photocurrent is due to the photo-generated charge carriers. For reverse bias, the majority carriers experience a large barrier. At the same time, the photo-generated electrons in Si core are transferred to the conduction of CdS and collected immediately by the positive electrode and the holes generated at the valence band of CdS are

collected by the negative electrode, minimizing the probability of recombination of the carriers. Thus a high ratio of photo to dark current is achieved. On the other hand, in the case of forward bias, the device is already in the ON state at 0.5V. Therefore, only the extra charge carriers due to photons contribute to the increase in the current. Thus, the differential increase in the current is expected to be much higher in the reverse bias case.

The CdS/Si nanowire core/shell heterojunctions were tested for photo-sensor application by taking its time dependent photo-response to a solar simulator (AM 1.5G i.e. 100mWcm^{-2} illumination) measured in air and at room temperature under reverse bias of -1V, six repeated cycles are displayed in Fig.6 (b). The increase in photo to dark current is clearly observed, and no obviously degenerate effect was found during the detecting process.

Based on the above experiments, it recalls me that rectifying effect enhancement is due to the improved crystallization and decrease of deep defect states present in CdS shell, but the presence of surface defect states in CdS shell explains the absence of the photovoltaic effect in our case although there are no reports on the CdS/SiNWA solar cell based on SILRA. The enhanced rectifying effect and obvious photo-response enable the application of CdS/Si nanowire arrays in the field of photo-electronics. All these results indicate that the CdS/Si nanowire arrays have a great potential in nano photo-electronics device applications.

4 Conclusions

In summary, large-scale and well-aligned CdS/Si core/shell NWAs are prepared using a facile solution method. The SiNWAs are prepared on silicon substrates by metal chemical etching method. Moreover, CdS shells are coated on SiNWs to form shell/core structures using the SILAR method. The experiment results indicate that I-V characteristic can be tailored effectively by changing the number of SIALAR cycle, CdS/SiNWA with 40cycles has good rectifying characteristics, obvious unidirectionality, and the small leakage current. Moreover, the electron transport across CdS/SiNW is also discussed. Obvious photo-response is observed, which indicates this structure can be used as photo detectors. We expect that our solution based approach for the fabrication of CdS/Si core/shell nanowire arrays will be applicable to the synthesis of various novel heterostructures for nano photoelectronic devices such as rectifying diodes, light-emitting diodes and solar cell in the future.

Acknowledgements

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A table of contents entry

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