Volume 1 | Number 1 | Jan 2013 | Pages 1–100

Journal of
Materials Chemistry C

Materials for optical and electronic devices
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A Two-Step Annealing Process for Enhancing the Ferroelectric Properties of poly(vinylidene fluoride) (PVDF) Devices

Ji Hoon Park[1], Narendra Kurra[1], M. N. AlMadhoun[2], Ihab N. Odeh[2], and H. N. Alshareef *[1]

[1] *Materials Science & Engineering, King Abdullah University of Science and Technology (KAUST), Thuwal 23955-6900, Saudi Arabia*

[2] *Corporate Research and Innovation Center, Saudi Basic Industries Corporation (SABIC), Thuwal 23955-6900, Saudi Arabia*

ABSTRACT

We report a simple two-step annealing scheme for the fabrication of stable non-volatile memory devices employing poly(vinylidene fluoride) (PVDF) polymer thin-films. The proposed two-step annealing scheme comprises the crystallization of the ferroelectric gamma-phase during the first step and enhancement of the PVDF film dense morphology during the second step. Moreover, when we extended the processing time of the second step, we obtained good hysteresis curves down to 1 Hz, the first such report for ferroelectric PVDF films. The PVDF films also exhibit a coercive field of 113 MV/m and a ferroelectric polarization of 5.4 $\mu C/cm^2$.

KEYWORDS: ferroelectric polymer; poly(vinylidene fluoride) ; annealing; solution process; low-cost process

Phone: +966-(0)12-808-4477 e-mail: husam.alshareef@kaust.edu.sa

Journal of Materials Chemistry C Accepted Manuscript

INTRODUCTION

Information-storage devices fabricated with ferroelectric polymers have recently attracted research attention because of their potential use as elements of nonvolatile, transparent and flexible memory devices on glass or plastic substrates.[1~5] One of the major advantages of ferroelectric polymers is their solution compatibility, which makes fabricating memory devices based on ferroelectric polymer using low-cost processes possible. Poly(vinylidene fluoride) [PVDF] and its copolymer with trifluoroethylene (TrFE), PVDF-TrFE, are the most widely investigated ferroelectric polymers due to their good polarization, solvent compatibility, and ease of obtaining the beta phase.[1~7] Synthesis of the copolymer remains time consuming and expensive; suggesting that, further research on the less resource intensive ferroelectric PVDF thin film is needed.[8] PVDF has other advantages such as better thermal stability due to higher Curie point and lower solubility in solvents, which allows for more flexible multilayer device integration, especially when involving solution processing.

A few papers have discussed the preparation and application of neat PVDF thin film by conventional spin coating or by the wire-bar coating method.[9~15] The focus of these past studies was on the preparation of smooth thin films that would be suitable for microelectronic applications [9,10,14], or on achieving a ferroelectric phase (beta-, gamma-, or delta-phase).[9,11~13, 15] The beta, and gamma phase (expressed in conformational sequences of TTTT, and TTTG, respectively) are most popular polar phases and are generally desired for information-storage devices. However, first, in order to achieve the beta-phase PVDF thin film, one needs to blend the PVDF with other polymer followed by quenching process, which is not desirable for large area electronics.[11] Second, direct formation of beta phase PVDF thin film is possible with very limited substrates (e.g., Au-coated substrate).[13] Here, we report the preparation of PVDF thin

films (200 nm) with gamma phase by means of simple two-step annealing process. The stable operation of the non-volatile memory with the gamma phase PVDF thin-film at various operating frequencies is demonstrated. In contrast, previous studies on PVDF thin film devices did not provide necessary frequency-dependent hysteresis data of the PVDF thin film devices, such as the coercive field and the remnant polarization. For instance, using hysteresis parameters measured at 1 kHz to predict device behavior at 50 ~ 60 Hz (50 Hz in Europe, and 60 Hz in America, and parts of Asia) is inappropriate. In the work reported here, we present a processing scheme that allows us to fabricate a ferroelectric gamma-phase PVDF thin-film with good hysteresis parameters in various frequency ranges (from 1 Hz to 1 kHz) based on an Au/PVDF thin film/Pt capacitor structure. We fabricated this thin film by using a two-step annealing process, above and below the melting temperature (T_m) of PVDF. The annealed PVDF thin films transform to the gamma phase during the first annealing step from their initial paraelectric alpha-phase. Subsequently, a densely packed morphology is established in the second annealing step, without affecting the crystallization of the gamma phase.

EXPERIMENTAL

PVDF powder (Aldrich, Mw = 534,000 g/mol) was dissolved into dimethylformamide solvent (Aldrich) to prepare the solution, and then the solution was filtered using a polytetrafluoroethylene filter (1 μm pore size). To create the capacitors, we sputter deposited a bottom electrode composed of 25 nm-thick Pt (25 nm)/ Ti (5 nm) on SiO_2 (100 nm)/silicon. A 200 ~ 250 nm uniform PVDF thin-film was deposited by spin-coating inside a N_2 gas filled glove box at 4000 rpm for 60 s with 5.1 ~ 5.5 wt.% concentration. Prior to the spin-coating, the PVDF solution was stirred and heated at 110 °C using a conventional hot-plate for ~20 min to

completely dissolve the PVDF.[16] This heating of the PVDF solution ensured that the spin-coated PVDF thin-films would be uniform. After spin-coating of the PVDF thin film, the sample was baked on hot-plate at 150 °C for 2 hrs inside the glove-box to render the thin-film solvent free. This annealing step was completed before the deposition of the Au top-electrode, and we call it the pre-electrode annealing step. A 90 nm Au top-electrode was then deposited on the thin-film by thermal evaporation through a shadow mask. For the initial 10 nm, Au was deposited using a 0.1 Å/s deposition rate, followed by a 1 A/s rate for the remaining 80 nm. The fabricated Au/PVDF/Pt capacitors were then annealed at 180 °C on a conventional hot plate for ~10 to 30 min (hereafter referred to as the transformation annealing (T-ANNL) step. Next the temperature was maintained below the melting point of PVDF for ~10 to 50 min (hereafter referred to as the densification annealing (D-ANNL) step. Scanning Electron Microscopy (Quanta 600 FESEM) was used to characterize the surface of the film. The ferroelectric phase was analyzed using Fourier-transform infrared spectroscopy (FT-IR, ThermoScientific Nicolet iS10). Polarization-voltage measurements were conducted using the Premier Precision II ferroelectric tester (Radiant Technologies Inc.).

RESULTS AND DISCUSSIONS

Figure 1 shows comparative crystallization results for the PVDF films (at 180 ºC, T-ANNL) before and after deposition of the top Au electrode. Figure 1(a) shows a scanning electron microscope (SEM) image of the Au/PVDF/Pt device in which the PVDF film was crystallized (pre-electrode annealing) before deposition of the top Au electrode. As revealed in the figure, this PVDF film exhibits the typical spherulitic morphology of the paraelectric alpha-phase [9,10,15,17], with a grain size of around 3 to 6 μm in diameter. The FT-IR spectra confirm the

existence of the alpha-phase as evidenced by the characteristic absorbance peaks at 612, 796, 1213 cm-1.[9,15,18] In comparison, we also studied the PVDF film crystallization on identical PVDF films after deposition of the Au top electrode. The T-ANNL step was performed at 180 °C for ~10 min, which is above the melting temperature of PVDF (167 °C) [13,15,19], followed by cooling to room temperature on a hot-plate. The Au/PVDF/Pt device was placed on the hot-plate which was already at 180 °C. To elucidate the effect of the presence of the top electrode during annealing, the top Au electrode was thoroughly removed by an Au etchant at room temperature after the annealing process.[20] Figure 1(b) displays the boundary (after removing the Au layer) between regions of the PVDF film that were covered by Au and the regions of the films that were not covered by Au during the annealing process. Figure 1(b) clearly shows a difference in morphology between the portion of the films where the Au-electrode existed and those that did not during the T-ANNL process. The area covered by the top electrode during the T-ANNL process appears to have a lamellar-like morphology right under the top Au electrode. It is expected that the PVDF film capped by a top Au electrode would experience phase-change during the T-ANNL process. We used FTIR to investigate the areas of the film where the Au layer was present or absent, as shown in Figure 1(b). The spectrum of the PVDF film under the Au electrode turns out to be in the gamma-phase (ferroelectric) as evidenced by the clear characteristic peaks at 840 and 1234 cm-1.[11,15,18] Interestingly, the PVDF film that was not covered by the Au electrode during the annealing is in the non-polar alpha-phase with and almost similar spectrum as that shown in Figure 1(a).

Based on the above results, it is expected that our PVDF capacitors will have different ferroelectric properties depending on the annealing process (annealing before deposition of the top electrode compared with annealing after deposition of the top electrode). Figure 2 shows the

polarization vs. electric-field (P-E) results for both cases. Even the film in which the alpha phase is dominant (the paraelectric phase) exhibits a hysteresis curve, and we attribute this hysteresis behavior to the formation of delta-phase of the PVDF film under an applied electric field that exceeds the coercive field value.[9,10,17,21] The coercive field (E_c) is not clearly defined before the T-ANNL process. Instead, the E_c gradually increases according to the applied electric field (until 360 MV/m). This larger E_c value compared with reported coercive voltages of the beta- or gamma-phase is attributed to the presence of the alpha-phase whose permanent polarization is less favorable with respect at low voltage due to its paraelectric nature. In the samples that underwent the T-ANNL process (Figure 2b), the improved remnant polarization (3.7 $\mu C/cm^2$), operating electric field, and E_c (146 MV/m) along with better hysteresis shape, is due to the formation of the gamma-phase after the T-ANNL process. It should be noted that the thin gamma PVDF crystalline film in its preferred orientation is conducive to aligning the H-F dipole parallel to the b axis of the PVDF crystal, as suggested by its lower coercive voltage.

No reports in the literature exist on the low-frequency hysteresis behavior of PVDF. However, we found that with hysteresis measurements below 100 Hz, PVDF capacitors are unstable regardless of the annealing process. At lower measuring frequency, the yield is almost zero in both cases (pre-electrode annealing or T-ANNL). In fact, the top Au electrode is in general blasted by the increased electric field (see Figure S1).

These results clearly indicate the crystallization after deposition of the top Au electrode results in better PVDF film performance. In fact, good hysteresis loops could be measured down to 1 Hz. We also developed another useful annealing process. In this process, we applied a second annealing step (after the T-ANNL process) by heating the device to a temperature below the melting temperature of PVDF (at 150 °C) for holding it at this temperature for 30 minutes.

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We called this step densification annealing (D-ANNL). We tried this because heat treatment facilitates the rearrangement of polymer chains and anneals out any defects that may be present in the PVDF films. It also helps the chains to pack more closely together.[22,23] It should be noted that the D-ANNL time for 50 min is enough to achieve good P-E loops at 1 Hz.

After the end of the D-ANNL process, we measured the hysteresis loops in relation to frequency, as shown in Figure 3. Within the frequency range between 1 Hz to 1 kHz, the ferroelectric parameters such as E_c and P_r change with consistency. The coercive field increased from 113 MV/m to 163 MV/m, and the P_r value decreased from 5.4 $\mu C/cm^2$ to 2.8 $\mu C/cm^2$. Representative P-E loops obtained at various electric fields and measuring frequencies can be found elsewhere (See Figure S2). A very similar phenomenon was reported earlier and was modeled in inorganic ferroelectric thin films by the Kolmogorov-Avrami-Ishibashi (KAI) model[24,25]. However, to the best of our knowledge, our result is the first report regarding the frequency-dependence of the switching parameters in PVDF thin-films. Interestingly, it should be noted that the cooling rate between the temperature of T-ANNL and D-ANNL doesn't show any meaningful effect on the P_r, and E_c value (Please see the Figure S3).

This result leads us to wonder about the role that the D-ANNL process plays to improve the performance of PVDF films at low frequency. Figure 4 shows the SEM images of PVDF thin-films that crystalized under identical conditions (with the Au electrode in place) after the D-ANNL process lasting various times. The SEM images were taken after the complete removal of the top Au electrode by a gold etchant. As shown in Figure 4(a), nano-sized cracks exist in the PVDF films that did not undergo the D-ANNL process. However, these cracks are effectively reduced when the PVDF film was treated with the D-ANNL process at 150 °C for 70 min. To determine any potential phase-change from the initial ferroelectric gamma-phase (obtained after

phase-transformation, T-ANNL, as shown in figure 1b), we again examined the FTIR spectra of each sample (Figure 4(a) - (c)). Interestingly, as shown in Figure 4(d), the characteristic peaks of the gamma-phase with respect to annealing time did not change. The two consecutive annealing processes below the melting temperature of PVDF effectively increases the density of the PVDF film without changing the gamma-phase of the PVDF thin film. We also measured the thickness change before/after the D-ANNL step by surface profiler. It shows a thickness of 203 ± 5 nm for the sample without D-ANNL step, and 196 ± 3 nm for the sample after the D-ANNL. The volume reduction of $\sim 3.4\%$ is achieved after D-ANNL process, indicating that some film densification has taken place. At lower measurement frequency, the exciting voltage approaches a direct current (DC) measurement, which is a more severe test condition of the PVDF capacitor, which can be expected to increase the leakage current of the device. Our two-step annealing process allows the characterization of PVDF devices even down to 1 Hz as shown in Figure3, indicating the improved leakage current characteristic after the D-ANNL process. It should be noted that lower leakage current is normally associated with lower defect density and more dense films.

A summary of the annealing scheme and its impact on the ferroelectric properties of PVDF-based devices is shown with a time-temperature-transformation curve in Figure 5. The alpha-phase is typically obtained using standard film processing techniques, such as spin-coating, presumably due to the fact that the alpha-phase of PVDF is the most thermodynamically stable phase. However, with our Au-capped crystallization above T_m, the capacitor structure can be regarded as a 'polymer melt confined between two plates' model, which has been widely investigated by dynamic Monte Carlo simulation .[26,27] According to this model, the ability of the polymer chain near the metal plate to reorient is hindered. Therefore, the polymer chain tends to

be aligned in a direction parallel to the plate.[19,28] Kang et al. has also verified that the c-axis of the gamma PVDF crystal is predominantly parallel to the surface by means of two-dimensional (2D) grazing incident X-ray diffraction.[15] We surmise that this gamma-phase nucleation of the Au layer propagates into (from the top Au layer to the bottom Pt electrode) bulk PVDF during the cooling process (red line of Figure 5(a)). However, the solidified gamma-phase PVDF film actually has nano-size cracks on the PVDF in its initial state, so that when we perform the D-ANNL process consecutively (blue line of Figure 5(b)) the cracks reduce. This D-ANNL process causes no phase-change of PVDF, but only affects its morphology. This two-step annealing scheme yields PVDF films with stable ferroelectric performance down to 1 Hz.

CONCLUSION

In summary, we have fabricated Au/gamma-phase PVDF/Pt capacitors using a simple two-step annealing process. The densely packed gamma-phase PVDF capacitor leads to good hysteresis behavior at frequencies as low as 1 Hz. The ferroelectric capacitors with PVDF film displayed a coercive field value of 113 MV/mm and a remnant polarization value of 5.4 $\mu C/cm^2$ at 1 Hz. We thus believe that the ferroelectric capacitors processed by our two-step annealing process are promising for ferroelectric, non-volatile memory applications.

CONFLICT OF INTEREST

The authors declare no competing financial interests.

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by subsequent rinsing with DI water. We found that this etching process doesn't impose any damage on the PVDF film surface.

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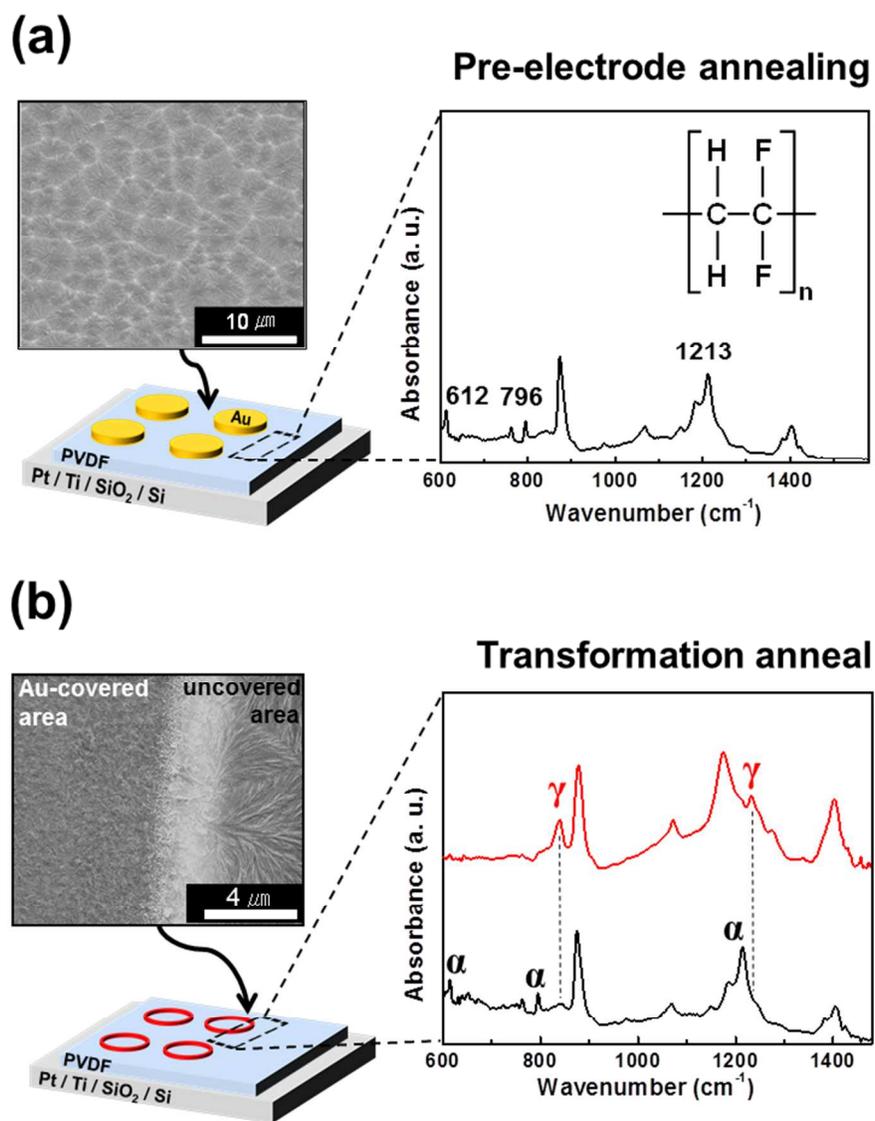28.   H. Li, S. Yan, *Macromolecules* 2011, **44**, 417.

Figure 1. (a) SEM images and FT-IR spectra of a thin PVDF film after the pre-annealing process. The characteristic absorbance peaks at 612, 796, 1213 cm^{-1} indicate the presence of the alpha-phase of PVDF. The inset shows the chemical structure of PVDF. (b) SEM images and FT-IR spectra of thin PVDF films after T-ANNL. The characteristic absorbance peaks at 840, 1234 cm^{-1} indicate the presence of the gamma-phase of PVDF induced by T-ANNL. The circle-type Au electrode was removed by an Au etchant. A clear boundary is shown in the SEM image.
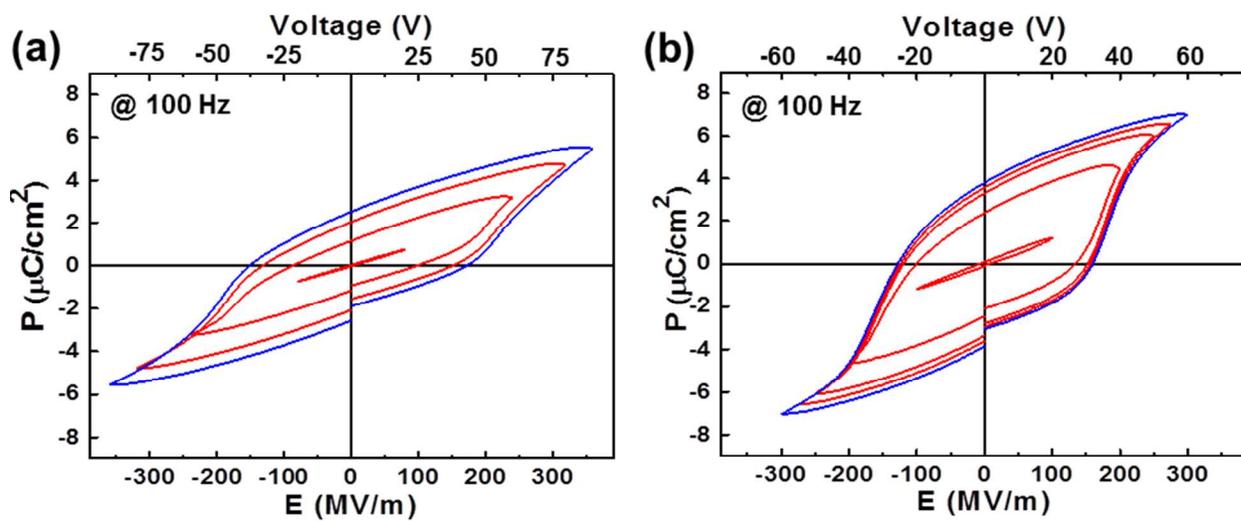
Figure 2. (a) Representative P-E curves of the Au/PVDF/Pt structure measured (a) before T-ANNL, and
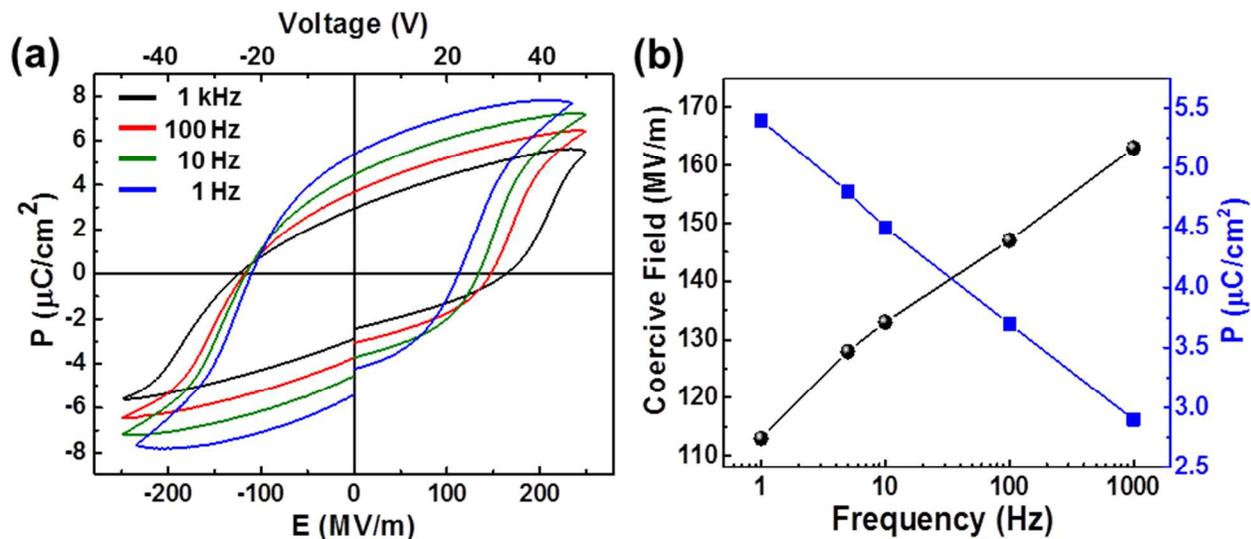
(b) after T-ANNL.

Figure 3. (a) Representative P-E curves of the Au/PVDF/Pt structure measured at various measuring

frequencies (1 Hz to 1 kHz). (b) The summary of E_c, and P_r values for each measuring frequency.
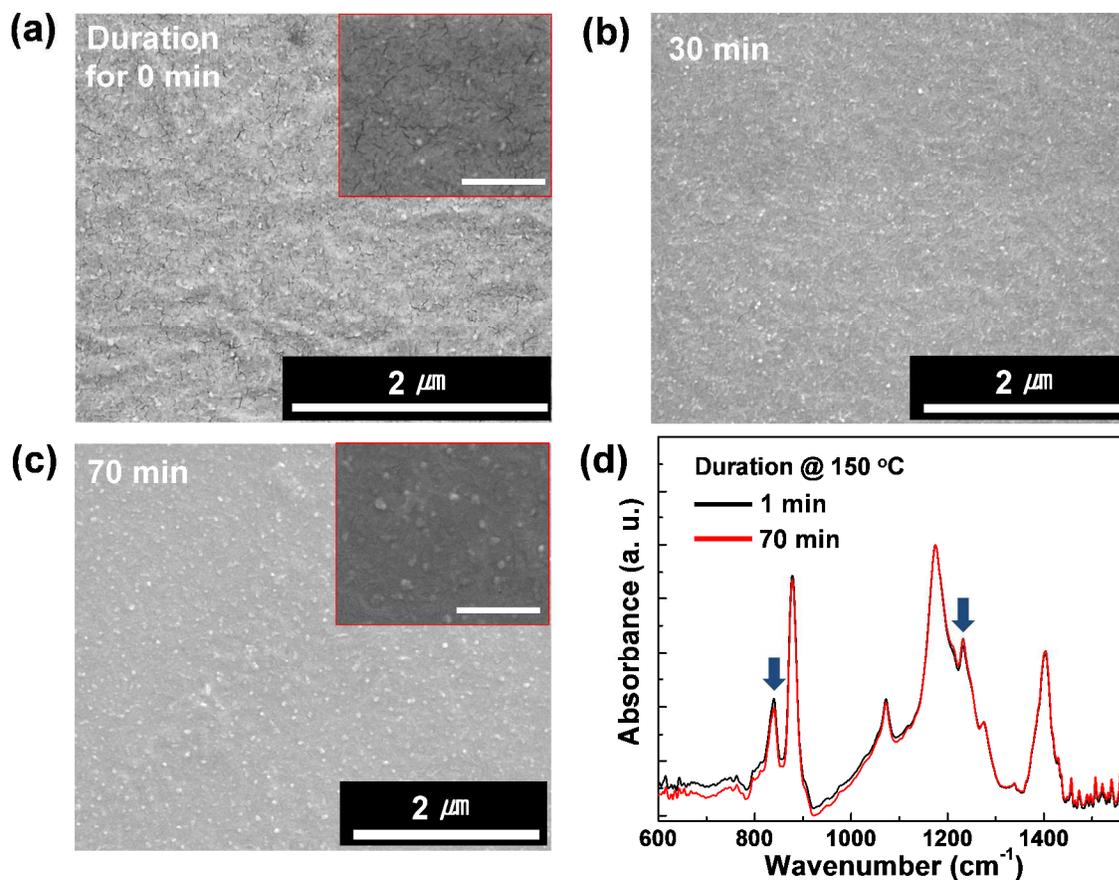
Figure 4. (a) - (c) The evolution of the surface morphology of a PVDF film capped with an Au electrode with respect to the duration time of D-ANNL. The inset shows a crack on the surface of the PVDF film, which disappeared after D-ANNL. The scale bar of the inset is 500 nm. (d) The FT-IR absorbance spectra of the films underwent D-ANNL for 1 and 70 min, respectively. The characteristic absorbance peaks indicated by arrows (840, 1234 cm^{-1}) of both spectra (black, red) shows no further improvement of gamma-phase.
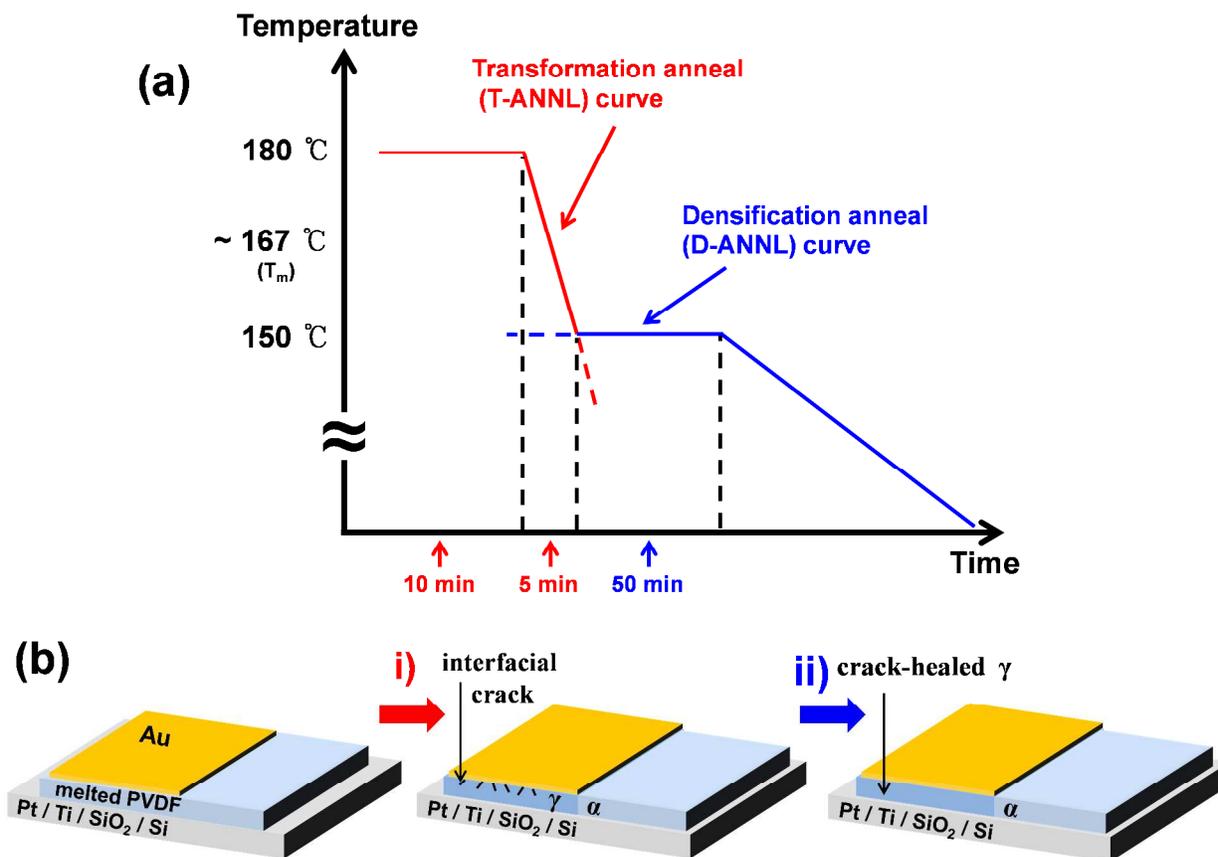
Figure 5. (a) A Time-Temperature-Transformation curve for the PVDF layer during T-ANNL and D-ANNL. (b) A schematic illustrating each step of the annealing processes.

TOC Image