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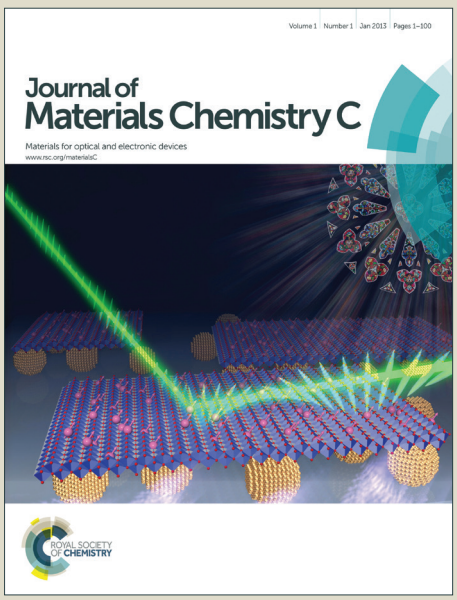

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Graphical Abstract

MoS_2 Nanosheet Channel and Guanine DNA-base Charge Injection Layer for High Performance Memory Transistors

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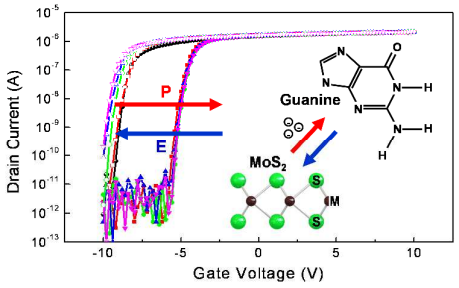

Charge injection memory transistors are promisingly demonstrated according to the unique properties of MoS_2 nanosheet channel and guanine trapping layer.

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DNA polymers have been studied in research area of information and nano-technology as well as biotechnology with such a variety of benefits as natural plenitude, biodegradability and low toxicity. Here we demonstrate a charge injection type non-volatile memory field-effect transistor (FET) with one of DNA-base small molecule, guanine, which is coupled with MoS_2 nanosheet channel as a trapping or charge injection layer material. Thanks to the unique properties of guanine layer and extremely thin MoS_2 nanosheet, our non-volatile memory MoS_2 FETs exhibit more than 3 V memory window under 35 V/-15 V gate voltage pulse for Program/Erase (or trapping/detrapping), maintaining a high Program/Erase ratio of ~10^3 for longer than 1000 s at least. Superior dynamic Program/Erase cycles were performed with memory inverter comprised of two memory FETs connected in series. Such non-volatile memory properties have been mostly well observed even after 45 days, since the trapped electrons charges were stably stored in guanine layer.

Introduction

Recently, DNA polymer and its components of DNA-base small molecules have extended their fields to information- and nano-technology according to their own benefits of natural plentitude, biodegradability, bio-functionality, low cost, and low toxicity.[1-5] Based on these advantages, many research groups have been showing the possibilities toward building blocks of various device applications such as light emitting diode, transistor, and solar cell.[6-10] In our previous report,[11] we applied one of DNA-base molecules, guanine ($C_5H_5N_5O$) as hydrogen getter and charge trapping layer for amorphous InGaZnO field effect transistor (FET) where stable trapping action by injection voltage pulse was achieved as the guanine was inserted between gate dielectrics. Unfortunately, charge detrapping by opposite voltage pulse was never efficient with the oxide thin-film FETs, since any ejection voltage (for detrapping) should be divided into two portions for the channel layer thickness (~50 nm) and the gate dielectric; if the channel thickness is ultrathin, such voltage would drop only through the gate dielectric thickness. In order to support such detrapping as well as trapping, extremely thin semiconducting channels are thus very necessary, so that non-volatile charge injection memory function may be efficiently achieved. As one of possible candidates for ultrathin semiconductor channel, 2-dimensional (2D) molybdenum disulfide (MoS_2) is the most attractive one which has the benefits of high mobility and on/off ratio from its bandgap over 1.2 eV.[12-23] MoS_2 has already been evidenced as the channel for such trapping and detrapping purposes but by only a few researchers;[24-25] the non-volatile memory device study adopting 2D channels and new trapping layer is still lacking, timely, and attractive in respect of theoretical/experimental confirmation and extended applications. Hence, in the present study, we have been motivated to fabricate and analyse the charge injection type non-volatile memory FETs and memory inverter by adopting guanine molecule and MoS_2 nanosheet as charge trapping layer and ultrathin channel, respectively. Atomic layer deposited (ALD) Al_2O_3 was used for both tunnelling and blocking dielectric layers in memory FETs.

Our non-volatile memory MoS_2 nanosheet transistor exhibited more than 3 V memory window under 35 V/-15 V gate voltage pulse for Program/Erase (or trapping/detrapping), maintaining a high Program/Erase ratio of ~10^3 for longer than 1000 s at least as its retention property. Superior dynamic Program/Erase cycles were performed with current signal by a memory FET, but also with distinct voltage signals by memory inverter comprised of two memory FETs connected in series. These retention properties have been mostly well observed from our memory inverter even after 45 days, since the trapped electrons charges were stably stored in guanine layer; such aging protection appears to be the main benefit of guanine as well matched to the non-volatile memory device.

Experimental

Device Fabrication

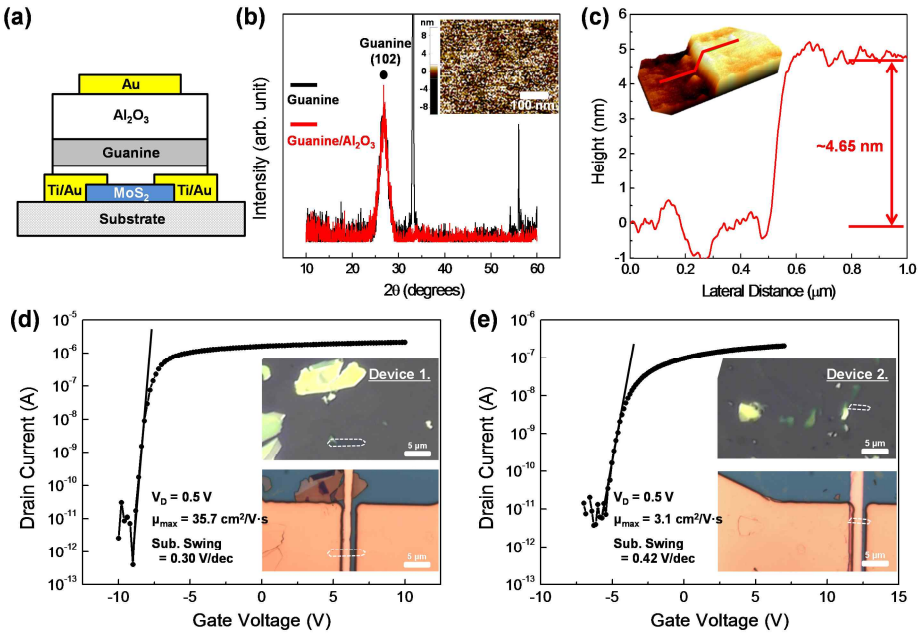

Figure 1. (a) Schematic cross section image of the MoS_2 nanosheet FET for non-volatile charge injection memory with embedded guanine charge trapping layer. (b) XRD spectra of 150 nm thick guanine layer grown on Si wafer before (black line) and after (red line) Al_2O_3 deposition. Both of the guanine layers show a monoclinic crystal structure with the same maximum intensity at the 2θ of 26.8° indicating the preferred orientation of (102) plane. The inset of AFM image shows small grain size as ~5 nm which should be related to the peak broadening of XRD spectra, and it also shows RMS roughness of guanine surface as ~1.8 nm. (c) Cross-sectional height profile of MoS_2 nanosheet as scanned along the red line in the inset AFM image. Transfer characteristics of MoS_2 nanosheet FETs for (d) Device 1 and (e) Device 2. The inset optical microscopy images are showing the mechanically exfoliated MoS_2 nanosheets before and after device fabrication.

A few nanometre-thin MoS_2 nano-flakes were exfoliated and transferred from bulk MoS_2 (SPI supplies, natural molybdenite) on highly-doped p^{++}-Si/285 nm SiO_2 substrates using standard scotch tape method. Then the optical microscope was used to trace the flakes and to conjecture the number of layers, which would be later precisely characterized by atomic force microscopy as shown in Figure 1(c). The source and drain electrodes of Ti/Au (25 nm/50 nm) bilayer were deposited by DC magnetron sputtering system while those were patterned by conventional photolithography and lift-off process with the lift-off-layer (LOR 2000: Micro Chem) and photo-resist layer (SPR 3612: Micro Chem). The channel width/length ratios were defined to be 0.95 μm/2.6 μm for Device 1 and 0.6 μm/3 μm for Device 2 using the optical microscope image of inset of Figure 1(d) and (e), respectively. After that, the 5 nm-thin tunnelling and 40 nm-thick blocking Al_2O_3 layer were deposited by atomic layer deposition (ALD) system, and the 20 nm guanine charge trapping layer was inserted between them by thermal evaporation system. Considering the thermal limit of guanine layer in vacuum (we deposited the guanine layer at 200 °C in thermal evaporation chamber), ALD process was maintained at a temperature lower than 150 °C in vacuum (~0.5 Torr). The top gate-electrode of Au (50 nm) was deposited and patterned as the source/drain electrodes. The memory inverter device was then fabricated by interconnecting Al wire.

Film Thickness, X-ray Diffraction, and Surface Morphology

The film thickness of guanine and Al_2O_3 films was measured by using a mechanical profiler (alpha-step) and optical ellipsometry method, respectively. Crystalline property and surface morphology of our guanine layer was investigated by Cu-Kα X-ray diffraction (XRD) and atomic force microscopy (AFM) after the guanine was deposited on a Si wafer. Details of XRD result and AFM image are shown in Figure 1(b) and its inset.

Electrical Measurement

The device current-voltage (I-V) characterizations were carried out with semiconductor parameter analyser (HP 4155C, Agilent Technologies), function generator (AFG 310, Sony/Tektronix) and oscilloscope (TDS 210, Tektronix).

Results and Discussion

Schematic cross section of our top-gate MoS_2 nanosheet FET for non-volatile charge injection memory is illustrated in Figure 1(a), where the MoS_2 nanosheet was attached on p^{++}-Si/SiO_2 by mechanical exfoliation method and was followed by 100 °C ALD process for 5 nm-thin tunnelling Al_2O_3. Guanine (20 nm thick) and 40 nm-thick blocking Al_2O_3 layers were then sequentially deposited by thermal evaporation and ALD. According to X-ray diffraction (XRD) analysis of Figure 1(b), the guanine layer before and after Al_2O_3 deposition exhibit the same intensity at the same 2θ of 26.8 °, indicating that the monoclinic guanine maintains a preferred orientation of (102).[26-27] The peak broadening should be related to the small grain size (~5 nm) in guanine layer,[28] whose surface is shown in the inset atomic force microscopy (AFM) image. The thickness of MoS_2 layers are also characterized by AFM, turning out to be ~4.65 nm corresponding to ~7 layers for FET Device 1 as shown in Figure 1(c) (and ~11 layers were examined by AFM for

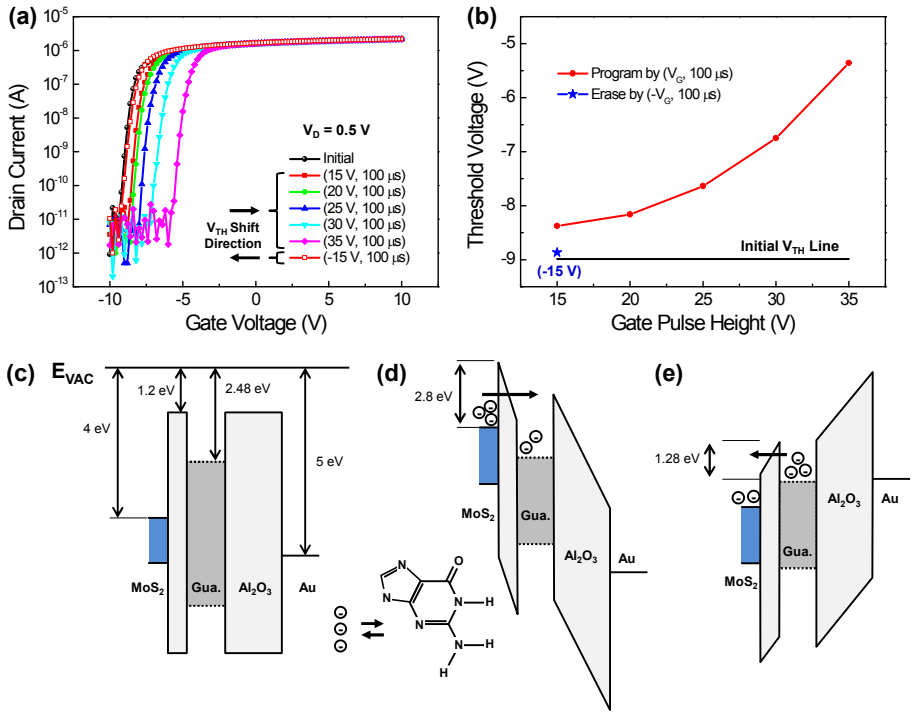

Figure 2. (a) Transfer characteristics of the Device 1 with guanine layer under the various gate voltage pulse height: V_G = 0 (initial), 15, 20, 25, 30, 35, and -15 V (after 35 V) under a constant pulse width (100 μs). (b) Gate pulse height versus V_{TH} plot; V_{TH} was defined by I_D current of 1 nA. Schematic band diagrams of our MoS_2 nanosheet FETs with guanine charge trapping layer under three conditions: (c) before V_G pulse, (d) after $+V_G$ pulse (trapping), and (e) after $-V_G$ pulse (detrapping). See the dotted line in HOMO and LUMO levels that indicates discontinuous organic guanine band. Inset between the band diagrams of (c) and (d) shows a guanine molecule layer that is trapping/detrapping electrons.

Device 2 although the data is not shown here). The transfer characteristics (drain current-gate voltage; I_D-V_G) of our Device 1 and 2 are shown in Figure 1(d) and (e), respectively, exhibiting the maximum linear mobility and sub-threshold swing as 35.7 cm^2/Vs and 0.30 V/dec for Device 1 while those are respectively 3.1 cm^2/Vs and 0.42 V/dec for Device 2. For both FETs, their on/off I_D ratios were higher than ~10^4. The optical microscopy images of our memory device are displayed in the insets of Figure 1(d) and (e), where white dashed lines indicate the mechanically exfoliated MoS_2 nanoflakes before and after device fabrication. (Figure S1 in ESI shows the output curves of our FET that evidence good ohmic behaviour with Ti/Au bilayer contact electrodes. Mobility difference between Device1 and 2 is related to the thickness and contact area of MoS_2 as discussed in details of ESI.)

Figure 2(a) displays the transfer curves of Device 1 which was electrically biased to the gate with various voltage pulse conditions: V_G = 0 (initial), 15, 20, 25, 30, 35, and -15 V (after 35 V) under a constant pulse width (100 μs) at a fixed drain voltage (V_D = 0.5 V). Since our 5 nm-thin Al_2O_3 plays as Fowler-Nordheim (FN) tunnelling barrier layer,[29-30] the accumulated electron charges in the thin MoS_2 channel should tunnel into guanine trapping layer in the presence of a sufficiently high positive electric field. These tunnelling phenomena result in threshold voltage (V_{TH}) shift toward positive gate voltages while the V_{TH} shift is mainly depending on the pulse voltage,[31] which is well displayed in both the transfer curves of Figure 2(a) and the pulse V_G vs. V_{TH} shift plot of Figure 2(b). According to the curves and plots, almost 4 V positive shift is obtained by +35 V gate pulse but the shifted voltage exactly go back to its original position by only -15 V gate pulse (voltages smaller than -15 V are too short to recover the original V_{TH}. Here, the V_{TH} was defined as the gate voltage when the I_D current reaches to 1 nA). It may be worthy of understanding why the trapping (charge injection) voltage should be larger than that for the detrapping (charge ejection). We thus prepared respective schematic band diagrams for the memory device under three conditions as seen in Figure 2(c), (d), and (e): before V_G pulse, after $+V_G$ pulse (trapping), and after $-V_G$ pulse (detrapping). (The band energy levels of DNA-base guanine layer and a few nm-thin MoS_2 were from previous reports.[11, 32-34]) Simply because the lowest unoccupied molecular orbital (LUMO: ~2.48 eV) of guanine layer is much higher than the conduction band edge of thin n-channel MoS_2 (~4 eV), it is highly likely that backward FN tunnelling for detrapping is much easier than FN tunnelling for trapping, requiring lower gate voltages as observed in the experiments. This means that non-volatile charge injection memory function can be achieved by asymmetrical bias pulsing. Here, we determined the two respective V_G of +35 and -15 V for trapping (Program) and detrapping (Erase). Although, such detrapping by gate pulse is easier than trapping, the trapped electrons may not travel easily within the trap layer because the constant LUMO energy states of organic guanine layer are discontinuous in real space unlike the conduction band edge of inorganic layer (as indicated by dotted line in the band diagrams). The asymmetrical Program and Erase voltages (+35 and -15 V, or corresponding electric(E)-fields), as illustrated in Figure 2(c) ~ (e), can be explained in view of Fowler-Nordheim tunnelling current density (J_{FN}) equation described below,[35]

$$J_{FN} = \frac{A}{\Phi_B} E_{ox}^2 \exp\left(-\frac{B\Phi_B^{3/2}}{E_{ox}}\right)$$

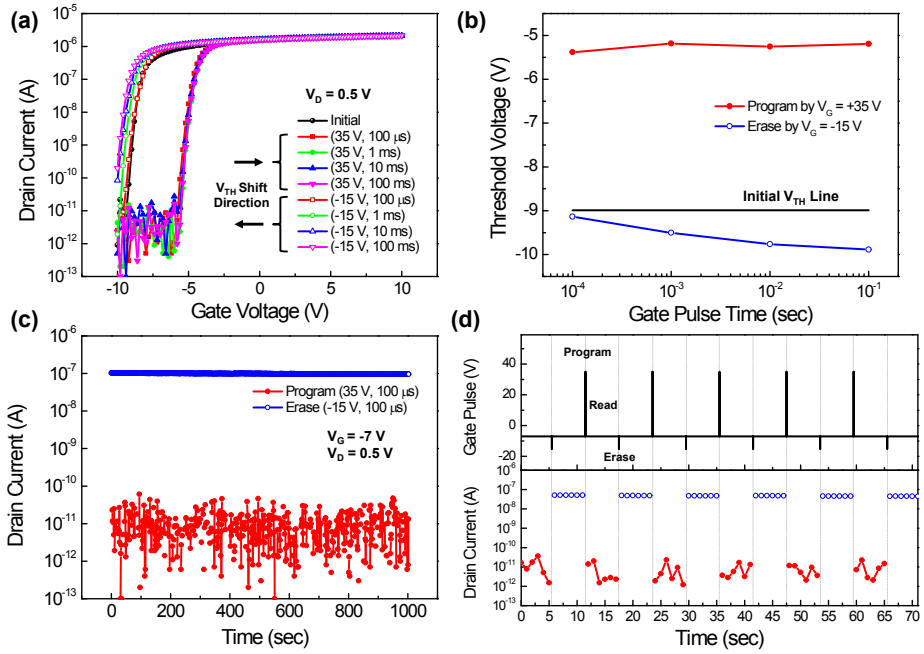

Figure 3. (a) Transfer characteristics of the Device 1 with guanine layer under the various gate voltage pulse time: 100 μs, 1 ms, 10 ms, 100 ms under constant pulse height of 35 V (Program)/-15 V (Erase). (b) Gate pulse time versus V_{TH} plot. (c) Static retention property and (d) Dynamic Program/Erase properties with Program (V_G = 35 V, 100 μs), Erase (V_G = -15 V, 100 μs), and Read (V_G = -7 V, V_D = 0.5 V) conditions. Note Program and Erase at the input gate pulse-time plot, and also note Read for output reading signals.

where A and B are constants, Φ_B is the barrier height at the injection interface. Since the electron affinities of MoS_2, Al_2O_3, and guanine are respectively reported as 4.0 eV,[32-33] 1.2 eV,[34] and 2.48 eV,[11] the barrier heights at MoS_2/Al_2O_3 and guanine/Al_2O_3 interfaces are calculated to be 2.8 eV and 1.28 eV as displayed in Figure 2(d) and (e). This indicates that the applied E-fields (E_{ox}) to tunnelling oxide would be different each other for acquiring the same J_{FN} during trapping and detrapping; E_{ox} for trapping is larger since Φ_B for trapping is larger, so higher gate voltage pulses are demanded. In spite of some inconvenience due to asymmetrical pulses, non-volatile memory function is one of the great benefits that 2D MoS_2 channel can uniquely provide by way of FET device structure; unlike 2D semiconductor channel, a thin-film transistor channel such as organic or oxide film supports only trapping function in general.[36-39] It is because during detrapping the total V_G is broken down into two parts for the depleted channel and dielectric thickness while in trapping event the total voltage drops through the dielectric only. (Figure S2 in ESI shows such one way trapping function observed in the case of InGaZnO FET with guanine trap layer in more detailed manner).

On the one hand, the pulse width (time) appeared not as important as the pulse height (V_G value). According to pulse width-dependent transfer curves and V_{TH} plots of Figure 3(a) and (b), the V_{TH} shift is not much varied in the width range of 100 μs ~ 100 ms either for Program or for Erase state. So, the static (retention) and dynamic Program/Erase properties were measured by applying 100 μs pulse to Device 1 as respectively shown in Figure 3(c) and (d) for their results, where V_G and V_D of -7 and 0.5 V were maintained for current reading (Read). The Program/Erase (ON/OFF) current ratio appeared exceeding 10^3 and was maintained up to more than 1000 s without any current decaying, according to Figure 3(c). In Figure 3(d), such ON and OFF current levels are well reflected but in dynamical way, responding to the gate pulse cycle [Program(P)-Read(R)-Erase(E)].

After examining the basic charge injection memory properties of our non-volatile memory FETs, we extended our device study to a memory inverter application so that output voltage signals might be distinctly extracted out for Program and Erase states (the analogue Program/Erase current signal can be transformed into digital one). For the memory inverter, two transistors of Device 1 and 2 were utilized to respectively play as driver and load as connected in series by using wire bonding method, as shown in inset circuit of Figure 4(b). The red line of both FETs in the inset circuit symbolizes the guanine charge injection layer. The transfer characteristics of the two FETs are displayed in Figure 4(a), where the transfer curve of Device 2 (load) shows Erase state of the device while those of Device 1 (driver) display Program and Erase states. (V_{TH} shift characteristics of Device 2 FET almost follow those of Device 1 in the manner of pulse voltage dependencies as shown in Figure S3 and ESI.) According to the voltage transfer characteristic (VTC) curves of Figure 4(b) for the memory inverter, scanning input voltage (V_{in}) from -10 V to 0 V at a fixed supply voltage (V_{DD} = 0.5 V) clearly distinguishes digital 0/1 states, and a memory window as large as ~3 V is acquired by Program/Erase voltage pulses (+35/-15 V, 100 μs), which exactly reflects the V_{TH} shift of the driver transistor. Dynamic Program/Erase cycle tests were also implemented with our memory inverter circuit, where V_G and V_D of -7 and 0.5 V were maintained for output voltage (V_{out}) reading. As a result, quite stable cyclic Program/Erase voltage signals were read to be 0.5/0.1 V without degradation as shown in Figure 4(c).

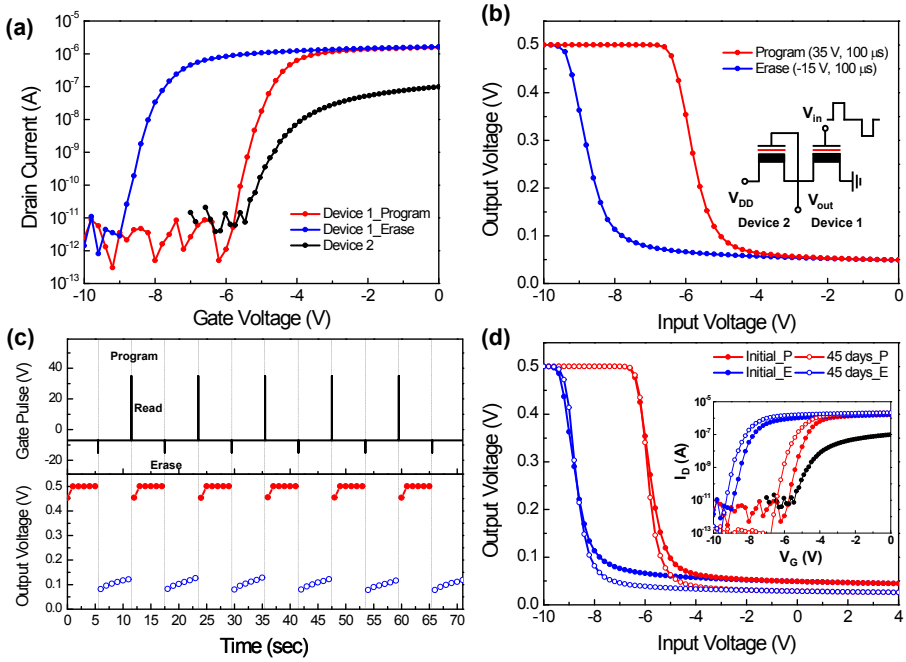

Figure 4. (a) Transfer characteristics of our load FET (Device 2) and driver FET (Device 1) with Program/Erase states. (b) Voltage transfer characteristics (VTC) curve of our memory inverter. The red line of both FETs in the inset circuit symbolizes the guanine charge injection layer. (c) Dynamic Program/Erase properties with same Program/Erase/Read conditions; note Program and Erase at the input gate pulse-time plot, and also note Read for output reading signals. (d) VTC curve of our memory inverter before and after 45 days aging in 25 ^{o}C-1 Torr state desiccator. Inset: Transfer characteristics before and after 45 days aging.

As a final characterization for our memory device, we implemented a device stability test aging the inverter device (comprised of two FETs) in 25 ^{o}C-1 Torr state desiccator for 45 days. According to the inverter VTC curves and transfer curves of Figure 4(d) and its inset, our memory device exhibits superior operational stabilities (non-volatility performance) against aging, showing almost the same memory window and only small deviations of V_{TH}s even after 45 days passed. We believe that such aging stability for non-volatile performance is attributed to the guanine trapping layer which would prevent the trapped electron charges from being leaked. This is quite understandable; since the constant LUMO energy states of organic guanine layer are discontinuous in real space unlike the conduction band edge of inorganic layer, the trapped electrons are not easy to travel but stay within the layer. (Figure S4 in ESI shows another transfer curve data obtained even after 110 days, according to which our FET further degraded but still appeared very operational.)

Conclusions

In summary, we have fabricated charge injection type non-volatile memory FETs and memory inverter by adopting guanine molecule and MoS_2 nanosheet for charge trapping layer and ultrathin channel, respectively. Our non-volatile memory MoS_2 nanosheet transistor exhibited more than 3 V memory window under +35/-15 V gate voltage pulse for Program/Erase, maintaining a high Program/Erase ratio of ~10^3 for longer than 1000 s as its retention property. The asymmetrical operation voltage for FN charge tunnelling originates from energy level discrepancies at the injection interfaces. Superior dynamic Program/Erase cycles were performed with current signal by a memory FET, but also with distinct voltage signals by memory inverter comprised of two memory FETs connected in series. Guanine layer worked as trapping layer and aging-protection agent as well, to support the non-volatile memory performance. We thus conclude that our memory device using ultrathin MoS_2 and guanine is very promising for high performance non-volatile performance.

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Notes and references

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