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Flexible One Diode-One Resistor Resistive Switching Memory Arrays on Plastic Substrates†

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Resistive random access memory (RRAM) has been developed as a promising non-volatile memory on plastic substrates for flexible electronic systems owing to its advantage of simple structure and low temperature process. Memory plays an important role in electronic systems for data processing, information storage, and communication, thus flexible memory is an indispensable element to implement flexible electronics. However, cell-to-cell interference existed in flexible memory array leads to not only undesired power consumption but also a misreading problem, which has been a big hindrance for practical flexible memory application. This paper describes the development of a fully functional flexible one diode-one resistor RRAM device. By integrating high-performance single crystal silicon diodes with plasma-oxidized resistive memory, cell-to-cell interference between adjacent memory cells is effectively prevented, and random access operation of the 1D-1R flexible memory device is successfully achieved on a flexible substrate. The work presented here could provide a useful methodology to realize the flexible non-volatile memory with high packing density for flexible electronic applications.

Introduction

System on plastic (SoP) has attracted attention as next generation electronics due to its advantages of outstanding portability, light weight, and convenient interfaces as compared to current electronic devices.[1-3] A flexible display for SoP is on the brink of commercialization, as flexible displays were demonstrated with several concept devices in the 2013 International Consumer Electronics Show (CES 2013).[4] However, in addition to the display, other parts of electronic devices such as the processor, energy source, and memory should be integrated into a single device on a flexible substrate to perform their respective functions in a SoP.[5-8] Among the many components of electronics, flexible memory is the main obstacle for realizing SoP, as it plays a significant role in electronic systems, including data processing, information storage, and communication with external devices.[8-10]

Resistive random access memory (RRAM) is considered as a promising candidate for flexible memory in SoP due to its advantages of simple structure, high-density integration, low temperature process, high-speed switching property, and low power consumption.[10-14] Several research groups have reported flexible resistive memory with a simple crossbar structure based on various materials such as GeO/HfON,[10] TiO_2,[15] SiO_x,[16] Al_2O_3,[17] Ag_2Se,[18] and polystyrene/carbon nanotube (PS/CNT).[19] Among many materials that have been developed for flexible resistive memory, plasma-oxidized binary metal oxides are of interest owing to their compatibility with a conventional micro-fabrication process.[17,20] Moreover, the plasma-oxidation process can provide uniform and reliable resistive switching materials on plastic substrates with high oxidation speed at low temperature. In spite of the strengths of plasma-oxidized metal oxides films, very few attempts have been made to apply them as flexible resistive memory.[17]

The major issue on flexible resistive memory is cell-to-cell interference occurring through leakage current paths during memory access operation; this is known as a cross-talk problem.[21-28] Since the cross-talk problem induces serious failure during memory operation, it limits memory size to just a few bits.[25,26] To fabricate a fully functional flexible memory, each memory cell must be integrated with a selection device, and thus they should be formed into one diode-one resistor (1D-1R)[24] or one transistor-one resistor (1T-1R) structure,[8] which has been a long term obstacle to achievement of SoP because of the absence of high-performance selection devices.[8]

In terms of integration, as in commercialized phase change memory,[29,30] a diode is preferred as a selection component over a transistor because the 1D-1R structure has advantages of small occupying area, simple design, easy fabrication, and high yield over the 1T-1R structure.[22-24] However, there are still unresolved issues with flexible diodes on plastic substrates,

such as insufficient current density for application as a selection element of memory. To achieve a high density flexible RRAM, the selection diodes should present a high forward current density exceeding 10^5 A/cm^2 and a high rectifying ratio over 10^6 for high packing density (>1 Mb),[24,25] but the previously reported selection diodes built on plastic substrates have not satisfied these specifications.[31,32]

Herein, we have developed a RRAM with a 1D-1R structure on a plastic substrate. High-performance flexible single crystal silicon diodes[33,34] were integrated with copper oxide based resistive memory[35] on a plastic substrate to prevent the cross-talk problem. The 1D-1R RRAM unit cells were interconnected with each other through word and bit lines in 8 × 8 arrays to control each memory unit cell independently.[8] Finally, the random access memory operation of 1D-1R RRAM on a flexible substrate was successfully performed by utilizing the integrated single crystal silicon diode with an excellent rectifying ratio (>10^5) and forward current density (>10^5 A/cm^2). The obtained results may open up new possibilities of realizing non-volatile memory with high packaging density for high performance flexible electronics.

Experimental

Fabrication process of flexible 1D-1R RRAM

The selection diodes used single crystal doped silicon nanomembranes as active layers. The fabrication began with definition of highly doped regions with boron and phosphorous on a p-type silicon on insulator (SOI) wafer with a 340 nm top Si layer and 1 μm buried oxide (SOITEC). Heavily n and p-doped regions were formed on a p-type Si layer (10 Ω·cm) by utilizing a spin-on-dopant (Filmtronic, P509) and boron implantation, respectively, and the SOI wafer was annealed in a rapid thermal annealing system. A photo-lithographically defined layer of SiO_2, deposited by plasma enhanced chemical vapor deposition (PECVD), was used as a doping mask. After doping, the underlying buried oxide was removed by a concentrated HF solution in order to release the ultrathin silicon membrane. Doped Si was transferred onto the 50 μm thick polyimide substrate (DuPont, Kapton) with a spin-cast PI precursor (Poly(amic acid), Sigma Aldrich) as a thermally curable adhesive. The PI precursor was fully cured at 250 °C for 1h in a nitrogen atmosphere. The diodes were then isolated by SF_6 plasma etching with active region of 300 × 150 μm^2 and cell-to-cell distance of 500 μm. The layers of Au/Cr (200 nm/10 nm) for metal contacts and Cu/Cr (250 nm/10 nm) for bottom electrodes were deposited respectively on anode and cathode regions of diodes using a radio-frequency (RF) sputtering and lift-off process. After the formation of Cu/Cr bottom electrodes, copper oxide was formed by oxygen plasma in an inductively coupled plasma-reactive ion etching (ICP-RIE) system at room temperature. Subsequently, the Al top electrodes with the active area of 50 × 50 μm^2 were formed in the same way as the bottom electrodes (see ESI† for details on the fabrication of a flexible RRAM on a plastic substrate, Fig. S1).

Measurement of the C-AFM sample

For sample preparation, the SET or RESET process of Al/Cu_xO/Cu memory was carried out, and then Al top electrodes were etched by an aluminum etchant. The reading process was performed at a voltage of 0.5 V in contact mode by an AFM equipped with a Pt/Ir-coated Si tip with arm length of 225 μm, width of 28 μm, and thickness of 3 μm.

Device Measurement

The electrical characterization of the flexible RRAM device was carried out with a probe station at room temperature using a Keithely 4200-SCS semiconductor characterization system equipped with a pulse measurement unit (Keithley 4225-PMU) and a remote amplifier/switch (Keithley 4225-RPM) for ultrafast pulsed I-V measurement.

Results and Discussion

Fig. 1a shows a schematic illustration of a flexible 1D-1R RRAM with 8 × 8 arrays on a plastic substrate. A flexible RRAM unit cell consists of a single crystal silicon diode as a selection device, and Al/Cu_xO/Cu layers deposited on the cathode region of the silicon diode for unipolar resistive switching. The selection diode is integrated to prevent cell-to-cell interference during memory operation by utilizing its rectifying property.[24] To fabricate single crystal silicon diodes as high performance selection devices of memory, single crystal silicon membranes, which had been doped at high temperature above 950 °C, were arrayed on a plastic substrate.[33] The Al/Cu_xO/Cu layers of metal-insulator-metal (MIM) structures were formed at the cathode region of the diode for resistance switching by radio frequency (RF) sputtering and O_2 plasma oxidation at room temperature.[35] Finally, all memory cells were interconnected with each other through word and bit lines in a passive matrix array for random access operation of the memory.[8] The resistive switching mechanism of the Cu_xO based unipolar memory can be explained by the formation and rupture of conductive filaments, as illustrated in the inset of Fig. 1a.[35,36] This plasma oxidized copper oxide has the advantage of being compatible with the standard complementary metal-oxide-semiconductor (CMOS) process, and it also provides a low temperature process that is suitable for flexible electronics.[17,20]

Fig. 1b shows a magnified optical image of the unit cells of the 1D-1R RRAM array. The word (WL) and bit lines (BL) cross each other to control the logic state change of each memory unit cell by forming a passive matrix. The inset of Fig. 1b shows a schematic cross-sectional view of 1D-1R unit cell on a plastic substrate. The anode region of the selection diode and the Al top electrode are connected to the WL and BL, respectively, and spin-cast SU-8 passivation layers provide an interlayer dielectric between the BL and WL. The integrated

diodes have a lateral structure in this study, but they can be converted to a vertical structure by adopting epitaxial silicon growth or well-controlled ion implantation, which can be applied to 1D-1R crossbar structure memory for larger array density.[24] Fig. 1c displays a photograph of the completed flexible 1D-1R RRAM on a 50 μm thick polyimide film with an active area of 1 × 1 cm^2. The inset shows good flexibility of the devices without any mechanical damage when rolled on a glass rod. All fabrication processes on a flexible substrate are carried out at low temperature under 300 °C, which offer stability to devices on plastic substrates.[37] Along with low fabrication temperature, ultrathin inorganic materials and the simple structure of the device can provide high flexibility as well as high performance on plastic substrates.[8,38]

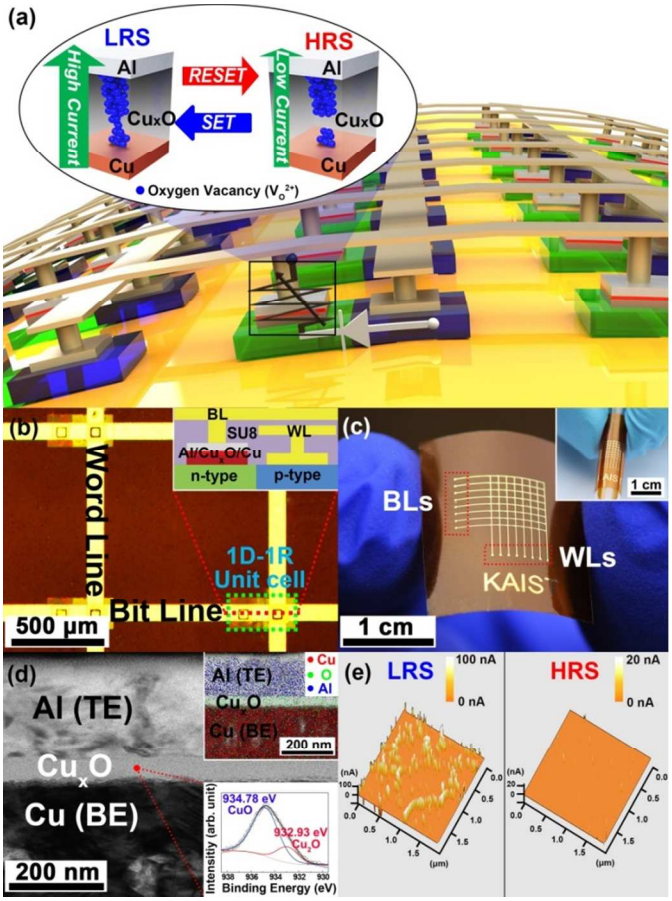


Fig. 1 (a) A schematic of 1D-1R flexible RRAM with an 8 × 8 arrays on a plastic substrate and corresponding circuit diagram of 1D-1R unit cell. The inset depicts the resistive switching mechanism of an Al/Cu_xO/Cu unipolar resistive memory. (b) A magnified optical image of the flexible RRAM unit cells. The inset shows a schematic cross-sectional view of a 1D-1R unit cell. (c) A photograph of a flexible RRAM device on a plastic substrate. The inset is a photograph of a flexible RRAM device wrapped on the surface of a glass rod with a diameter of 7 mm. (d) A cross-sectional BFTEM image of an Al/Cu_xO/Cu structure on a plastic substrate. The upper inset shows the TEM-EDX elemental mapping of Al (blue), O (green), and Cu (red). The lower inset shows the XPS spectrum of Cu $2p_{3/2}$ obtained from a plasma-oxidized copper oxide. (e) Mapping results of the current flow through the surface of Cu_xO/Cu with respect to the LRS and HRS measured by C-AFM.

Fig. 1d presents a cross-sectional bright-field transmission electron microscopy (BFTEM) image of the MIM structure (185 nm Al/37 nm Cu_xO/233 nm Cu) on a plastic substrate. The existence of a copper oxide layer between the top Al and Cu layers can be confirmed through TEM energy dispersive X-ray spectroscopy (EDX) elemental mapping of Al (blue), O (green), and Cu (red) in the upper inset of Fig. 1d. The composition analysis of Cu_xO was conducted by X-ray photoelectron spectroscopy (XPS), as shown in the lower inset of Fig. 1d. The main peak (blue line) at 934.78 eV and a shoulder (red line) at 932.93 eV respectively correspond to CuO and Cu_2O; these results indicate the coexistence of CuO and Cu_2O in the Cu_xO layer.[20]

For verification of the localized filamentary switching characteristics of copper oxide based resistive memory, conductive atomic force microscopy (C-AFM) was used to analyze the current distribution in the low resistance state (the LRS) and high resistance state (the HRS). Fig. 1e shows current maps of Cu_xO surface in the LRS and HRS obtained by C-AFM using a Pt/Ir-coated conductive Si tip. The C-AFM tip scanned over an area of 2 × 2 $μm^2$ of Cu_xO in contact mode with a reading voltage of 0.5 V. In Fig. 1e, numerous localized high-conductive spots are observed in the LRS, but the conductive peaks in the HRS are very weak and sparse. These results support the conductive filamentary path model in the copper oxide based memory where the resistance state is determined by the formation and rupture of localized filaments.[27,36]

Fig. 2a shows the I-V characteristics of the single crystal diode used as selection device of the memory. The integrated diodes exhibit high-performance electrical properties with a high rectifying ratio of 10^5 at ±1 V and a current density of 10^5 A/cm^2 in the forward bias region. The selection devices have sufficient current output to operate unipolar switching memory on plastic substrates where high current over a few mA is needed to cause rupture of conductive filaments.[24] Furthermore, specifications of this selection diode will be theoretically applied to a high array density memory over 1 Mb.[25] Fig. 2b shows the typical Cu_xO-based unipolar memory switching behavior after a forming process (see Fig. S3 in ESI† for the forming process of resistive memory). The resistance state of RRAM switched to the HRS at 0.6 V, as the voltage is swept from zero to a positive voltage: the RESET process. By sweeping the applied voltage on the top electrode with current compliance of 1 mA, the device is returned from the HRS to the LRS at 2.3 V: the SET process. The upper inset in Fig. 2b shows linear I-V characteristics of Al/Cu_xO/Cu resistive memory in positive and negative voltage regions, indicating that our resistive change material shows unipolar resistive switching where the resistance state switching is independent of the voltage polarity.[13] It is interesting that the resistances of the HRS and LRS decreases with increased temperature, as presented in the lower inset of Fig. 2b. This resistance behavior implies that the conduction mechanism in the LRS is dominated

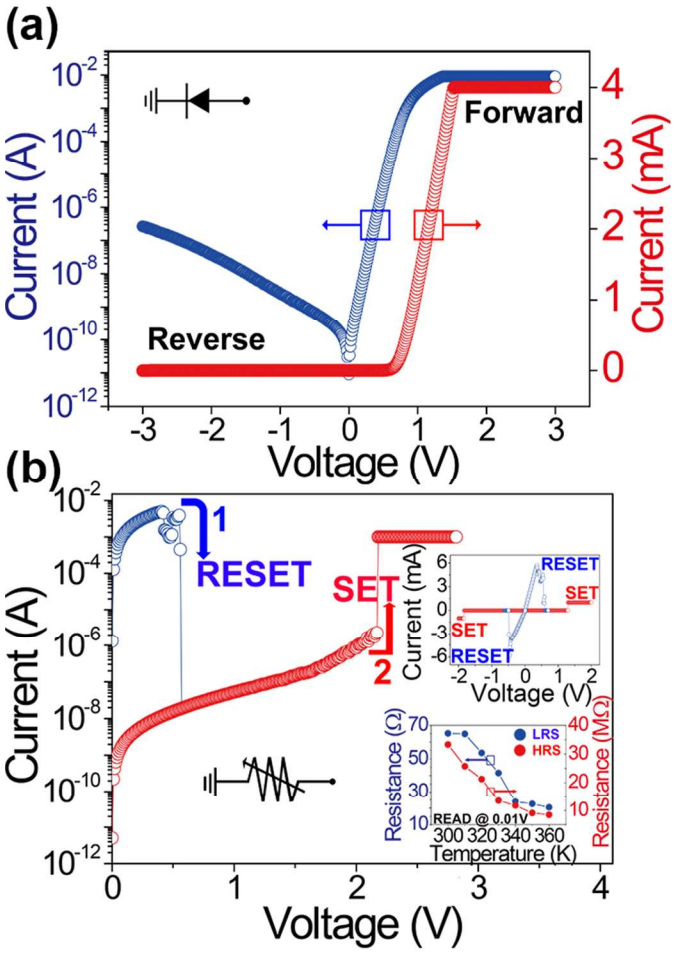


Fig. 2 (a) Output performance and circuit diagram of a single crystal silicon diode used as a selection device on a plastic substrate. (b) I-V characteristics of Cu_xO based unipolar memory and its circuit diagram. The upper inset shows linear I-V characteristics of an Al/Cu_xO/Cu resistive memory. The lower inset presents the temperature-dependence trend of the LRS at 0.01 V, showing that the ionic conduction mechanism may be dominant in the LRS.

by ionic filaments that are typically composed of oxygen vacancies, not metallic filaments.[39,40]

In order to characterize the 1D-1R unit cell in 8 × 8 arrays, electrical properties were evaluated in dc sweep and pulse modes. Fig. 3a shows the I-V characteristics of the flexible 1D-1R memory unit cell in the dc sweep mode with its circuit diagram. While the diode prevents resistance switching of the Al/Cu_xO/Cu layers due to its rectifying property in the reverse bias, resistance switching of the 1D-1R device is successfully observed in forward bias with a SET voltage of 2.5 V, a RESET voltage of 1.8 V, and a resistance ratio of 10^2 between the LRS and HRS at 1 V (reading voltage). Fig. 3b shows the electrical response of 1D-1R memory to the input voltage pulses: 5 ms/5 V pulse for the SET, and 5 ms/2 V pulse for the RESET, and 10 ms/1 V for the reading. This pulse mode of memory operation is more practically significant than the dc sweep mode, because actual memory devices have been driven by voltage pulses. In the beginning, the resistance state of 1D-1R memory is set to the HRS. As pulse voltage of 5 V is applied for the SET process, the resistance value of the memory is turned to a LRS of 1.23

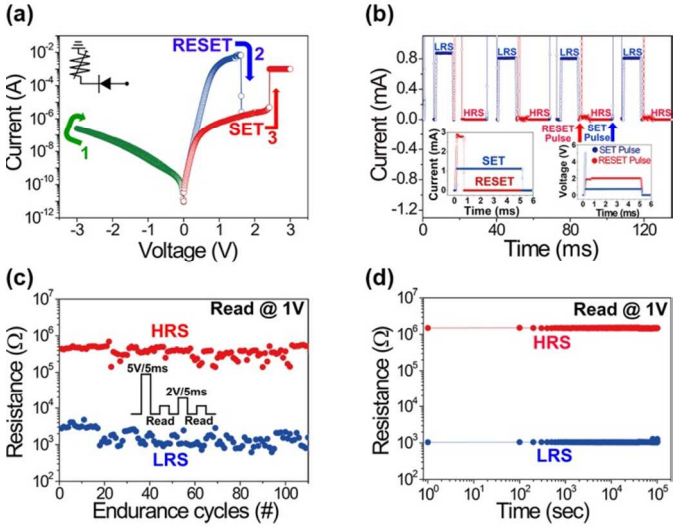


Fig. 3 (a) I-V characteristics of a 1D-1R unit cell in the dc sweep mode on a plastic substrate and the related circuit diagram. (b) Electrical responses of 1D-1R RRAM to SET/READ/RESET/READ pulses. The inset shows detailed transition response current waveforms for the SET and RESET processes. (c) Endurance test of the 1D-1R memory measured during more than 100 cycles. The inset indicates voltage pulses for SET, RESET, and READ processes. (d) Retention characteristics of the 1D-1R memory.

kΩ, and this resistance state of the device reverts to a HRS of 4.31 MΩ by applying a voltage pulse of 2 V. The resistance switching phenomenon of 1D-1R memory occurs stably and consistently in repeated pulse mode, as shown in Fig. 3b. The detailed transition response waveforms for the SET and RESET processes are presented in the left (current) and right (voltage) insets of Fig. 3b, respectively. In the case of the SET process, the electric current value abruptly increases after 15 μs has passed since the voltage of the pulse reached 5 V and the response current is maintained at 1.12 mA due to current compliance. On the other hand, 550 μs with a pulse height of 2 V is required to convert the resistance state of the unit cell to the HRS (see ESI† for electrical response of memory cell to much shorter voltage pulse, Fig. S6).

To investigate the reliability of the flexible 1D-1R RRAM, endurance and retention tests were performed. Fig. 3c shows the results of the endurance test conducted by applying repeated voltage pulses, depicted in the inset, on the memory cell of 1D-1R RRAM. During more than 100 repeated switching cycles, the two states retain their resistance values without significant variation, although there is slight fluctuation during repeated cycles. The retention characteristics of the 1D-1R device were also assessed at a read voltage of 1 V to evaluate the data storage ability in the HRS and LRS. As shown in Fig. 3d, the 1D-1R memory has a stable retention property of up to 10^5 s at room temperature. These results show that the 1D-1R devices have remarkable reliability performance on flexible substrates.

Bending tests as a function of bending radius and bending cycles were conducted to confirm the mechanical reliability of the 1D-1R memory on a plastic substrate for flexible electronic application. The 1D-1R memory shows almost the same

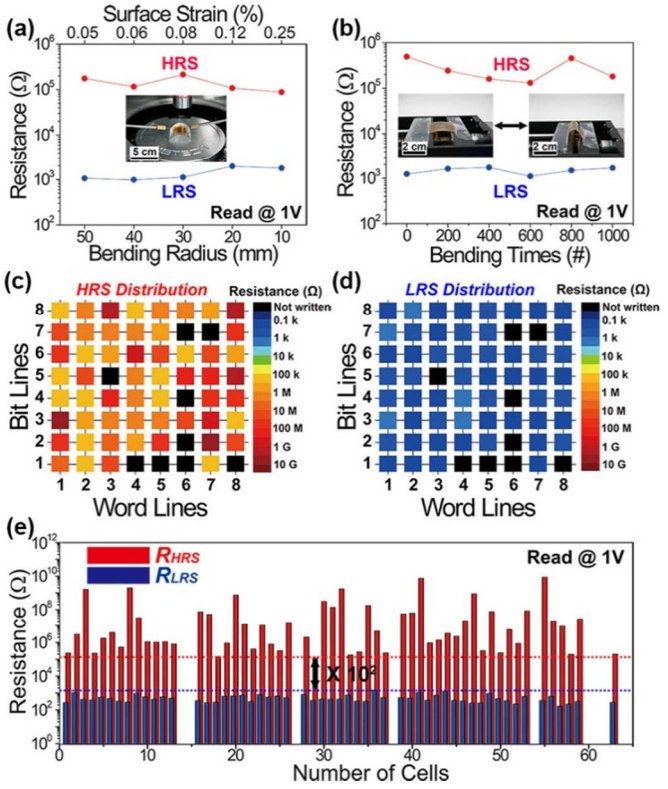
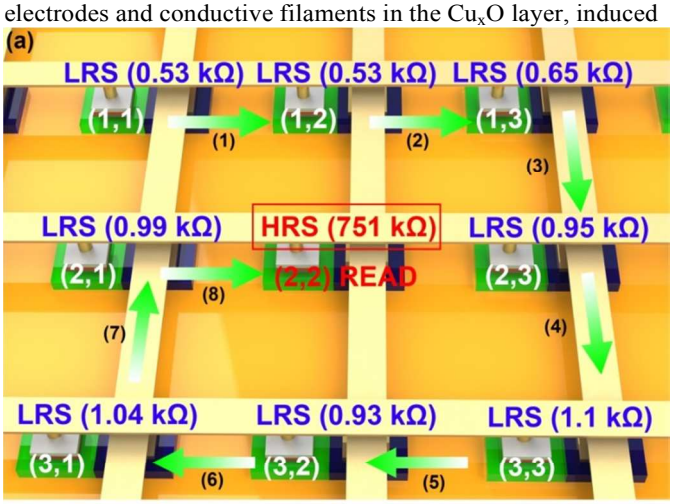


Fig. 4 (a) The resistance values of HRS and LRS as a function of bending radius. The inset is a photograph of an I-V measurement being performed under a flexed condition. (b) Bending fatigue test results of the 1D-1R memory during 1000 bending cycles for the 1D-1R memory. The inset shows photographs of the bending and unbending states. (c,d) Color map images of the resistance distribution of memory cells in the HRS (c) and LRS (d) measured from 64 memory cells in unbent condition. For the measurement of resistance distribution, the device are programmed by pulses of 5 ms/5 V (SET), 5 ms/2 V (RESET), and 5 ms/1 V (READ). The resistance values are represented in different colors, as shown in a color scale bar. (e) A histogram of the LRS and HRS resistance distribution. This result shows good separation with a resistance ratio of more than 10^2 between the LRS and HRS.

resistive switching property under different bending radii from 50 to 10 mm, which corresponds to various surface strains from 0.05 to 0.25 %, as shown in Fig. 4a. Similarly, Fig. 4b presents that 1D-1R RRAM retains its resistance ratio between HRS and LRS without significant degradation during repeated bending cycles, which demonstrates that the 1D-1R RRAM also has excellent mechanical robustness.

Color maps according to the resistance distribution of 64 memory cells in a 8 × 8 array were prepared to examine the uniformity of memory cells and are presented in Fig. 4c and 4d for the HRS and the LRS, respectively. Although some cells denoted by black color do not work due to defects generated during the transfer process,[33] the final yield of the integrated device reaches 85~90 %, and the device yield can be improved further by adopting an automated fabrication process.[41] Interestingly, the distribution of the LRS is very narrow, but the resistance value of the HRS ranged from 10^5 to 10^{10} Ω. This may arise from the variation of the gap distance between the electrodes and conductive filaments in the Cu_xO layer, induced



(b)

Operation Conditions for 1D-1R Memory Cells			
Pulse	SET	RESET	READ
Voltage	5 V	2 V	1 V
Width	5 ms	5 ms	5 ms

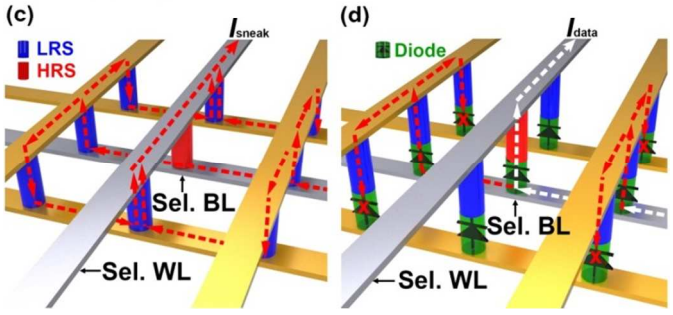


Fig. 5 (a) Schematic illustration of the random access operation of 3 × 3 flexible 1D-1R memory device. The green arrows indicate the order of the writing process. (b) Operation conditions for the 1D-1R memory cells arranged in a passive matrix array. (c) Schematic illustration of the reading operation of cross-point memory without selection devices. Possible misreading paths (sneak paths) through low resistance cells are denoted by red dotted lines. The gray lines indicate selected word and bit lines. (d) An illustration of the reading process of a 1D-1R RRAM. The integrated diodes do not permit the electrical leakage path and enable random access operation. The white dotted line denotes a correct data signal corresponding to the logical state of the (2, 2) cell.

by nonuniform rupture of the conductive filament during the RESET process.[13] However, the resistance value between the lowest value of the HRS cells and the highest value of the LRS cells demonstrates good separation with a ratio of more than 10^2, as shown in Fig. 4e (see ESI† for details of statistical analyses of 1D-1R unit cells).

We conducted random access operation of 3 × 3 flexible 1D-1R RRAM cells, as schematically illustrated in Fig. 5a, and their operation conditions are presented in Fig. 5b. The initial state of all cells is set to the HRS. By applying the SET pulse on the

word lines, the (1,1), (1,2), (1,3), (2,3), (3,3), (3,2), (3,1,), and (2,1) cells are sequentially changed from the HRS to the LRS (the writing process, see Fig. S12 in ESI†). The READ pulse is then applied to the (2,2) cell in order to read the resistance state of the (2,2) cell. The measured resistance value of the selected cell (2,2) in the 3 × 3 1D-1R array corresponds to the HRS (751 kΩ), indicating that the integrated diodes effectively suppress unintended current paths. If there is no selection device, the correct reading process is impossible due to the sneak current paths, as represented by the red dotted lines in Fig. 5c (see ESI† for the reading operation of 1R memory array without selection diodes at the worst case scenario, Fig. S10). On the contrary, an accurate reading process is possible in the 1D-1R RRAM, because the selection device does not permit current paths through neighboring low resistance states (see Fig. 5d). Finally, we conducted the SET process of the (2,2) cell by applying a SET pulse, and all memory cells were changed back to the HRS by applying the RESET pulse to demonstrate the erasing process[8] (see ESI† for details of the writing/reading/erasing process).

Conclusions

In summary, we demonstrated a flexible 1D-1R RRAM with 8 × 8 arrays composed of high-performance silicon diodes and a resistive change material. The stability and reliability of flexible RRAM were confirmed from an endurance/retention test and a statistical analysis. The developed devices also showed excellent mechanical reliability in terms of bending radii and times tests. Finally, the proposed flexible 1D-1R RRAM demonstrated random access operation including write/read/erasing on a plastic substrate due to the rectifying property of integrated diodes. This flexible 1D-1R RRAM technology shows the possibility of realizing high packing density memory on plastic substrates, and may offer an important breakthrough for realizing a flexible electronic system through integration with flexible large-scale integration (LSI). We are currently developing this technology by adopting wafer-level transfer protocol on plastic substrates to achieve high density memory and cost reduction.[42]

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Notes and references

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†Electronic Supplementary Information (ESI) available: Fabrication schematics for flexible 1D-1R device, the forming process, the switching I-V characteristics, statistical analysis of flexible RRAM, electrical pulse measurement of 1D-1R device, resistive switching properties under the bended condition, conduction mechanisms of the memory in the LRS and HRS, the random access operation for 2 × 2 1R memory cells and 3 × 3 1D-1R RRAM cells. See DOI: 10.1039/b000000x/

‡These authors contributed equally to this work.

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