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Optimal Design of High Performance H-JLTFET using HfO_2 as Gate Dielectric for Ultra Low Power Applications

Pranav Kumar Asthana[1], Bahniman Ghosh[1,2], Shiromani Bal Mukund Rahi[1] and Yogesh Goswami[1]

[1]*Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur 208016, India (email: pranava@iitk.ac.in),*

[2]*Microelectronics Research Center, 10100, Burnet Road, Bldg. 160, University of Texas at Austin, Austin, TX, 78758 (email: bghosh@utexas.edu)*

Abstract-In this paper we have proposed optimal design of Hetero - Junctionless Tunnel Field Effect Transistor using HfO_2 as a gate dielectric. The device principle and performance are investigated in 2D simulator. During this work, we investigated the transfer characteristics, output characteristics, transconductance, G_m output conductance, G_D, and C-V characteristics of our proposed device. Numerical simulations resulted in outstanding performance of H-JLFET such as I_{ON} of ~0.23mA/μm, I_{OFF} of ~2.2×10^{-17}A/μm, I_{ON}/I_{OFF} of ~10^{13}, sub-threshold slope (SS) of ~12mV/dec, DIBL of ~93mV/V and V_{th} of ≃0.11V at room temperature and V_{DD} of 0.7V. This indicates that H-JLTFET can play an important role for further development of low power switching applications.

Keywords **Band-to- Band Tunneling (BTBT), Tunnel Field Effect Transistor (TFET), Junctionless Tunnel Field Effect Transistor (JLTFET), Hetero Junctionless Tunnel Field Effect Transistor (H-JLTFET), I_{ON}/I_{OFF} ratio.**

I. Introduction

MOSFETs have severe challenges for sub 20nm technology because of steep doping profiles at source and drain junctions. Junctionless FETs provide solution to this problem as they do not have doping junctions[1-3]. Also they are suited for high speed applications but their high subthreshold swing, as in CMOS, makes them power consuming devices. TFETs received attention for low power applications because of low subthreshold swing[4-7]. However, low on current hinders it from many other high speed applications. Now, Junctionless Tunnel FETs (JLTFETs) are subject of intensive studies in device research as it has low subthreshold swing along with higher ON current giving better speed[8-9]. This device structure utilizes quantum tunneling using charge plasma concept. Additionally, it does not have any doping junctions. It has established itself as one of the most promising candidates of future logic circuits which operate for supply voltages smaller than 0.5V. Moreover, process budget reduces because of junctionless channel. Also, JLTFET shows better electrical performance and less variability than MOSFET [10] because there are no p-.n junctions.

In this paper we proposed and investigated a new structure, H-JLTFET. This structure takes advantage of dual material channel causing higher tunneling in ON state and reduced tunneling in OFF state. As a result of that, there is drastic improvement in performance. We have optimized our device structure using Silvaco TCAD Atlas 2D.

II. Device structure and parameters

Fig.1 shows the proposed device structure of Si: Ge Hetro-Junctionless Tunnel Field Effect transistors. n^+ Poly Gate and p^+ Poly Source are used to provide appropriate work function difference between gate and channel for creation of p-i-n regions. Lower band gap material germanium on the source side causes higher tunneling in ON state while drain side tunnelling weakens because of higher band gap material silicon. There are many reports indicating successful attempts to fabricate Si and Ge interface[10-11]. Parameters used in our simulations for Si:Ge H-JLTFET are: gate length=20nm, gate dielectric, HfO_2 thickness (T_{ox}) =2nm, Si:Ge film thickness (T_{si}) =5 nm, low-k spacer thickness=2nm, work function of poly n^+ region of gate =4.2eV, work function of poly p^+ region of gate=5.3eV, supply voltage=0.7V and carrier concentration in uniformly doped channel N_D =$1.0\times10^{18}/cm^3$. Si-TFET has same parameters except channel with doping junctions, with

channel region doping concentration of $10^{16}/cm^3$ and source/drain doping of $10^{18}/cm^3$. Similarly, Si-JLTEFT has same parameters, except Si channel instead of Si: Ge interface.

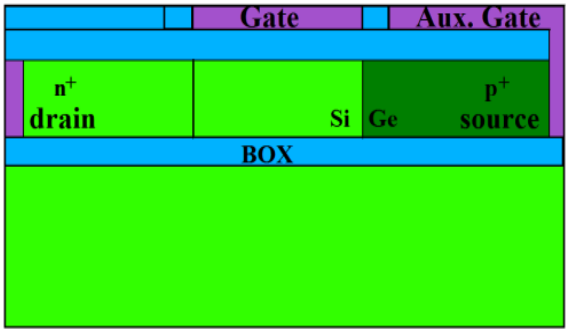


Fig. 1. Cross sectional view of device structure of Si: Ge Hetro-Junctionless Tunnel Field Effect transistor

Fig. 2 shows the valence and conduction band energy profiles along x- direction at channel and HfO_2 interface of H-JLTFET shown in Fig.1. It is observed that, in OFF state, tunneling barrier is too large which causes negligible tunneling probability of electrons. In OFF state only small leakage current flows in device. Fig. 3 shows the charge concentration profile for electron and hole along x-direction at the channel and HfO_2 interface of H-JLTFET. From Fig. 3, it is observed that on applying gate voltage on control gate (named gate in our proposed structure, as shown in Fig.1), electron concentration beneath this gate increases. This result shows that applied gate voltage causes tunneling barrier lowering between source and channel.

For a tunnel FET, it is found that ON current increases exponentially with decrease of tunneling barrier [11]. From Fig. 2 it is noticed that in ON state barrier width is sufficiently lower causing increase in the tunneling probability of electrons from valence band to conduction band, resulting in sufficient amount of current flow in the device. Further use of high-k gate dielectric material, HfO_2, improves gate control and hence ON current and subthreshold slope. All simulations are done in SILVACO ATLAS 2D V5.15.32 R [12]. Drift-diffusion current transport model, Lombardi mobility model and SRH recombination model are included for simulations [12-13]. Apart from that, Band Gap Narrowing (BGN) model is used because of highly doped channel [14]. Non local band to band tunneling model is included for studying the effect of tunneling [12]. For further accuracy, Schenk's Trap Assisted Tunneling (TAT) model and Quantum Confinement (QC) model are incorporated [12, 15]. Grid points are kept at 0.2 nm spacing in x-direction and at 0.5 nm spacing in y-direction.

III. Results and Discussions

Fig. 4 shows comparison of the I_D-V_G characteristics of our proposed device with Si-JLTFET and Si-TFET for same dimensional parameters. It can be observed that proposed device has much better device characteristics than other two. Further, I_{ON}, of 0.23mA/μm, 0.82 μA/ μm and 0.08 μA/ μm; I_{OFF}, of 2.2×10^{-17}A/μm, 1.9×10^{-14}A/μm and 1.6×10^{-15}A/μm; I_{ON}/I_{OFF}, of 10^{13}, 4.3×10^{7} and 5×10^{7} are observed for H-JLTFET, JLTFET and TFET respectively. TFET has lower OFF state current than JLTFET as JLTFET has no physical junction rather created by charge plasma concept. However, ON state current is much higher than TFET because of inheritance of Juntionless FET. TFET and Junctionless FET blended JLTFET has significantly higher I_{ON}/I_{OFF} than TFET. Si:Ge Hetero-structure tremendously improves performance in comparison to JLTFET due to increased band to band tunneling in source side in ON state. Fig. 4 clearly depicts that from subthreshold slope to ON and OFF state current, H-JLTFET has enhanced device characteristics. Transfer characteristics of proposed device are shown in Fig. 5 for different drain voltages. This figure also indicates the drain induced barrier lowering which is highly suppressed as clear from the fig. 5. XOI and Junctionless FET with highly controlled tunneling employing hetero structure and that too at very low voltage are the reasons of highly suprresed DIBL. This result shows that our device works well for long range of applied voltages from 0.0V to 0.7V. DIBL is calculated from following formula [16]

$$\text{DIBL} = \frac{V_{th_{V_{DS}=0.7V}} - V_{th_{V_{DS}=0.05V}}}{V_{DS=0.7V} - V_{DS=0.05V}} \qquad (1)$$

Where $V_{th_{V_{DS}=0.7V}}$ is threshold voltage at $V_{DS} = 0.7V$. H-JLTFET has DIBL of 73mV/V. Also, subthreshold slope of 12mV/decade is calculated for V_{DS} = 0.7V and V_{GS} = 0.7V through following formula

$$\text{Average subthreshold slope (SS)} = \frac{V_{th} - V_{ref}}{\log\frac{I_{th}}{I_{ref}}} \qquad (2)$$

ITRS made predictions for 2013 that 22nm HP will have I_{ON} of 2.2mA/μm and I_{OFF} of 0.37μA/μm while 22nm LSTP will have I_{ON} of 0.5mA/μm and I_{OFF} of 2×10^{-11}μA/μm[17-18]. Clearly, H-JLTFET surpasses both the limits of both the technologies.

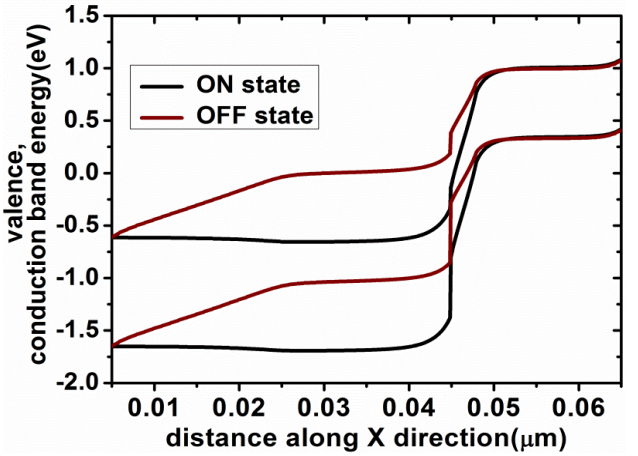
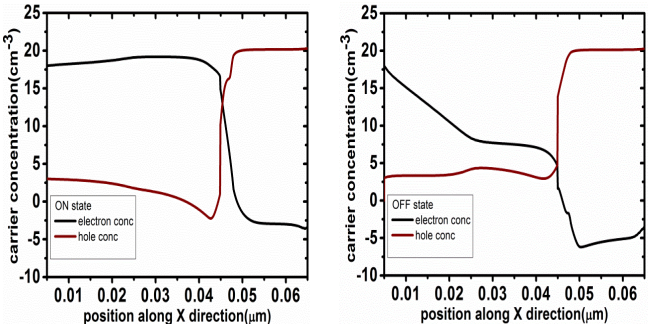


Fig. 2. Energy band diagrams taken horizontally across the channel of hetero structure bulk junction less tunnel FET, in ON state (V_{DS} = 0.7V, V_{GS} = 0.7V) and OFF state (V_{DS} = 0.7V, V_{GS} = 0V) along X direction at channel and HfO_2 interface for H-JLTFET

Output characterstics of H-JLTFET for V_{GS} ranging from 0.1V to 0.7V are shown in Fig. 6. We observed exponential increase in drain current with gate voltage, depicting better gate control. Also, saturation region is flatter, indicating negligible channel length modulation. Besides, other short channel effects reported previously, specially kink effect, are highly suppressed [19-20]. Fig.7. shows transconductance as a function of gate voltage for V_{DS} ranging from 0.05V to 0.7V. The transconductance obtained for gate voltage resembles the conventional curve at lower gate voltages. However, deviation is observered for higher values of gate voltage as



(a) (b)

Fig. 3. Electron and Hole Concentration Profile of H-JLTFET as function of position along the x-direction in (a) ON state (V_{DS} = 0.7V, V_{GS} = 0.7V) (b) OFF state (V_{DS} = 0.7V, V_{GS} = 0V) at channel and HfO_2 interface

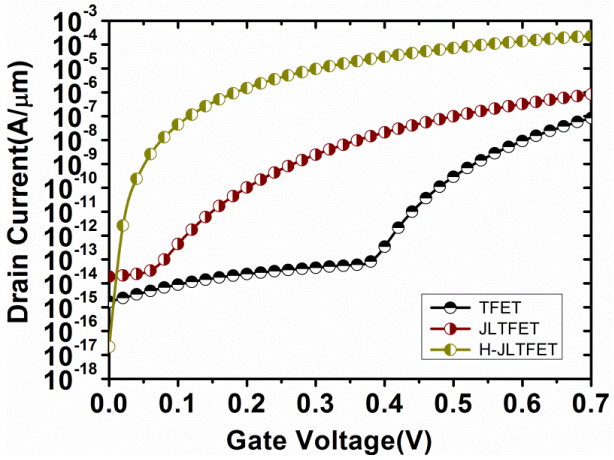


Fig. 4. Comparison of transfer characteristics of Si-TFET, Si-JLTFET and Si: Ge H-JLTFET with same dimensional parameters

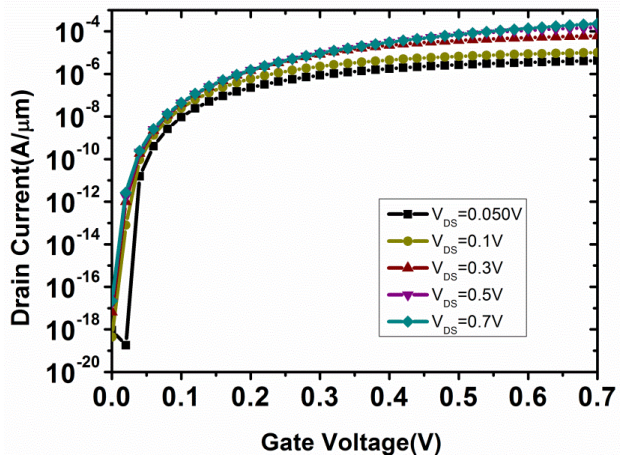


Fig. 5. Drain current versus Gate voltage for H-JLTFET at V_{DS} from 0.05V to 0.7V

tunneling is a nonlinear phenomena and it depends on orientations of band structure. Similarly, output conductance, $G_D = \frac{\partial I_D}{\partial V_{DS}}$ characteristics are complied in Fig. 7 for V_{GS} ranging from 0.1 to 0.7V . There is a hump observed in G_D around $V_{GS}/2$ due to Drain Induced Tunneling (DIT). At high V_{GS} and low V_{DS}, little increase in V_{DS} causes more tunneling. Hence drain duplicates behaviour of gate at low V_{DS} but for $V_{DS}>V_{GS}/2$ DIT fades as rate of increase of tunneling decreases and hence transconductance follows conventional behaviour afterward.

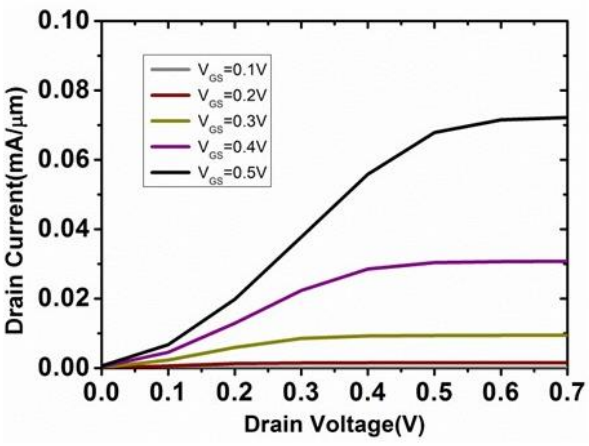


Fig. 6. Output characterstics at V_{GS} from 0.1 to 0.7V for H-JLTFET

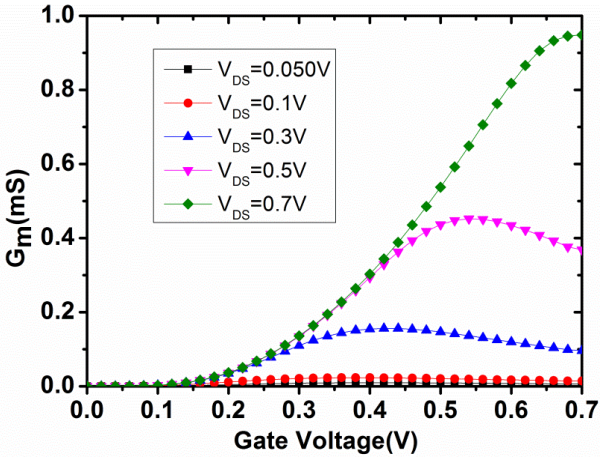


Fig. 7. Transconductance, G_m versus Gate voltage for H-JLTFET at V_{DS} from 0.05V to 0.7V

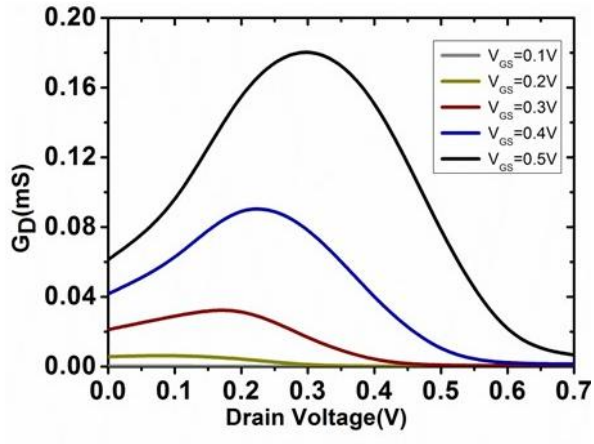
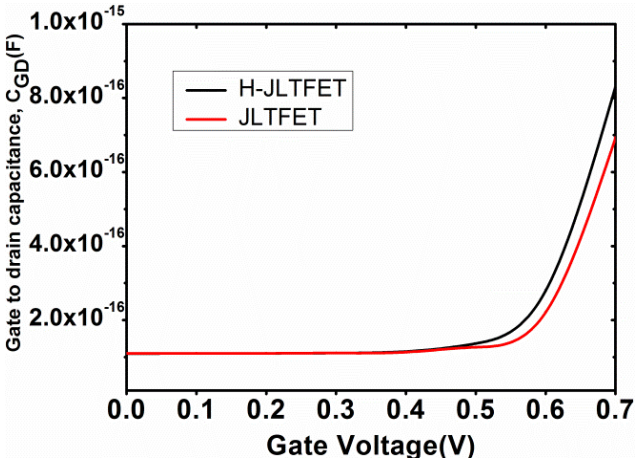
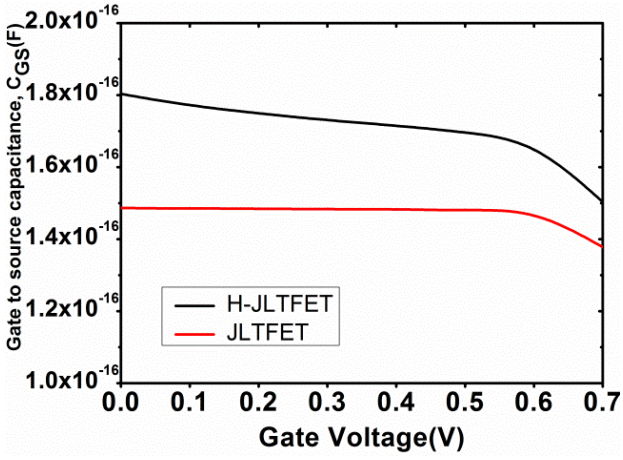


Fig.8. Drain conductance, G_D vs. V_{DS} at V_{GS} from 0.1 to 0.7V for H-JLTFET

Figs. 9(a) and (b) show comparison of gate-to-drain and gate-to-source capacitance respectively for H-JLTFET and JLTFET as a function of gate voltage at drain voltage of 0.7V, frequency of 1MHz and small signal voltage of 0.01V. JLTFET provides little lower gate-to-drain/source capacitance than H-JLTFET at higher gate voltages.



(a)



(b)

Fig. 9: Variation of (a)gate to drain capacitance, C_{GD} and (b) gate to source capacitance, C_{GS}, with gate voltage at V_{DS}=0.7V, frequency=10^6Hz and v_{ss}=0.01V for H-JLTFET

Conclusions

In this work, we proposed optimal design of Hetero-Junctionless Tunnel Field Effect Transistor (H-JLTFET) using HfO_2 as a gate dielectric and discussed its static operation. Through simulation, we also studied the characteristics of H-JLTFET, especially for switching applications. The device provides high speed operation even at very low supply voltage with low leakage and reduced number of steps in fabrication process which indicates that H-JLTFET is a promising candidate for switching performance. In addition, it has potential for further scalability.

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