ROYAL SOCIETY OF CHEMISTRY

www.rsc.org/nanoscale

Nanoscale

ARTICLE

Exploration of yttria film as gate dielectric in sub-50nm carbon nanotube field-effect transistors

Li Ding,[a] Zhiyong Zhang,[a, *] Jun Su,[b] Qunqing Li[c] and Lian-Mao Peng[a, *]

Thin yttria film is statistically investigated for use as gate dielectric in carbon nanotube (CNT) field-effect transistors (FETs) with gate length scaled down to sub 50 nm. The yttria film is shown to provide omega-shape-gate dielectric with low interface trap density, which leads to excellent gate control ability and thus a low average subthreshold swing (SS) of 74 mV/decade for both long and short CNTFETs and small drain-induced-barrier-lowering. It is also demonstrated that the performance of CNTFETs increases with decreasing temperature, showing an excellent SS of 22 mV/decade at liquid-nitrogen temperature. Furthermore a method is developed to retrieve interface trap density in CNTFETs, and a low interface trap density of $5.2 \times 10^6 \ cm^{-1}$ is achieved, indicating high electric quality of the yttria film.

Introduction

Field-effect-transistor (FET), a device that uses an electric field to control the conductivity of a semiconductor channel, is the most important and widely used electric device for modern integrated circuits (ICs). A high-performance FET must be provided with excellent semiconducting channel materials, ideal ohmic source/drain contacts, and high-quality gate dielectric, and none of the above is dispensable. As the mainstream FET device, silicon-based metal-oxide-semiconductor (MOS) FET has been developed for more than 50 years according to the famous "Moore's Law", and will encounter its limit both scientifically and technologically in the near future.[1, 2] Carbon nanotube (CNT) is considered as one of the most promising candidate material for replacing silicon as channel material for constructing next generation high-performance FET, mainly owing to its unique structural, mechanical, chemical, and in particular electric properties, including ultra-thin body, high carrier mobility and high saturation velocity.[3-6] Since the first FET was built on CNT in 1998,[7] CNT-based FETs have been developed for over fifteen years, and great advances have been made on developing high performance CNTFETs, circuits and systems.[4-11] In particular, ideal ohmic contacts have been realized in CNTFETs through adopting Sc[12] and Y[13] for n-type and Pd[4] for p-type contacts, leading to a contact resistance that approaches quantum limit. Moreover high-k dielectrics such as HfO_2, ZrO_2, and Al_2O_3 have been explored for using as gate dielectrics to enhance gate efficiency of CNTFETs, and high trans-conductance and low sub-threshold swing (SS) have been achieved in both n- and p-type FETs for relatively long gate length (larger than 100 nm) devices.[14-20] However, these conventional high-k dielectrics are not suitable for CNT to provide the highest gate efficiency. Experimentally almost all top-gated CNTFETs with short gate length (smaller than 50 nm) show degraded SS of larger than 80 mV/decade.[21-23] Sub-threshold swing is important because it is

the key parameter for describing the turn-off speed of a FET. In general the smaller the SS is, the smaller the off-state current at a fixed supply voltage and thus reduced power dissipation. Recently CNT-based FETs have been scaled down to sub-10 nm and shown to exhibit much better on-state current than silicon MOS FETs, while suffered little degradation of SS. However, these sub-10nm CNTFETs were fabricated using a back-gate device geometry,[24-25] and by doing so the difficult job of growing ultra-thin high-k top-gate dielectric was avoided.

To fabricate high performance top-gate CNTFETs which are more suitable for constructing large scale ICs, ultra-thin dielectric layer should be fabricated on CNT to ensure efficient gate control on the channel. However dielectric layer of thinner than 8 nm cannot be readily grown on CNT via conventional methods, e.g. atomic layer deposition (ALD).[26] This is because usual high–k dielectric layer cannot nucleate on perfect CNT without defects, and thick dielectric layer is usually grown from SiO_2 substrate to bury CNTs. On the other hand it is highly desirable to have an ultra-thin high-quality gate dielectric to provide the needed efficient control on small CNTFETs with gate length less than 50 nm. Lanthanum oxide was recently demonstrated as a good gate dielectric for CNTFETs owing to its high-k and low interface trap density.[27] But the method was demonstrated only for back-gate CNTFETs and the material is integrated with CNT devices using molecular beam epitaxy/chemical beam epitaxy (MBE/CBE). In an earlier paper we demonstrated that yttria (Y_2O_3) film is a perfect top-gate dielectric for carbon based electronics mainly owing to its good wetting with sp^2 carbon skeleton.[28] CNTFETs with Y_2O_3 gate dielectric exhibited perfect switching off characteristic, and in particular SS was pushed down to its room temperature limit of 60 mV/decade for a long channel device. Although it was predicted that Y_2O_3 film will remain competent as gate dielectric for sub-10 nm carbon FETs,[29] experimentally sub-50 nm top-gated CNTFETs with SS below 80 mV/decade at room temperature has never been demonstrated. This paper aims to

present a statistical and systematical study on Y_2O_3 film as top-gate dielectric layer in CNTFETs with gate length scalded down to sub 50 nm regime.

Results and discussion

The device structure we used in this work and electric characteristics for some typical long and short channel CNTFETs are shown in Fig. 1. All these devices used a 6 nm Y_2O_3 film as gate dielectric, and a typical scanning electron microscopy (SEM) image showing a short channel device is presented in Fig. 1(b), where the channel length is about 122 nm and gate length is 48 nm. The measured electric characteristics of this short channel FET are shown in Fig. 1(c) and 1(d) respectively, exhibiting high-performance n-type field-effect property owing to adopting Sc as the contact to CNTs.[11-12] As a comparison, long gate length (about 1.5 μm) CNTFETs were fabricated and measured, and typical device characteristics are shown in Fig. S1 in the Electronic Supplementary Information (ESI). The short gate FET (Fig. 1(b)) shows excellent SS, about 65 mV/decade, approaching the theoretical limit of 60mV/decade at room temperature. In addition, almost no drain-induced-barrier-lowering (DIBL) is observed for the same device, indicating that source and drain electric field have little effect on gate electrical field to the channel. Combination of small SS and negligible DIBL indicates that short channel effect can be avoided for small CNTFETs with gate length scaled down to 50 nm, since the gate electrode on the Y_2O_3 film can provide enough controlling ability on the CNT channel.

While the switching off properties of a FET are important and can be characterized by SS and DIBL, its turning on characteristics are equally important since they reflect the speed and driving ability of the transistor. Long gate CNTFETs typically have large saturation current of more than 6 μA and peak trans-conductance (g_m) of 14 μS at bias of 1 V [see Fig. S1(b) in the ESI], while for short gate FETs the saturation current increases further up to more than 12 μA and g_m increases up to 17 μS at V_{ds} = 0.5 V (Fig. 1(d)). The increase in saturation current and trans-conductance is direct consequences of scaling down the transistor. Furthermore, the on-state performance of the CNTFET can be further improved if a self-aligned gate structure is used to fabricate the short gate FETs.

We now consider further electric characterization of Y_2O_3 gate dielectric in CNTFETs, including leakage current and hysteresis. Typically less than 10 pA leakage current and as small as 80 mV hysteresis was found for those CNTFETs as shown in the ESI as Fig. S2 and S3. It is thus concluded that through adopting Y_2O_3 film as gate dielectric in CNTFET, we can take the full advantage of device dimension scaling while suffering little short channel effects, such as SS degradation and increased DIBL.

An ideal gate dielectric shall enable a consistent yield of low SS in devices,[27] which in turn reflects the quality and uniformity of the dielectric layer and the interface between dielectric layer and CNT. To test this consistency, we fabricated and measured numerous CNTFETs including 10 devices with short gate length and 19 devices with long gate length, and transfer characteristics of these short and long gate length CNTFETs are respectively plotted in Fig. 1(e) and 1(f). Although the 19 long gate devices were fabricated using different CNTs on different regions of the silicon wafer, the results show little variation on SS (from 62 to 82 mV/decade).

The average SS value is as low as 74 mV/decade, which is nearly equal to that of the best back-gated CNTFETs with lanthanum oxide as gate dielectric.[27] The threshold voltage (V_t) variation is around 0.38 V owing to the fluctuations of CNT diameter and environment for different CNTFETs on the Si wafer. For the 10 short channel devices with gate length of about 50 nm, the SS varies from 64 to 88 mV/decade, and the average SS value is also 74 mV/decade. Statistical analysis reveals no SS degradation as the gate length is shrunk from 1.5 μm to 50 nm, i.e. these devices are hardly affected by the short channel effects down to sub-50nm regime. Compared with long channel result, V_t variation is around 0.5 V for the short gate length devices, which is a little larger (about 120 mV) than that of long gate length devices.

By definition, low SS means low off-state current for a given bias. Off-state current is an important parameter for a FET in low power circuits design because it determines static power dissipation of integrated circuits.[30] Ideally a FET should have low off state current and thus low static power dissipation, and high on state current for high speed and driving ability. To evaluate our CNTFETs, two typical CNTFETs (with long and short gate length respectively) were examined at V_{ds} = 0.5 V. Transfer characteristics of the two devices are shown in Fig. 2(a), in which the long gate device with L_g = 1.5 μm shows a SS of 65 mV/decade while the short gate device with L_g = 56 nm shows a SS of 75 mV/decade. From these transfer characteristics, on- and off-state currents may be extracted using the standard method[31] as shown in Fig. 2(b). A blue box with a width V_{ds} (= 0.5 V) is first defined around the threshold voltage of the device V_{th}, extending 1/3 V_{ds} to lower and 2/3 V_{ds} to higher voltage. This box intercepts the transfer characteristics (which are aligned to V_{th}), and the left and right intercepts are respectively I_{off} and I_{on}. The I_{on}/I_{off} ratio is respectively 1.8 μA/4.7 nA (383) for the long device and 7.6 μA/14 nA (543) for the short device. This increased current on/off ratio is a direct consequence of more rapidly increased on-state current than off-state current for this short CNTFET, given the condition that SS of the device is not significantly degraded. To obtain a statistic picture, on- and off-state currents values for 10 short gate devices are presented in Fig. 2(c), and those for 16 long gate devices are presented in Fig. 2(d). For long gate devices, I_{on} vary from 0.4 μA to 3.5 μA, and I_{off} vary from 0.6 nA to 55 nA. For short gate devices, I_{on} vary from 2.9 μA to 8.0 μA, and I_{off} vary from 14 nA to 314 nA. Although I_{off} increases in short gate devices comparing to long gate device, the current on/off ratio remains at about several hundred which is similar to that of long gate devices (see Fig. S4 in the ESI). Benefitting from scaling of FET, the distribution of I_{on} values of short devices is obviously narrower than that of long gate devices since the sub 50 nm devices are beginning to be dominated by ballistic transport and be immune to effects from channel scatterings.

To compare the performance of the CNTFETs with Y_2O_3 as gate dielectric to Si MOS FETs and CNTFETs fabricated using other gate dielectrics with comparable gate lengths, we use two key popular metrics, i.e. SS and intrinsic gate delay, to benchmark the switching-off and turning-on properties of our short gate CNTFETs. Shown in Fig. 3 are SS of various kinds of short channel FETs with L_g < 120 nm. For gate length of about 100 nm, the CNTFETs with Y_2O_3 as gate dielectric show similar SS to the planar silicon FETs. As gate length scales down to 50 nm, SS of planar Si FETs is degraded to beyond 80 mV/decade owing to the short channel effects, while SS of our CNTFETs does not increase significantly. Excitingly SS of our

CNTFETs is as good as (or even better than) that of the conventional semiconductor based FETs with well-designed gates such as Fin-gate, Tri-gate and gate-all-around, and we attribute this excellent performance to the combination of the ultra-thin body of CNTs and high gate efficiency of the high-quality Y_2O_3 gate dielectric used in this work. Compared with other published sub-50 nm CNTFETS,[21-23] our devices obviously exhibit lower SS owing to higher gate control ability of Y_2O_3 dielectric layer and lower trap density at the Y_2O_3/CNT interface. It is obvious from Fig. 3(a) that almost all FETs suffer the degradation of SS as scaling the gate length down to sub 100 nm, while our CNTFETs with Y_2O_3 as gate dielectric show no visible tendency of SS degradation down to 45 nm.

The intrinsic gate delay of our CNTFETs is calculated using the method, which is also used in Ref. [13, 15, 16, 32], proposed in Ref. 31, and results are plotted in Fig. 3(b) together with that of previously reported n-type FETs.[16, 32] The gate delay values of our CNTFETs are systematically smaller than that of Si n-FETs with the same gate length. Obviously the use of Y_2O_3 allows the gate delay of n-type CNTFETs to be scaled down with gate length according to the scaling track of our previous work,[16, 32] and the best gate delay of n-type CNTFET is further pushed down to 0.41 ps in one device with gate length of about 45 nm. The excellent gate delay of our n-type CNTFET is originated from the use of excellent n-type ohmic contact, high-quality Y_2O_3 gate dielectric, the nature of quasi-ballistic transport in short channel CNTFETs and the very high Fermi velocity of CNT.[3]

The transmission electron microscopy (TEM) image shown in Fig. 3(c) reveals a cross section of the gate stack used in our devices. The CNT is seen to have been fully covered by a thin yttria film, which forms an excellent Ω gate stack around the CNT. Above yttria, metal Pt was deposited to protect the device from being damaged during focused ion beam (FIB) cutting of the device in preparing electron beam transparent sample for TEM examinations. Two important observations may be made from the TEM image which may have remarkable influences on device performance. First, the yttria layer wets very well with the CNT, which results from the excellent wetting behavior of metal Y and CNT. As a direct result, the yttria layer uniformly wraps around the CNT to form a perfect Ω gate, which may yield excellent electrostatic gate control on CNT channel and high gate efficiency.[33] Second, the yttria layer has clearly a continuous polycrystalline structure where no large defects such as pin-holes are observed. The high crystallinity indicates that the structure quality of the yttria film is high, and this is further confirmed by the XPS results shown in Fig. 3(d). The Y:O element ratios at various depths in the yttria film are extracted from XPS results (for details, see Fig. S5 in the ESI). For an ideal yttria film the Y:O ratio is 0.667, which is seen to be almost the case for most of the 6nm thick film, except at the interface with SiO_2 substrate where little intermixing may have occurred leading to a slightly higher O ratio to Y at the interface.

An excellent gate dielectric for a FET shall not only lead to large gate capacitance, small leakage current, but also low interface trap density. The interface traps may result in hysteresis in transfer characteristic of the FET, and induce SS degradation. Therefore interface trap density is an important parameter for charactering the gate dielectric, and should be retrieved from experimental results reliably. For a FET, SS is given by

$$SS = \frac{dV_g}{d(logI_{ds})} = m \cdot ln(10) \cdot \frac{kT}{q}, \qquad (1)$$

where k is the Boltzmann constant, T is the temperature, q is the charge of an electron, and m is usually referred to as an ideality factor.[2, 34] According to Eq. (1), SS of a device is proportional to temperature T, meaning that CNTFETs shall exhibit better switching-off behavior at low temperature. Measurements are thus conducted at various temperatures on a typical short gate CNTFET with $L_g = 50$ nm and results are presented in Fig. 4. Shown in Fig. 4(a) are transfer characteristics of the device measured at room temperature (300K) and liquid nitrogen temperature (77K) at $V_{ds} = 0.1$ V. It is obvious that the transistor exhibits much better performance at lower temperature, i.e. larger on-state current and lower off-state current. In particular SS is reduced from 80 mV/decade at 300K to 24 mV/decade at 77K. The increased on-state current at lower temperature is mainly owing to the frozen of phonon scatterings, while the perfect linear I_{ds}-V_{ds} relation at low bias in Fig. 4(b) demonstrates that the perfect ohmic contact to the CNT used in the device can at least retain to temperature as low as T = 77 K.

As depicted in Fig. 4(c), for a CNTFET, interface traps are usually located at the interface between CNT and gate dielectric layer. Interface trap states usually lay within CNT band gap and may exchange charges with CNT quickly.[2, 34] In addition to interface trap charges, fixed oxide charges, ionic mobile charges and oxide trap charges may also exist and locate near the interface or inside the oxide layer. In principle all kinds of charges near the CNT channel could affect device performance, e.g. on SS, but those interface trap charges near the interface dominate since the electrostatic interaction decays rapidly with distance. To a good approximation, the factor m in Eq. (1) may be expressed as,[15, 17-20, 27]

$$m = 1 + \frac{C_{it}}{C_{ox}}, \qquad (2)$$

where C_{ox} represents oxide capacitance and C_{it} represents that due to interface traps. In a CNTFET, oxide dielectric capacitance C_{ox} can be calculated to be 2.16 pF/μm using the relation

$$C_{ox} = 2\pi\epsilon_r\epsilon_0/ln(2t_{ox}/r), \qquad (3)$$

where ϵ_r is relative dielectric constant of Y_2O_3 (about 10),[29] t_{ox} is thickness of Y_2O_3 layer (about 6 nm), and the radius of the CNT r is about 1 nm. C_{it} may be readily extracted from SS values of the device measured at different temperatures once the oxide capacitance C_{ox} is known accurately. Indeed, several groups had obtained interface trap density by using this direct method.[17, 20, 27] This direct method assumes, however, that SS value is 0 mV/decade at 0 K, which is not true for real devices. This is because measurement errors and precision limit induced by instruments and wiring may result in deviation of actual SS from its ideal value. We note that this systematic deviation is not dependent on the sample temperature since all measurement instruments are kept at room temperature. In order to account for this systematic error, here we propose an improved method to obtain interface trap density through fitting the temperature dependent SS values.

A representative CNTFET was measured at 77 K, 170 K and 290 K respectively, and the temperature dependent SS of the CNTFET is plotted in Fig. 4(d), showing a good linear dependence on temperature. The fitted slope of SS-T data set is 0.27 ± 0.031, which is in turn used to retrieve the ideality factor of Eq. (1) to yield m = 1.39 and $C_{it} = 0.39C_{ox}$= 0.84 pF/μm. The capacitance associated with interface trap states is defined as interface trap charges divided by surface potential, i.e. $C_{it} = Q_{it}/\varphi_s$, where the surface potential φ_s is the potential applied by gate voltage at the interface between CNT and Y_2O_3.

Interface trap charges Q_{it} is defined as $Q_{it} = qN_{it}$, with N_{it} being the interface trap density. We may thus obtain interface trap density from interface trap capacitance to obtain $N_{it} = 5.2 \times 10^6$ cm^{-1} at $\varphi_s = 1V$. This and relevant quantities are summarized in Table 1, and compared with three other group's results. It is worth mentioning that the interface trap density found in our transistors is much smaller than that of reported CNTFETs with other gate dielectrics made of thermal oxidation process[17, 20] and even MBE/CBE process.[27] The low interface trap density indicates that our Y_2O_3 film as dielectric layer is of very high quality, and the combination of low interface trap density and large C_{ox} ensures excellent SS for CNTFETs integrated with Y_2O_3 gate dielectric.

Experimental

The CNTs used in this work were directionally grown on a silicon substrate, and semiconducting single-walled CNTs were identified via field-effect measurements using the substrate as the back gate. Three steps process is employed for fabricating CNTFETs using Y_2O_3 as top-gate dielectric. Large test pads were first developed via electron beam lithography (EBL) process, and a bi-layer metal Ti(5nm)/Au(35nm) were deposited on silicon wafer via electron beam evaporation (EBE). A subsequent standard lift-off was carried out to form test pad. A 3 nm thick layer of Y which is 99.9% purity and purchased from Grirem Advanced Materials Co.,Ltd. was then deposited at 1 A/s rate through electron beam evaporator with vacuum higher than 5e-8 Torr. After thermal oxidization on hot plate at 240 ℃ in air, Y_2O_3 film of 6nm was formed. The last step involves fabricating gate and source/drain electrodes through EBL and EBE. Usually gate electrode was metal layers of 5 nm / 70 nm thick Ti / Au (or Pd) while source / drain contact metal was 70 nm Sc for n-type FET. It should be noted that the Sc film was evaporated under an ultrahigh base vacuum of up to 5×10^{-8} Torr to form high-performance n-type ohmic contacts to the CNT.[12] All electric measurements were carried out by probe station. The temperature properties of devices were tested on probe station in air, while low temperature measurement were carried on low temperature probe station (Lakeshore TTP-4) in vacuum varying from room temperature to liquid nitrogen temperature. A Keithley 4200 semiconductor analyzer and an Agilent 4156 semiconductor analyzer were used in DC transport measurements.

Conclusions

We fabricate tog-gated sub-50 nm CNTFETs using completely oxidized high-quality Y_2O_3 as gate dielectric which forms continuous polycrystalline structure without any large defects. Provided with omega-shape-gate geometry and low interface trap density, Y_2O_3 film showed excellent gate control ability for CNTFETs. In particular for both long-gate and short-gate CNTFETs with sub-50nm gate length, a low average SS of 74 mV/decade is achieved, and small DIBL is observed. The performance of the CNTFETs is shown to increase with decreasing temperature, and excellent SS down to 22 mV/decade is obtained at liquid-nitrogen temperature. Furthermore a method based on variable temperature measurement data is developed to retrieve interface trap density in CNTFETs with yttria as the gate dielectric, and relatively low interface trap density (about 5.2×10^6 cm^{-1} at 1 V surface potential) is achieved.

Notes and references

[a] Key Laboratory for the Physics and Chemistry of Nanodevices, Department of Electronics, Peking University, Beijing and 100871, (P. R. China).
[b] Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, Wuhan and 430074, (P. R. China).
[c] Department of Physics and Tsinghua-Foxconn Nanotechnology Research Center, Tsinghua University, Beijing and 100084, (P. R. China).
[*] To whom correspondence should be addressed.
E-mail: (Z.Y.Z.) zyzhang@pku.edu.cn; (L.M.P.) lmpeng@pku.edu.cn.

1   Semiconductor Industry Association, International Technology Roadmap for Semiconductors (2011); available at http://public.itrs.net.
2   P. Avouris, Z. Chen and V. Perebeinos, *Nature Nanotechnology*, 2007, 2, 605-615.
3   R. Saito, G. Dresselhaus and M. S. Dresselhaus, *Physical Properties of Carbon Nanotube*, Imperial College Pr, 1998.
4   A. Javey, J. Guo, Q. Wang, M. Lundstrom and H. J. Dai, *Nature*, 2003, 424, 654-657.
5   A. Javey, Q. Wang, W. Kim and H. Dai, *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International*, 2003, DOI: 10.1109/IEDM.2003.1269387, 31-31.32.34.
6   J. Appenzeller, *Proceedings of the Ieee*, 2008, 96, 201-211.
7   S. J. Tans, A. Verschueren and C. Dekker, *Nature*, 1998, 393, 49-52.
8   M. M. Shulaker, G. Hills, N. Patil, H. Wei, H.-Y. Chen, H. S. PhilipWong and S. Mitra, *Nature*, 2013, 501, 526-530.
9   L. Ding, Z. Zhang, S. Liang, T. Pei, S. Wang, Y. Li, W. Zhou, J. Liu and L.-M. Peng, *Nature Communications*, 2012, 3.
10   L. Ding, S. Liang, T. Pei, Z. Zhang, S. Wang, W. Zhou, J. Liu and L.-M. Peng, *Applied Physics Letters*, 2012, 100, 263116-263116.
11   Z. Zhang, S. Wang, Z. Wang, L. Ding, T. Pei, Z. Hu, X. Liang, Q. Chen, Y. Li and L.-M. Peng, *ACS Nano*, 2009, 3, 3781-3787.
12   Z. Zhang, X. Liang, S. Wang, K. Yao, Y. Hu, Y. Zhu, Q. Chen, W. Zhou, Y. Li, Y. Yao, J. Zhang and L.-M. Peng, *Nano Letters*, 2007, 7, 3603-3607.
13   L. Ding, S. Wang, Z. Zhang, Q. Zeng, Z. Wang, T. Pei, L. Yang, X. Liang, J. Shen, Q. Chen, R. Cui, Y. Li and L.-M. Peng, *Nano Letters*, 2009, 9, 4209-4214.
14   G. D. Wilk, R. M. Wallace and J. M. Anthony, *Journal of Applied Physics*, 2001, 89, 5243-5275.
15   A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuen, M. Lundstrom and H. J. Dai, *Nature Materials*, 2002, 1, 241-246.

ARTICLE

16 Z. Zhang, S. Wang, L. Ding, X. Liang, T. Pei, J. Shen, H. Xu, Q. Chen, R. Cui, Y. Li and L.-M. Peng, *Nano Letters*, 2008, 8, 3696-3701.

17 R. Martel, H. S. P. Wong, K. Chan and P. Avouris, *Electron Devices Meeting, 2001. IEDM '01. Technical Digest. International*, 2001, DOI: 10.1109/IEDM.2001.979456, 7-7.5.4.

18 Q. Cao, M.-G. Xia, M. Shim and J. A. Rogers, *Advanced Functional Materials*, 2006, 16, 2355-2362.

19 R. T. Weitz, U. Zschieschang, F. Effenberger, H. Klauk, M. Burghard and K. Kern, *Nano Letters*, 2007, 7, 22-27.

20 S. Kumar, N. Pimparkar, J. Y. Murthy and M. A. Alam, *Applied Physics Letters*, 2006, 88, 123505.

21 A. D. Franklin, S. O. Koswatta, D. B. Farmer, J. T. Smith, L. Gignac, C. M. Breslin, S.-J. Han, G. S. Tulevski, H. Miyazoe, W. Haensch and J. Tersoff, *Nano Letters*, 2013, 13, 2490-2495.

22 A. Javey, J. Guo, D. B. Farmer, Q. Wang, E. Yenilmez, R. G. Gordon, M. Lundstrom and H. J. Dai, *Nano Letters*, 2004, 4, 1319-1322.

23 S.-J. Choi, P. Bennett, K. Takei, C. Wang, C. C. Lo, A. Javey and J. Bokor, *ACS Nano*, 2013, 7, 798-803.

24 A. D. Franklin and Z. Chen, *Nature Nanotechnology*, 2010, 5, 858-862.

25 A. D. Franklin, M. Luisier, S.-J. Han, G. Tulevski, C. M. Breslin, L. Gignac, M. S. Lundstrom and W. Haensch, *Nano Letters*, 2012, 12, 758-762.

26 Y. R. Lu, S. Bangsaruntip, X. R. Wang, L. Zhang, Y. Nishi and H. J. Dai, *Journal of the American Chemical Society*, 2006, 128, 3518-3519.

27 A. D. Franklin, N. A. Bojarczuk and M. Copel, *Applied Physics Letters*, 2013, 102, 013108.

28 Z. Wang, H. Xu, Z. Zhang, S. Wang, L. Ding, Q. Zeng, L. Yang, T. Pei, X. Liang, M. Gao and L.-M. Peng, *Nano Letters*, 2010, 10, 2024-2030.

29 H. Xu, Z. Zhang, Z. Wang, S. Wang, X. Hang and L.-M. Peng, *ACS Nano*, 2011, 5, 2340-2347.

30 J. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits: A Design Perspective; 2nd ed.*, Pearson Education, Upper Saddle River, NJ, 2003.

31 R. Chau, S. Datta, M. Doczy, B. Doyle, J. Jin, J. Kavalieros, A. Majumdar, M. Metz and M. Radosavljevic, *Ieee Transactions on Nanotechnology*, 2005, 4, 153-158.

32 Z. Y. Zhang, S. Wang, L. Ding, X. L. Liang, H. L. Xu, J. Shen, Q. Chen, R. L. Cui, Y. Li and L. M. Peng, *Applied Physics Letters*, 2008, 92, 133117.

33 Y. Li, H.-M. Chou and J.-W. Lee, *Nanotechnology, IEEE Transactions on*, 2005, 4, 510-516.

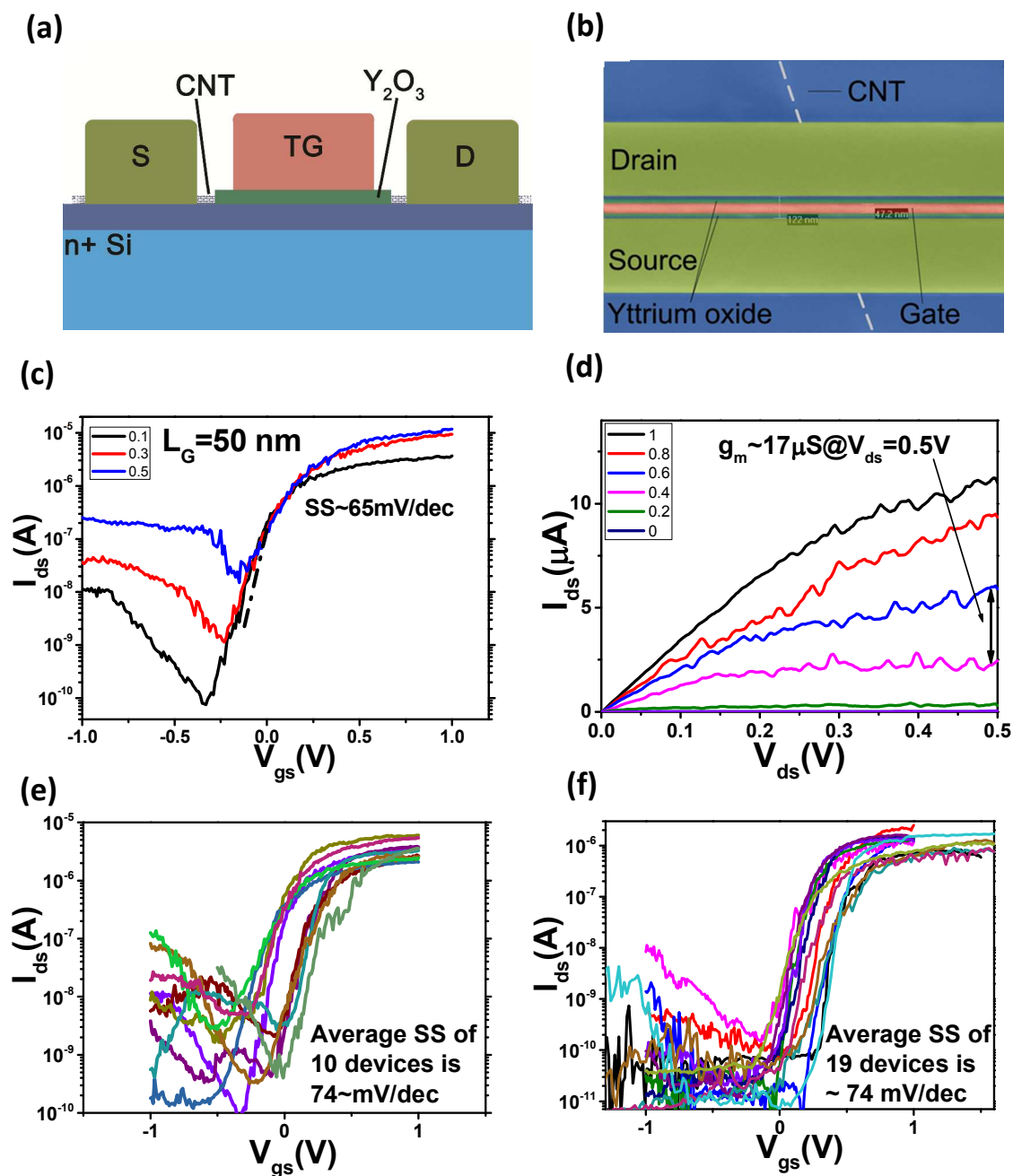34 S. M. Sze and K. N. Kwok, *Physics of Semiconductor Devices; 3rd ed.*, Wiley, Hoboken, NJ, 2007.

(a)

(b)

(c)

(d)

(e)

(f)

Figure 1. Electric characteristics of some typical CNT FETs with Y_2O_3 film as gate dielectric. (a) Device structure and (b) SEM image showing a real device with a gate length $\sim$ 50 nm. (c) Transfer characteristics of the device shown in (b) and its (d) output characteristics. (e) Transfer characteristics of 10 short channel devices with $L_g \sim 50\ nm$ and $V_{ds} = 0.1$ V. (f) Transfer characteristics of 19 long channel devices with $L_g \sim 1.5\ \mu$m and $V_{ds} = 0.1$ V.
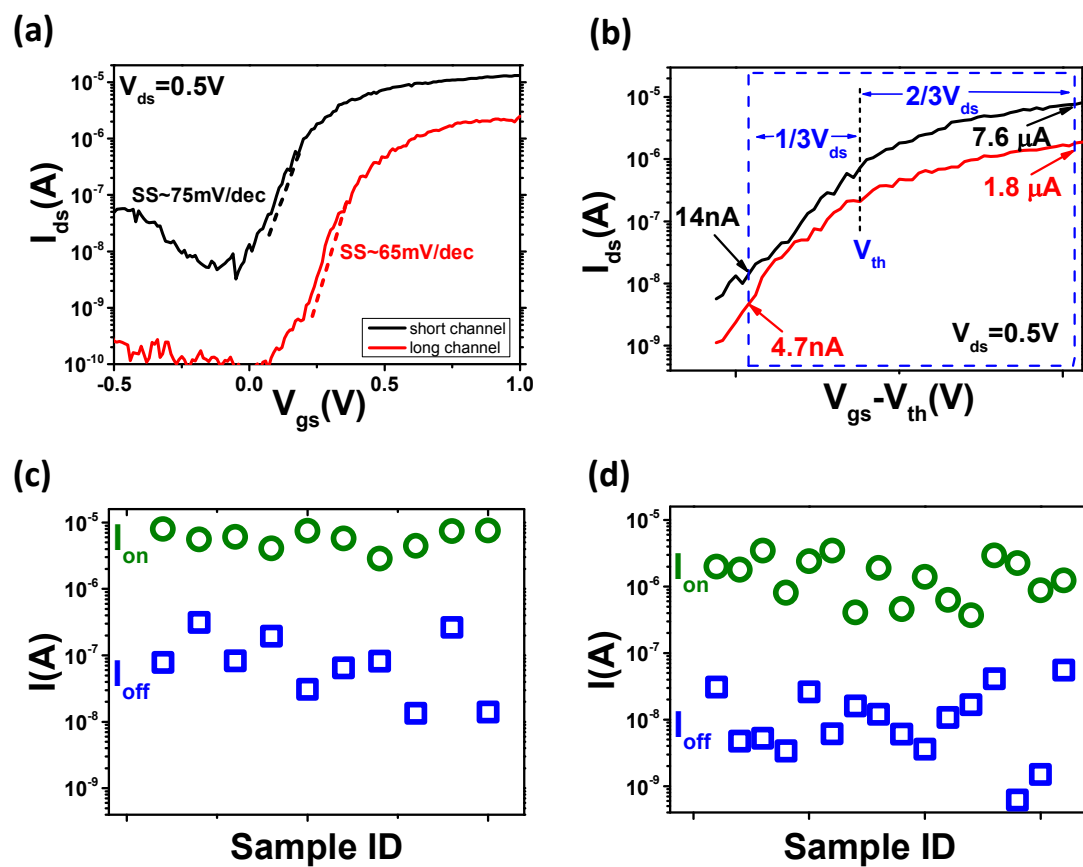
(a)

(b)

(c)

(d)

Figure 2. On- and off-state current extraction for CNT FETs with Y_2O_3 gate dielectric. (a) Transfer characteristics of a typical long gate and a typical short gate CNT FETs at $V_{ds} = 0.5$ V. (b) On- and off-state current extraction. (c) On- and off-state current data extracted from 10 short gate devices of Fig. 1(e). (d) On- and off-state current data extracted from 16 long gate devices of Fig. 1(f).
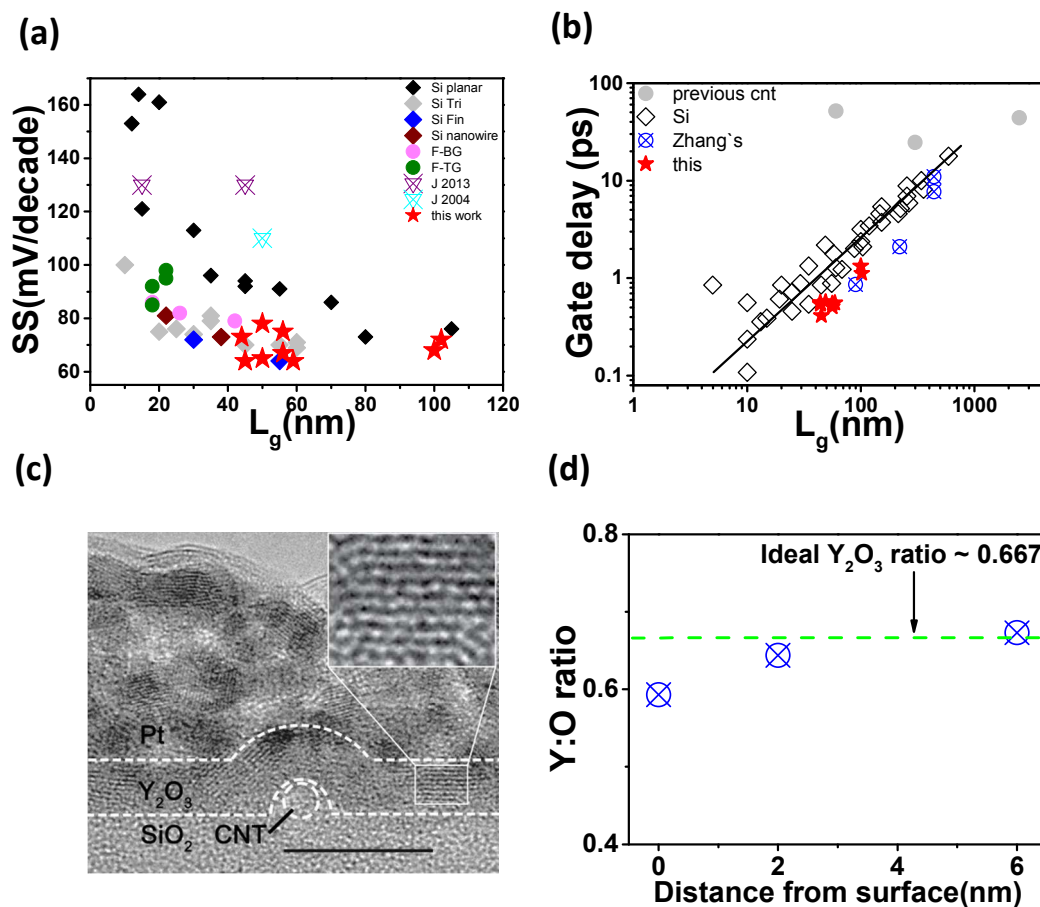
(a)

(b)

(c)

(d)

Figure 3. Performance comparison between CNT FETs and Si devices. The data for Si devices is taken from Ref. [31], F-BG, F-TG, J 2013 and J 2004 are respectively taken from Ref. [25, 21, 23, 22] and Zhang's is taken from Ref. [16, 32]. (a) SS and (b) intrinsic gate delay versus gate length. (c) Typical cross-sectional TEM image showing a CNT device with yttria as gate dielectric. Scale bar denotes 10 nm. Inset at upright corner is an enlarged region of yttria marked by the white square in the image. (d) Atomic ratio of Y to O extracted from XPS results measured at three different depth (0, 2 and 6 nm) from the yttria film surface.
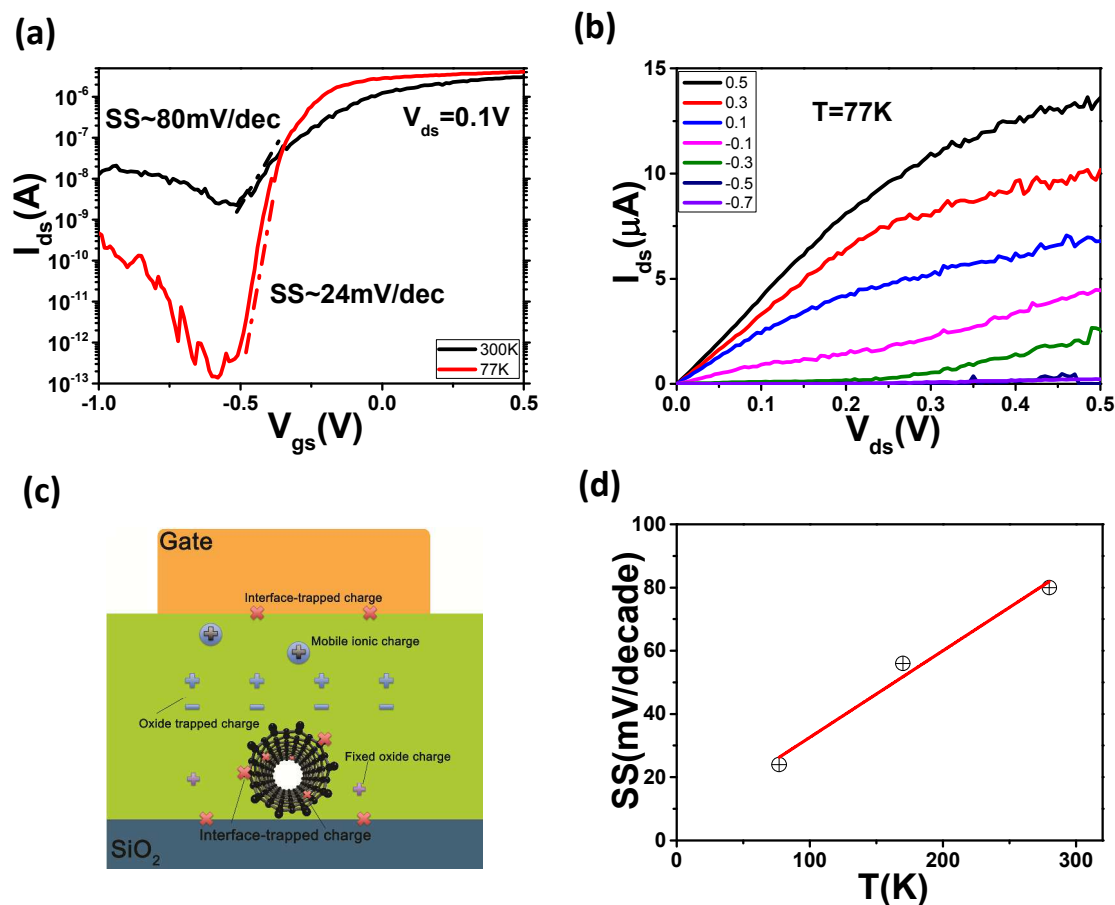
(a)

(b)

(c)

(d)

Figure 4. Low temperature measurements of CNT FETs with Y_2O_3 as gate dielectric layer. (a) Transfer characteristics of one device measured at room temperature (black curve) and 77 K (red curve), at $V_{ds} = 0.1$ V. (b) Output characteristics of the device as (a) measured at 77K. (c) Schematic diagram depicting interface traps in top-gated CNT FETs. (d) Experimental and fitted SS values from room temperature to 77 K.

Table 1. Comparison of some typical gate dielectrics used in CNTFETs

	Oxide	Process	ε_r	m	C_{ox}(pF/cm)	C_{it}(pF/cm)	N_{it}(1e6/cm)@1V
IBM [17]	SiO_2	Thermal oxidation	3.9	12.2	*	*	*
Purdue [20]	SiO_2	Thermal oxidation	3.9	16	0.18	2.72	18
IBM [27]	Lanthanum oxide	MBE/CBE	27	1.22	6.2	1.35	8.4
This work	Y_2O_3	Thermal oxidation	10	1.39	2.16	0.84	5.2