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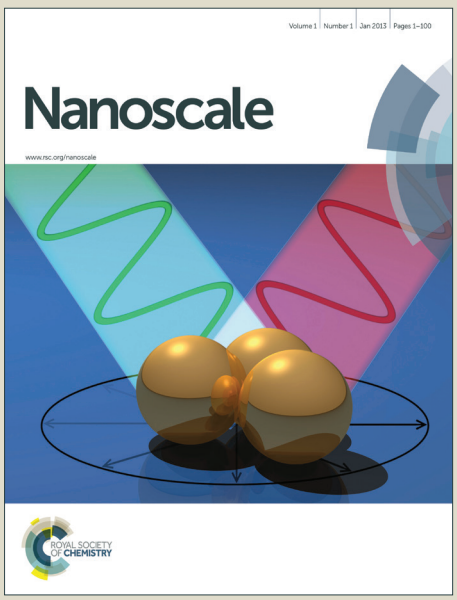

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ARTICLE

Multiprotocol-induced plasticity in artificial synapses

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We suggest a 'universal' electrical circuit for realization of an artificial synapse that exhibits long-term plasticity induced by different protocols. The long-term plasticity of the artificial synapse is basically attributed to the nonvolatile resistance change of the bipolar resistive switch in the circuit. The synaptic behaviours realized by the circuit is termed 'universal' insomuch as i) the shape of the action potential is not required to vary so as to implement different plasticity-induction behaviours, activity-dependent plasticity (ADP) and spike-timing-dependent plasticity (STDP), ii) the behaviours satisfy several essential features of biological chemical synapse including firing-rate and spike-timing encoding and unidirectional synaptic transmission, and iii) both excitatory and inhibitory synapses can be realized using the same circuit but the different diode polarity in the circuit. The feasibility of the suggested circuit as an artificial synapse is demonstrated by conducting circuit calculations and the calculation results are introduced in comparison with biological chemical synapses.

Introduction

Mammalian brains have distinctive features in comparison with digital computers. First, they are typical examples of analogue data processors, enabling the limited number of data process units, i.e. neurons, to deal with a much larger amount of information than digital systems.[1, 2] Second, they process information by means of a large population of neurons (population representation) rather than individual neurons.[2-4] Therefore, as the information encoding and decoding is realized in a statistical manner, erroneous computation occurring in a number of individual neurons have little impact on the overall performance of the population including them, in other words, a fine example of error-tolerant-computing. Third, mammalian brains are able to learn and adapt themselves, which is one of the most distinctive features differentiating them from digital computers. Given these interesting three basic features, there have been attempts to achieve some brain-like on-chip functionalities by means of solid-state devices. Such efforts are referred to as neuromorphic engineering.[5]

The mammalian brain is understood as a complex network of neurons that are connected via synapses; in mammalian brains, on average, there are thousands of synapses (local memory) for each neuron, which makes them a bottleneck of any hardware implementation. Synapses are understood to play significant roles in the aforementioned features of the brain, i.e. population representation[6, 7], memory, and adaptation (learning)[8]. There are two types of synapses: electrical synapse (also known as gap-junction) and chemical synapse.[1] The latter is regarded to be mainly involved in learning and memory in the happocampus[8], while recent study suggests that electrical synapses play a key role in fear learning and memory[9]. Chemical synapses are plastic and involved in learning and memory. In other words, plasticity of their synaptic efficacy defines the connectivity between two associated neurons. Chemical synapses undergo such plastic change upon external electrical stimulation of their associated neurons. It should be noted that the synaptic transmission through a chemical synapse is unidirectional insomuch as the transmission takes place by means of neurotransmitters (chemical messengers) that are released from the 'presynaptic neuron' and arrive at receptors on the 'postsynaptic neuron'.[1] Several plasticity-induction protocols are known, such as activity-dependent plasticity (ADP) and spike-timing-dependent plasticity (STDP), in which a chemical synapse encodes firing rate (activity) information conveyed by the presynaptic neuron and the spike-timing information. On the contrary, electrical synapses are bidirectional, since the transition through their narrow gap-junctions (ca. 3 nm) occurs in an electric manner, which resembles an electric resistor. Chemical synapses have been the main point of focus in neuromorphic engineering. Therefore, in this study, the term 'synapse' denotes a 'chemical synapse' unless otherwise stated.

To date, several candidates for artificial synapses have been proposed, which are based on functional materials such as ferroelectrics[10, 11], phase-change materials[12, 13], ferromagnetic

materials[14], and nanoionic resistive switching materials[15-22] or conventional complementary metal-oxide-semiconductor technologies[23-27]. Recently, a number of neuromorphic circuits based on nanoionic resistive switching materials have been proposed.[28-31] This class of neuromorphic circuits can be classified in a rather general category of "memristive devices and circuis".[32, 33] In general, most of the nanoionic candidates are two-terminal capacitor-shaped devices, thus pre and postsynaptic terminals can be mapped to the device's two electrodes. A popular approach to implementation of synaptic plasticity induction in such a capacitor-shaped synapse is to vary action potential (AP)'s shape that is suitable for each plasticity induction protocol.[11, 12, 14, 20] This approach appears to be suitable for neuromorphic circuits based on synaptic plasticity induced by a particular single protocol. However, regarding the general use of artificial synapses, which is not protocol-specified, such a method perhaps lacks 'universal' feature of artificial synapses in a broader term as a fundamental neuromorphic system building-block. Another potential problem of this approach is the difficulty in generating such shape of APs using artificial neurons. Therefore, the universality of artificial synapses appears to be of significant importance in enabling various induction-protocols to be realized by employing fixed shape of APs, e.g. square-shaped, which can be easily generated by artificial neurons. Besides, several other aspects of artificial synapses should be considered to satisfy general features of biological synapses. These aspects include unidirectional synaptic transmission and excitatory and inhibitory behaviours. These aspects seem to be barely implemented in two-terminal artificial synapses, in particular, those based on bipolar resistive switches (BRSs). The difficulty mostly lies in such that passive stand-alone BRSs cannot avoid bidirectional transmission and realize negative 'static' resistance, required for inhibitory synaptic behaviour.

This paper suggests an artificial synaptic circuit based on a BRS. Circuit calculations were conducted under different stimulation conditions in a time domain so as to identify the successful encoding of presynaptic spikes', i.e. APs', firing rate and timing of pre and postsynaptic spikes. Both pre and postsynaptic spikes were set the same square-shaped voltage pulse of constant height and width. A cation-based Pt/$GeSe_x$/Ag system was regarded as the BRS in the circuit; its behavioural parameters, acquired from the switching measurements, were used in the calculations. The results show good agreement with the mentioned features of biological synapses. The proposed circuit appears to pave the way for realization of hardware-based artificial neural networks (ANNs) as well as computer-simulation-based, i.e. *in silico*, ANNs. This simple circuit may be employed in *in silico* ANNs as an artificial synapse exhibiting multi-protocol-inducing plasticity fulfilling the given characteristics of biological synapses. In addition, our synaptic circuit perhaps promises a progress in building interfaces with biological neurons for a detailed investigation of biological neural behaviour and a further development of brain-machine interfaces.

Experimental

Bipolar switch fabrication

A cation-based Pt(bottom electrode)/$GeSe_x$/Ag(top electrode) BRS was formed in crossbar structure of 10×10 μm^2 area. The thicknesses of the Pt, $GeSe_x$, and Ag layers are 100, 50, and 100 nm, respectively. The Pt bottom electrode (BE) was sputtered onto an oxidized Si wafer with a Ti adhesion layer on top and patterned by using a standard photolithography technique. Thereafter, the $GeSe_x$ solid electrolyte layer was sputtered onto the patterned bottom electrode. Finally, the Ag top electrode (TE) was e-beam-evaporated onto the $GeSe_x$ layer and patterned by using a photolithography technique.

Bipolar switching measurements

Quasi-static current-voltage (*I-V*) characteristics of the BRS were measured by using a Keithley 236 Source Measure Unit. The response of the switch to consecutive voltage pulses was identified using a Tektronix AFG3101 function generator and a Tektronix TDS5104 oscilloscope. The TE was subject to an applied voltage while the BE was grounded.

Circuit calculation

The calculations in this work were performed by using an LTspice circuit simulator. A BRS code was carefully chosen among a number of memristor models, providing the best fitting results. Basically, the model proposed by Biolek *et al*.[34] provides an optimal fit to the experimental results. However, threshold voltages for switching were employed in our circuit calculation. The N-channel metal-oxide-semiconductor field-effect-transistor (n-MOSFET) in this work was simulated by using the sub-0.13 micron BSIM 4 model.[35] All remaining elements were taken directly from the list proposed by the simulator software.

Synaptic calculation

Bipolar switching behaviour of a Pt/$GeSe_x$/Ag switch

A BRS of Pt(bottom electrode)/$GeSe_x$/Ag(top electrode) was regarded to be used in the synaptic circuit; the following synaptic calculations were conducted based on its behavioural parameters. A representative *I-V* curve of the BRS is shown in Figure 1a. Employing Ag electrode in cation-based memory has an advantage of low threshold voltage compared with, for instance, Cu electrode.[36] The BRS exhibits threshold voltages for resistance decrease (V_{set}) and increase (V_{reset}) of approximately 0.2 and –0.2, respectively. The presence of thresholds defines a voltage-window ($V_{reset} - V_{set}$), and thus only voltage staying out of the window allows a nonvolatile change in resistance. In Figure 1a, linear *I-V* behaviour which is zero-crossing is also seen, so that resistance can be regarded constant within the subthreshold voltage-window. These characteristics are of importance in choosing a proper SPICE model of the BRS.

An attempt to further identify the switching behaviour of the BRS was made by observing BRS' responses to consecutive square voltage pulses whose width and height were 1μs and 0.3 V, respectively. As shown in Figure 1b, nonvolatile changes in resistance in both directions were realized by applying the voltage pulse train plotted in the inset. Both increase and decrease in resistance are rather gradual, therefore, the BRS is able to represent various resistance states. Electrical characteristics of the BRS are shown in detail in Supplementary Information.

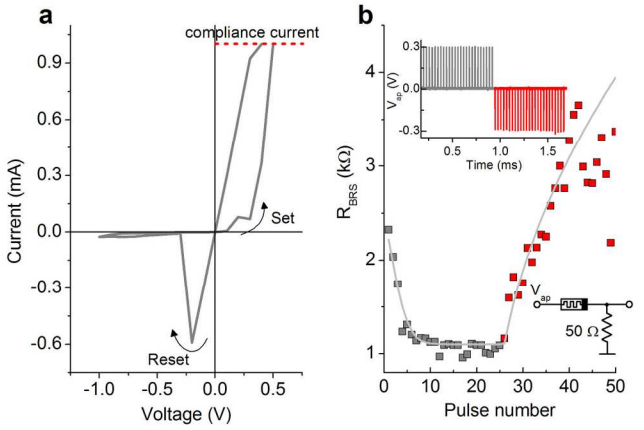

Figure 1. (a) Quasi-static *I-V* behaviour of the Pt/GeSe$_x$/Ag BRS. A compliance current of 1 mA was applied. (b) Change of R_{BRS} upon a voltage train applied to the BRS in the configuration shown in the lower inset. The applied voltage train (V_{ap}) is plotted in the upper inset, where the voltage pulse width and height are 1 μs and 0.3 V, respectively. The grey line denotes a curve fitting the data.

Table 1. Parameters used for the calculations

Parameter		Value
R_{BRS} in the full ON state (R_{ON})		1.4 kΩ
R_{BRS} in the full OFF state (R_{OFF})		7.5 kΩ
Cation mobility (μ_v)	positive V	1.5×10^{-8} m^{2}s^{-1}V^{-1}
	negative V	2.8×10^{-9} m^{2}s^{-1}V^{-1}
Switching layer thickness (D)		50 nm
Window function parameter (p)	positive V	1
	negative V	0.7
V_{reset}		-0.2 V
V_{set}		0.2 V
Threshold function parameter (s)		10^{-3} V
MOSFET channel length/width		150/500 nm
MOSFET V_{th}		0.2 V
MOSFET channel resistance		17.1 kΩ (V_{ds}=1.5 V and V_g=1)

Implementing the above-mentioned switching behaviours using a SPICE model allows much easier and simpler calculations of the aimed circuit. The remarkable characteristics of the BRS are such as i) presence of thresholds, ii) linear *I-V* behaviour, and iii) non-linear resistance change upon consecutive voltage pulses. Given these features, the model proposed by Biolek *et al.*[34] together with the threshold function most likely provides the best fitting result; the differential equation of the state variable w is given by

$$\frac{dw}{dt} = \frac{\mu_v R_{ON}}{D^2} \cdot I(t) \cdot f_w(w) \cdot f_{th}(V), \quad (1)$$

where w and μ_v *nominally* denote the length of Ag-filaments within the initially insulating electrolyte layer of thickness D and the mobility of the Ag ions confined within w. R_{ON} denotes the resistance of the BRS in the extreme case when w=D, i.e. the lowest resistance of the BRS. f_w indicates the window function implementing nonlinear migration of the nominal Ag-filament/electrolyte boundary across the thickness D. In this work, a new window function, which provided the best fitting, was introduced and is given by

$$f_w(w) = \left(\frac{\cos(\pi w)+1}{2}\right)^p, p > 0, \quad (2)$$

where p is a window function parameter. The aforementioned threshold voltages for nonvolatile switching are implemented in Eq.(1) by introducing the threshold function f_{th} given by

$$f_{th}(V) = e^{-(V_{TH}-|V|)/s}, V_{TH} \in \{V_{set}, V_{reset}\}, \quad (3)$$

where s is a parameter determining the slope of the threshold function in the vicinity of V_{TH}. The smaller s, the steeper a change in f_{th} with respect to $|V|$ in the vicinity of V_{TH}.

Note that this SPICE model is highly empirical, which describes the bipolar switching kinetics of the Ag-based BRS under limited conditions such as pulse height and width up to 0.6 V and 5 μs, respectively (see Supplementary Information). Thus, this model including the parameters is unlikely useful unless the BRS is subject to the given range of input. In particular, the switching voltages (V_{reset} and V_{set}) are strongly dependent on the duration, i.e. pulse width.[37, 38] A generic model of cation-based switching, considering the source and sink of cations, i.e. redox reactions, describes switching kinetics in extremely wide time and voltage domains.[37, 38] Such a model can cover all approximations, e.g. the SPICE model in the present study, localized in the domains.

Using this SPICE model with the parameters listed in Table 1, the change of R_{BRS} upon the voltage pulse train, shown in Figure 1b, was successfully fitted (grey line in Figure 1b). Note that different μ_v and p values for different electric field directions, i.e. asymmetric migration-rate constants, were used in this fitting. These parameters form the basis for the following circuit calculations. The parameters in use were extracted from statistical analysis on the BRS' responses to different inputs (pulse width: 0.5 – 1.5 μs and height: 0.3 – 0.6 V).

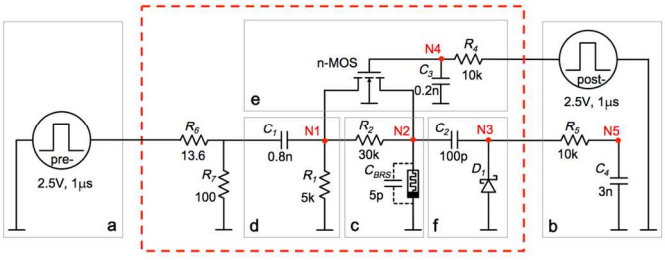

Figure 2. Electrical circuit for the artificial synapse (red dashed line) and a circuit for synaptic plasticity evaluation.

Circuit configuration

The circuit used for the multiprotocol-induced plasticity implementation is shown in Figure 2. Pre and postsynaptic spike-firing was simulated by invoking two voltage pulse generators, which are shown in Figures 2a and b, respectively. The width and the amplitude of each spike were set 1 μs and 2.5 V, respectively. Note that spike shapes were not varied throughout the whole study; instead, inter-spike interval (ISI) and pre and postsynaptic spike-timing were varying time-domain parameters. The RC integrator in Figure 1b was employed to evaluate the change of postsynaptic membrane potential upon the synaptic efficacy; the integrator corresponds to the membrane of the postsynaptic neuron. In this work, synaptic plasticity will mainly be described in terms of postsynaptic potential (PSP), so that potentiation and depression were defined by relative changes in PSP, i.e. ΔPSP, upon plasticity induction trials. This circuit was aimed to encode presynaptic activity (firing rate) and the timing of pre and postsynaptic spikes for both excitatory and inhibitory synapse cases. The subcircuits in Figures 2c, d, e, and f play key roles in synaptic plasticity induction.

The essential features of long-term plasticity of the biological synapse, long-term potentiation (LTP) and long-term depression (LTD), were realized by using the BRS, which is placed in Figure 2c. As discussed earlier, both polarities are required to alter the resistance in different directions, i.e. the resistance increases and decreases under negative and positive voltage, respectively. In the circuit shown in Figure 2, a change in R_{BRS} leads to a change in voltage drop across the BRS, and consequently a change in PSP evolution in due course. For instance, an increase in R_{BRS} results in potentiation, since the resistance increase elevates the voltage at node N2, which consequently elevates the PSP, i.e. causes potentiation. A decrease in R_{BRS} results in a change in the opposite direction, so that depression is achieved. It is therefore apparent that the role of a BRS in an artificial electronic synapse depends on the circuit configuration. For instance, in a typical single BRS-based electronic synapse, where pre and postsynaptic spikes are incident on the two terminals of the BRS, potentiation and depression are realized by a decrease and an increase in the resistance, respectively.[15, 16, 20] Note that C_{BRS} denotes the capacitance of the BRS due to the use of the solid electrolyte which is dielectric.

The subcircuit in Figure 2d plays an important role in realization of ADP. Employing charging and discharging of capacitor C_1 enables the polarity of a voltage, applied to the BRS, i.e. V_{N2}, to be altered without changing the polarity of the presynaptic spikes. In addition, the contribution of each charging and discharging effect to the change of R_{BRS} varies upon charging and discharging time-windows. Thus, changing the ISI, while using identical spike widths, realizes a change in their relative contributions, which implies ADP. The MOSFET shown in Figure 2e, 'crops' a part of the RC output signal at node N1 and transmits it to the BRS; cropping is controlled by the gate to which postsynaptic connection is applied. Therefore, a voltage assigned to the BRS, i.e. V_{N2}, depends on the pre and postsynaptic spike-timing, hence, implementing STDP. The subcircuit in Figure 2f determines either excitatory or inhibitory synaptic behaviour depending on the polarity of diodes D_1. Under the current configuration, the subcircuit in Figure 2f implements an excitatory synapse and an inhibitory configuration can be realized by simply flipping the polarity of the diode. The diode is employed to introduce an asymmetric V_{N3} profile when charging and discharging capacitor C_2, which in turn leads to asymmetry in V_{N5}, i.e. *PSP*. This asymmetry is attributed to the asymmetric current-voltage relationship of the diode. Unless otherwise stated, the calculations in the following sections are conducted on excitatory synapse. The detail of plasticity induction of the given circuit is addressed in following subsections.

The circuit parameters listed in Table 1 realize the synaptic plasticity in an activity domain below 500 kHz. However, depending on the purpose of the artificial synapse, the activity-window can be optimized by changing the circuit parameters, in particular, resistance and capacitor values.

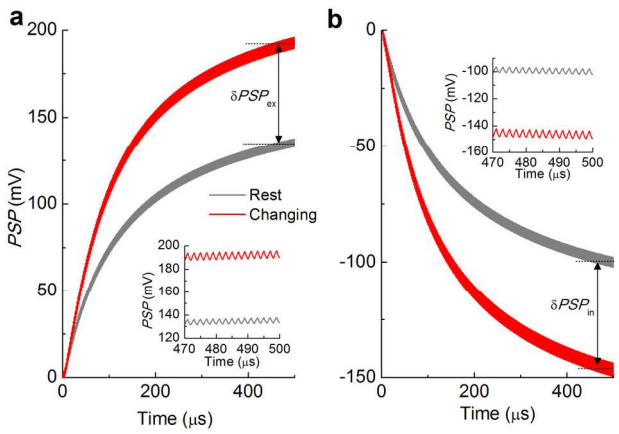

Figure 3. PSP evolution for the 'rest' and 'changing' synaptic efficacy cases, calculated on (a) excitatory and (b) inhibitory synapses. For both cases, presynaptic activity was set 500 kHz to realize HFS-induced LTP. δ*PSP* denotes a difference in PSP between the 'rest' and 'changing' efficacy runs at a given time. The number of voltage pulses for the time period (0 – 500 μs) is 250. The PSP evolution in the time range 470 – 500 μs is zoomed in in the insets.

PSP evaluation

As mentioned earlier, the membrane model of a postsynaptic neuron was implemented by means of the RC integrator shown in Figure 2b. The PSP was a measure of the electrostatic potential difference across capacitor C_4. A change in synaptic efficacy upon plasticity induction was evaluated by calculating a difference in PSP between 'changing' and 'rest' efficacy cases at a certain time after stimulation; $\Delta PSP=(PSP_c-PSP_0)/PSP_0\times100$, where PSP_c and PSP_0 denote PSPs for the changing and the rest efficacy cases, respectively. For instance, an LTP-caused deviation of PSP evolution from the rest efficacy case is plotted in Figure 3. The LTP was achieved by applying a high frequency stimulus (HFS), 500 kHz, to the presynaptic terminal in Figure 2a. ΔPSP was evaluated at 500 μs. On the contrary, LTD rather decreases PSP evolution from

the rest case, showing negative ΔPSP. In case of LTP, R_{BRS} increases, leading to elevation of V_{N2}. This in turn elevates V_{N5} denoting the PSP. During LTD, R_{BRS} change proceeds in the opposite direction, so that V_{N2} decreases, and so does V_{N5}, compared to the rest efficacy case. Note that the PSP varies upon the capacitance of the integrator, which is of the postsynaptic neuron; the choice of the capacitance is a matter of artificial neuron rather than synapse. For all calculations in this study C_4 was set 3 nF. Note that the read-out time is measured from the initiation of pulse application and the read-out time for each synaptic behaviour is specified since PSP evaluation depends on read-out time. One can identify a change in synaptic efficacy after a training period; however it gives almost the same percentage change as long as the BRS is of non-volatile resistance change.

Results

Activity-dependent plasticity

The charging and discharging of capacitor C_1 in Figure 2d varies upon the ISI of the presynaptic spike-train. In particular, when it comes to ISI values that are close to the characteristic RC time-constant of the circuit (ca. 3.2 μs), the discharging as well as the subsequent charging is significantly affected by the ISI. Subsequently, the output voltage from the RC circuit depends on the ISI, i.e. presynaptic activity. Utilizing these charging and discharging effects enables the BRS to undergo resistance change in both directions, i.e. up and down, while the polarity of incident spikes is maintained positive.

The PSP of the circuit was evaluated by applying presynaptic spike-trains of different ISI values, 39, 4.05, and 4.29 μs, corresponding to 25, 198, and 700 kHz in activity, respectively, while no postsynaptic spikes were applied. Figure 4 shows the calculated transient profile of V_{N2}, i.e. a voltage across the BRS, and the corresponding change of R_{BRS} for the three different activities. The shaded regions in the figure denote a subthreshold voltage range (-0.2 to 0.2 V) for the change of R_{BRS}; voltage within the range does not lead to resistance change. Capacitor C_1 is fully discharged during the ISI period when the ISI largely exceeds the RC time-constant (see the upper panel of Figure 4a). In this case, the maximum amplitudes of both negative and positive output voltage barely change upon spike number. Upon an incident single AP, induced V_{N2} during charging and discharging is asymmetric; the negative maximum of V_{N2} is much larger than the positive one as can be seen in Figure 4a. Despite this asymmetry, the contribution of the negative maximum to R_{BRS} change is not dominant over that of the positive one because of the asymmetry of μ_v, i.e. higher under positive voltage than negative one. Therefore, at each incident, only a slight decrease in R_{RBS} is seen, leading to LTD (see Figure 4a bottom panel).

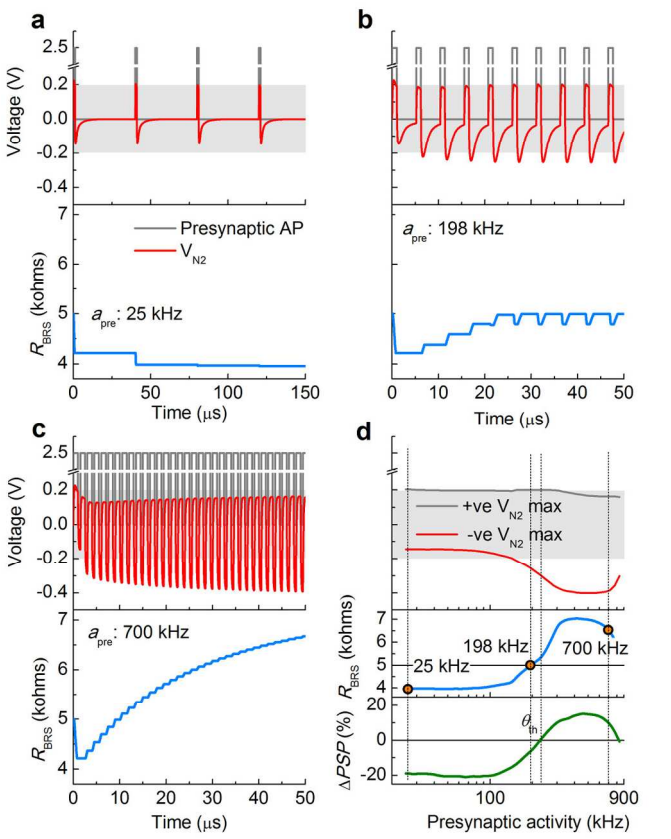

Figure 4. Transient V_{N2} profile and the corresponding R_{BRS} under a presynaptic AP train at activities (a_{pre}) of (a) 25, (b) 198, and (c) 700 kHz. In all cases, the initial resistance was set to 5 kΩ. The grey zone indicates the subthreshold voltage region, i.e. $V_{reset} < V < V_{set}$, for the change of R_{BRS}. (d) The positive and negative V_{N2} maxima with respect to presynaptic activity. The corresponding R_{BRS} and ΔPSP are also plotted. The threshold activity θ_{th} (ca. 198 kHz) for LTP is designated using a dashed line. The PSP was read at 50 μs for all three cases.

In contrast, when the ISI decreases and it becomes close to or even shorter than the RC time-constant, full discharge is prevented, pushing the transient voltage towards negative values (see upper panels in Figures 4b and c). This eventually lets the negative voltage peaks largely exceed V_{reset}, while the positive peaks decrease, resulting in a stepwise increase in R_{BRS} as shown in Figures 4b and c. The positive and negative voltage peaks in the steady state, the corresponding R_{BRS}, and the ΔPSP value read at 50 μs are plotted in an activity domain in Figure 4d. These results identify that the presynaptic activity information is successfully encoded in the synaptic circuit, exhibiting a threshold activity θ_{th} for LTP induction (ca. 198 kHz) as shown in Figure 4d. Activities below the threshold induce LTD rather than LTP. These features are well consistent with ADP in biological synapses. In addition, the calculated ADP behaviour avoids unlimited growth of synaptic efficacy. In fact, limited growth of synaptic efficacy is seen in biological synapses.[39, 40] This limited growth in Figure 4d is understood in terms of switching kinetics of the BRS. The higher the presynaptic activity is, the narrower the negative effective voltage at node N2 is. Thus, switching time sufficient to cause a large change in R_{BRS} is barely given to the BRS at high

activities despite the high negative voltage peaks. Given this trade-off between the voltage peak height and the voltage application time, a R_{BRS} increase rate tends to decrease at high activities slightly.

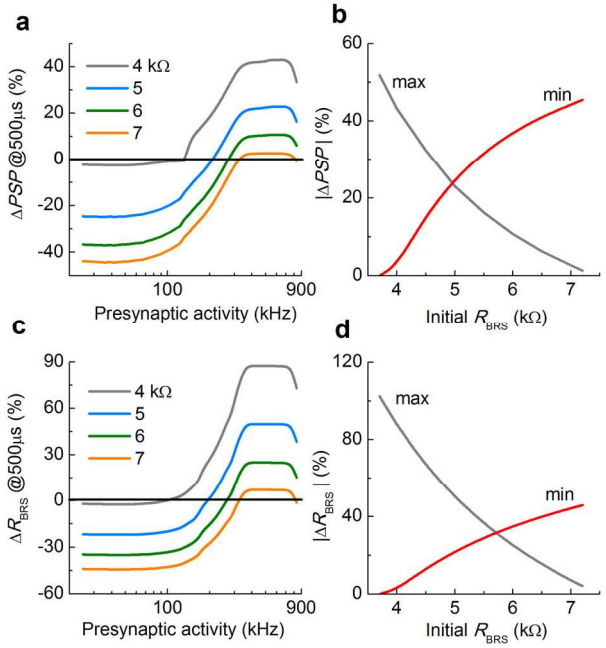

Figure 5. ADP behaviour and the corresponding ΔR_{BRS} of the artificial synapse were calculated with different initial R_{BRS} values, i.e. different initial synaptic efficacies, and plotted in (a) and (c), respectively. The maximum of positive ΔPSP due to LTP and the minimum of negative one due to LTD are plotted in (b). The corresponding maximum and minimum of ΔR_{BRS} are shown in (d). All ΔPSP and ΔR_{BRS} values were taken at 500 μs.

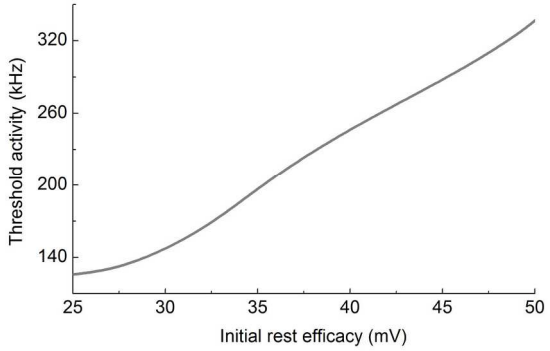

Figure 6. Dependence of threshold activity for LTP in ADP on initial synaptic efficacy. The PSP was evaluated at 500 μs.

The history-depending BRS allows its various initial resistance states on each induction trial, implying that the artificial synapse is history-dependent. The ADP behaviour was calculated for different initial R_{BRS} (4 – 7 kΩ) and is plotted in Figure 5a. High initial resistances mean high initial synaptic efficacies that can be achieved by previous LTP induction. As shown in Figure 5b, the positive ΔPSP at high activities tends to continuously decrease with the initial resistance while the negative ΔPSP exhibits the opposite behaviour. The continuous decrease in the positive ΔPSP indicates the fact that the limited synaptic efficacy, i.e. saturation, is achievable by repeating LTP induction trials. The corresponding change of R_{BRS} at the various initial R_{BRS} in an activity domain is shown in Figure 5c. Note that the PSP was read at 500 μs so as to observe more obvious ADP behaviour.

Regardless of the initial resistance, a threshold activity θ_{th} for the transition between LTD and LTP is noticed in Figure 5a. Such thresholds have been well known in biological synapses, working as criteria for either LTD or LTP in an activity domain. There have been several empirical models accounting for the activity-dependent plasticity of chemical synapses by taking into account such thresholds, e.g. the Bienenstock-Cooper-Munro (BCM) rule[41] and the Oja rule[42]. Notably, in our artificial synapse, the threshold activity increase with the initial synaptic efficacy, i.e. higher activities are required to induce LTP as the initial efficacy increases. The relationship is seen in Figure 6, where initial efficacy was described as a 'rest' PSP value evaluated at 500 μs. This implies that the threshold is given by a function of synaptic efficacy.

Spike-timing-dependent plasticity

The n-MOSFET in Figure 2e crops the RC circuit's output voltage at node N1 upon arrival of a postsynaptic spike at the gate terminal (turning on the channel when $V_{N4} > V_{th}$=0.2 V) and transmits the cropped voltage to node N2. However, capacitor C_3 and resistor R_4 in Figure 2e delay transmission of the postsynaptic spike to node N4, and thus the consequent elevation of V_{N4}. Therefore, a time lag between the postsynaptic spike firing and the channel's turn-on occurs.

Upon arrival of the postsynaptic spike at the MOSFET and the channel's turn-on in due course, V_{N2} increases insomuch as the channel works as a bypass between nodes N1 and N2. The relative timing of the pre and the postsynaptic spikes therefore determines relative contributions of positive and negative voltage inputs to R_{BRS} change. These aspects of the circuit realize general features of STDP in biological synapses, such as encoding the timing of pre and postsynaptic spikes and LTP-induction at even lower presynaptic activities than the ADP threshold θ_{th}.[43-45] The STDP behaviour of the circuit at a particular interval between a pre and a postsynaptic spike Δt was evaluated by applying a train of several pairs of pre and postsynaptic spikes with certain time interval. By varying the spike interval on each trial, the entire STDP characteristics of the circuit were evaluated. The frequency of the voltage-pair train was set 50 kHz for all calculations, which is sufficiently low to differentiate the STDP implementation from the LTP induction by HFS in ADP. Note that Δt is taken positive when the presynaptic spike is ahead of the postsynaptic. The arrival and termination times of a presynaptic (postsynaptic) spike are denoted by t_{pre1} (t_{post1}) and t_{pre2} (t_{post2}), respectively, so that $\Delta t = t_{post1} - t_{pre1}$.

Calculation results for ΔPSP and R_{BRS} are shown in Figures 7a. The number of spike-pairs on each trial, i.e. in each voltage train, was 25, which corresponds to 500 μs in time. As shown in the inset of Figure 7a, the change of the PSP upon the spike-timing is proportional to the number of pairs. The calculated

STDP characteristics are in agreement with those of biological synapses; positive Δt, i.e. a presynaptic spike ahead of a postsynaptic, leads to LTP and negative Δt to LTD. Time-windows for the LTD and the LTP are approximately 3 and 1.5 μs, respectively. There is a transition zone of approximately 1.4 μs width between the LTD- and LTP-windows, which is depicted using a grey zone. The centre of the zone is placed at around Δt =0.

To highlight the STDP features, V_{N2} and the corresponding R_{BRS} change were evaluated in a time domain at three representative Δt points, -0.73, 0.12, and 0.52 μs, at which i) the maximum LTD, ii) a negligible change in the PSP, and iii) the maximum LTP are shown, respectively. Their profiles are plotted in Figures 7b, c, and d, respectively. Note that, due to capacitor C_3 and resistor R_4 in Figure 2e, the take-off and the peak of V_{N4} indicate the arrival and the termination of the postsynaptic spike, respectively.

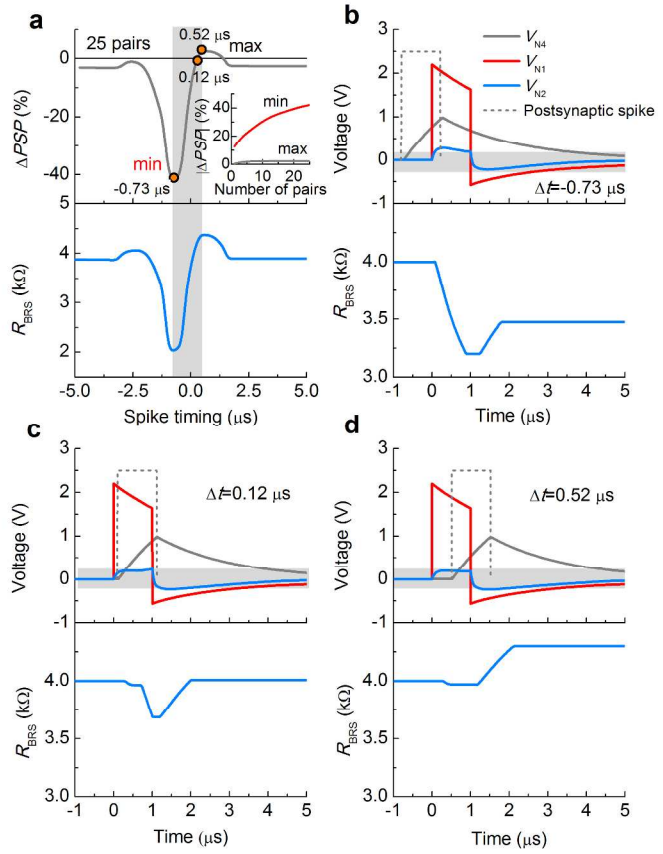

Figure 7. (a) Upper panel: Calculated STDP behaviour of the artificial synapse. The STDP was evaluated after 25 pairs of pre and postsynaptic spikes at 50 kHz, corresponding to a read-out time of 500 μs. The larger the number of pairs, the higher $|\Delta PSP|$, as shown in the inset of the figure. Lower panel: The corresponding R_{BRS} change with respect to timing of pre and postsynaptic spikes. Indicated using the cycles are the three timing values (-0.73, 0.12, and 0.52 μs) when the LTD maximum, negligible plasticity in total, and the LTP maximum occur respectively. The profiles of V_{N1}, V_{N2}, and V_{N4} in a time domain are evaluated for the three timing values: (b) -0.73, (c) 0.12, and (d) 0.52 μs. For each case, R_{BRS} in the given timing range is also plotted in the lower panel of each figure [(b), (c), and (d)]. The initial resistance was set to 4 kΩ.

i) Δt=-0.73 μs: $t_{post1} < t_{pre1} < t_{post2} < t_{pre2}$. The postsynaptic spike arrives 0.73 μs ahead of the presynaptic spike, leading to the profile of V_{N2}, shown in Figure 7b. Given that the channel of the n-MOSFET works as a bypass upon arrival of the postsynaptic spike, which turns on the channel, the resistance in total between nodes N1 and N2 decreases, and thus V_{N2} becomes higher than that in the absence of the postsynaptic spike (compare Figures 4a and 7b). In the time-window, $0 \le t \le 1$ μs, V_{N2} exceeds V_{set}, leading to a decrease in R_{BRS} as shown in the lower panel of Figure 7b. Upon the termination of the presynaptic spike the negative maximum of V_{N2} is reached, which is higher than that shown in case of ADP (see Figure 4a). This transient negative V_{N2} leads to an increase in R_{RBS} in due course. Given the asymmetry of μ_v, the contribution of the positive V_{N2} to the R_{BRS} change is larger than the negative voltage. This effect is shown in the lower panel of Figure 7b. Thus, the overall change of R_{BRS} is negative, implying LTD.

ii) Δt=0.12 μs: $t_{pre1} < t_{post1} < t_{pre2} < t_{post2}$. In this case, the presynaptic spike arrival (t_{post1}) is 0.12 μs ahead of the postsynaptic, which means the postsynaptic spike arrives while the presynaptic spike is present. The profile of V_{N2} and the consequent R_{BRS} change are shown in Figure 7c. Upon arrival of the postsynaptic spike the voltage increases and crosses V_{set}, leading to a negative change in R_{BRS}. This negative change is maintained until the presynaptic spike terminates ($t_{post1} \le t \le t_{pre2}$). In the time range $t_{pre2} < t \le t_{post2}$, the absence of the presynaptic spike triggers the discharging of capacitor C_1. However, the presence of the bypass, due to the postsynaptic spike, maintains the higher $|V_{N2}|$ (V_{N2}<0), which exceeds V_{reset}. Thus, a positive change in R_{BRS} is achieved during this time period. As can be seen in the lower panel of Figure 7c, the positive and negative voltage contributions to the change of R_{BRS} are almost identical, resulting in the negligible change in R_{BRS}.

iii) Δt=0.52 μs: $t_{pre1} < t_{post1} < t_{pre2} < t_{post2}$. Since the termination of the postsynaptic spike is behind that of the presynaptic spike, the effect of the bypass on an increase in V_{N2} and the consequent decrease in R_{BRS} are not large. For the same reason, $|V_{N2}|$ (V_{N2}<0) is elevated in $t_{pre2} < t < t_{post2}$, resulting in a relatively large contribution of the negative voltage to R_{BRS} change. The change of R_{BRS} in total is therefore positive, which implies LTP.

In case of large interval between the pre and postsynaptic spikes, i.e. when Δt goes out of the LTD- / LTP-window, no change in R_{BRS} arises from the STDP protocol, since spikes separated by such large interval do not change $|V_{N2}|$ largely enough to differentiate it from case of low frequency stimulus (LFS) in the ADP. In Figure 7, a small offset of the ΔPSP is seen outside the time-windows. This offset arises from the LFS-induced LTD at 50 kHz, which is consistent with the ADP behaviour shown in Figure 5a. This observation implies the crosstalk between the two different induction protocols. It is found that the STDP cannot be achieved in a high frequency range insomuch as no LTD in the STDP is observable. This

behaviour is well consistent with biological synaptic behaviour, which will be addressed in Discussion section.

Capacitor C_3 and resistor R_4 mostly determine the overlap between V_{N1} and V_{N4}, arising from the pre and the postsynaptic spike, respectively, in the time domain. Thus, the STDP behaviour, such as the centre of the transition zone bet

ween the LTD- and LTP-windows and the widths of the windows, can be designed by changing C_3 and R_4.

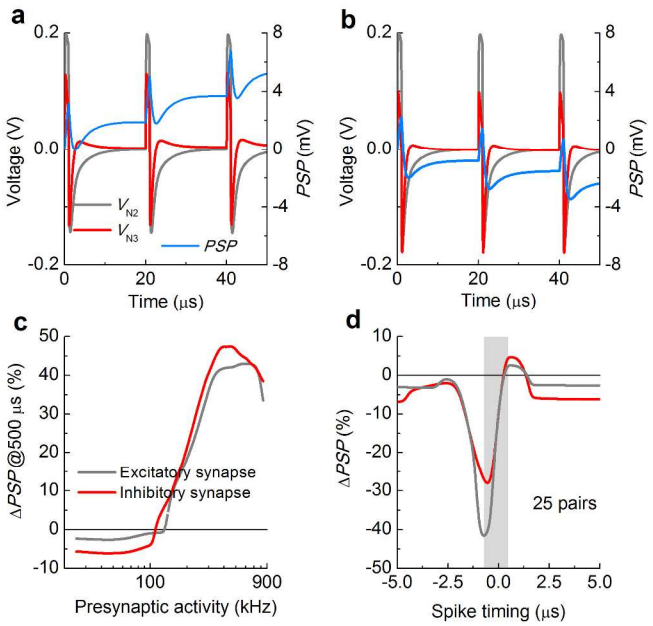

Figure 8. V_{N2}, V_{N3}, and the consequent PSP profiles are plotted for (a) excitatory and (b) inhibitory synapses. In both cases, the calculations were conducted at a presynaptic activity of 50 kHz. The calculated (a) ADP and (b) STDP behaviours in both excitatory and inhibitory synapses are plotted. The ΔPSP in (c) was read at 500 μs at each presynaptic activity and that in (d) after 25 pairs of pre and postsynaptic spikes, corresponding to a read-out time of 500 μs.

Synaptic excitation and inhibition

Diode D_1 in the subcircuit in Figure 2f results in different RC time-constants depending on the polarity of V_{N3} and the diode configuration. In addition, the polarity of diode D_1 strongly affects V_{N3} while charging and discharging capacitor C_2. While charging, a reverse bias voltage is applied to diode D_1, so that the resistance of diode D_1 is high. Thus, V_{N3} becomes positively high, which in turn increases the PSP, i.e. V_{N5}. However, discharging capacitor C_2 confronts a different condition; while discharging capacitor C_2, i.e. $V_{N3} < 0$, electrons released from capacitor C_2 see a much lower resistance of diode D_1 as the diode is forward-biased. Consequently, the deviation of V_{N3} from the ground potential is much less than that in the charging case, meaning the contribution of discharging of capacitor C_2 to the PSP is not as prominent as that of charging. Given this condition, the PSP evolves into a positive value. The evolution of PSP during LFS-induced LTD for excitatory synapse can be seen in Figure 8a. It is seen that the positive PSP evolution arises from the charging process rather than discharging process.

When it comes to inhibitory synapse, the evolution of the PSP should proceed towards negative values. This can be achieved by the contribution of discharging of capacitor C_2 to the PSP evolution, which is dominant over that of charging. Flipping the polarity of diode D_1 ensures a lower but still positive V_{N3} value than the case of the diode polarity shown in Figure 2. That is, during charging of capacitor C_2, diode D_1 is subject to a forward bias voltage, so that the resistance of diode D_1 is low, leading to small V_{N3} compared with the excitatory synapse case. However, during discharging, diode D_1 is subject to a reverse bias voltage, so that electrons released from capacitor C_2 confront high resistance through diode D_1. Thus, V_{N3} shifts towards higher negative values. As a matter of fact, the negative maxima of V_{N3} for excitatory and inhibitory cases are approximately -0.131 and -0.172 V, respectively. This mismatch between the contributions of charging and discharging of capacitor C_2 leads to evolution of negative PSP, i.e. inhibitory synaptic behaviour. Indeed, as shown in Figure 8b (LFS-induced LTD case), the negative PSP evolution arises from the discharging process unlike the positive PSP evolution case (excitatory synaptic behaviour). The ADP and STDP calculations were performed on the inhibitory synapse and the results are plotted in Figures 8c and d. Note that C_2 for the inhibitory synapse was 70 pF since the lower capacitance than that for the excitatory synapse gives a better correspondence with the excitatory synapse case. It is seen that both ADP and STDP behaviours are successfully implemented in the inhibitory synapse.

Unidirectional synaptic transmission

As illustrated in Figure 2, application of postsynaptic spikes to the circuit turns on the channel of the n-MOSFET. However, without presynaptic spikes, turning on the channel barely leads to the change of V_{N2}, so that plasticity cannot solely be induced by the arrival of the postsynaptic spikes. This implies the fact that the synaptic transmission is unidirectional, i.e. from the presynaptic neuron to the post synaptic one. As stated earlier, the unidirectional synaptic transmission is a key feature of biological synapses, which defines pre and postsynaptic neurons. This unidirectionality cannot be achieved in two-terminal capacitor-type synapses employing memristive devices, given that bidirectional current flow is unquestionably required for long-term plasticity, i.e. LTD and LTP, in such artificial synapses.

Discussion

The STDP behaviour in our artificial synapse is activated at only low presynaptic activity. High presynaptic activity allows the ADP behaviour to be dominant over the STDP, so that only LTP is seen. The extinction of the STDP, i.e. LTD to be specific, at high presynaptic activity is understood in terms of the relative contributions of the charging and discharging effects to the voltage across the BRS, i.e. V_{N2}. The positive

maximum of V_{N2} shifts towards the negative side with respect to presynaptic activity as shown in Figure 4d. Thus, the lack of the positive voltage contribution to the change of R_{BRS} prevents the LTD in the STDP despite the V_{N2} elevation upon arrival of postsynaptic spikes at the n-MOSFET. In addition, as shown in Figure 7, the STDP behaviour at low presynaptic activity and timing out of the time-windows exhibits LTD. This LTD basically arises from the low presynaptic activity, 50 kHz, which triggers LTD in the ADP. Given these examples, the crosstalk between the protocols is estimated. Indeed, such crosstalk has been found in biological synapses, implying the good agreement of our artificial synapse with biological one.[46]

Several complex effects on plasticity induction, e.g. complex spike-train, such as triplet and quadruplet spike-train, effects on STDP[47] underpin a further research to be implemented. There may be much more effects that are required to be implemented in artificial synapses. Considering effects that play important roles in given applications of artificial synapses, the suggested circuit needs to be modified in the future. In addition, the detailed synaptic behaviours of the circuit can be fine-tuned by adjusting the components in the circuit. In particular, several components in the circuit as well as the height and width of an AP should be carefully chosen by taking into account the detailed resistive switching behaviour of the BRS. Further, artificial neurons should be of concern in optimizing the circuit components since the shape of the AP produced by the artificial neuron is supposed to be restricted by the artificial neurons.

Regarding integration of this synaptic circuit, scalability is of significant concern. In comparison with the state-of-the-art CMOS synapses[25, 26], a less number of circuit components, particularly transistor, in a unit synapse is beneficial in terms of fabrication cost. However, the obstacle to scalability is the requirement of such large capacitance (C_I: 0.8 nF) mainly for the ADP realization compared with the CMOS synapses[25]. Nonetheless, it should be emphasized that the focus of our synaptic circuit is on its functionality capable of multiprotocol-induced plasticity, and thus it cannot be directly compared with the CMOS synapses that implement particular protocols separately. A possible solution to such a large area of a unit synapse is probably use of high-k dielectrics or/and three-dimensional capacitors, which enable a large increase in capacitance per unit area of a wafer.[48] Regarding power consumption, the synaptic circuit consumes approximately 1 mW/spike, and thus 1 nJ/spike. The ADP induction, shown in Figure 5, costs a minimum of 13 nJ (at 25 kHz, 12 spikes) and a maximum of 275 nJ (at 900 kHz, 450 spikes). Certainly, the energy consumption is larger than several CMOS synapses, e.g. recently reported CMOS synapse implementing STDP, which consumes 0.37 pJ/spike.[27] Thus, a further optimization of the circuit is required for minimization of synapse area as well as energy consumption, which is indeed beyond the scope of this work. Thus, we leave the question open for the moment.

The behaviour of the BRS as the key component of the proposed synaptic circuit has a significant impact on synaptic plasticity of the circuit in detail. That is, different BRS (memristor) models result in differences in detailed synaptic behaviour. Therefore, a proper BRS model should be chosen by taking into account the experimental switching behaviour of the BRS under consideration. Other types of BRSs than the Pt/$GeSe_x$/Ag switch can be utilized in the synaptic circuit with optimal values of the circuit components. Accordingly, the BRS model is required to be replaced by that reflecting the reality of the BRS in use. Since the first suggestion of a BRS model by Strukov et al.[49] in 2008, the original model has been largely modified for the fidelity to the reality of BRSs.[34, 50-52] Recent review papers on BRS models well sort available models and their characteristics.[53, 54]

Conclusions

We suggested an electrical circuit able to encode presynaptic activity and timing of pre and postsynaptic spikes. The circuit also satisfies general features of biological synapses such as excitatory and inhibitory synaptic behaviours and unidirectional, i.e. pre → postsynaptic neuron, synaptic transmission. The calculation results let us know the feasibility of the circuit as an artificial synapse, regarding the successful implementation of ADP and STDP behaviours. Of course, synaptic functionalities required to be implemented in artificial synapses depend on the purposes of the systems including the synapses, so that only particular functionalities rather than general ones are necessary to be realized.[21, 28, 30, 31] However, for the moment, it is of significant importance to achieve artificial synapses implementing general aspects of biological synapses, which can be versatile. Thus, they can be used in various neuromorphic systems for diverse purposes.

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Notes and references

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