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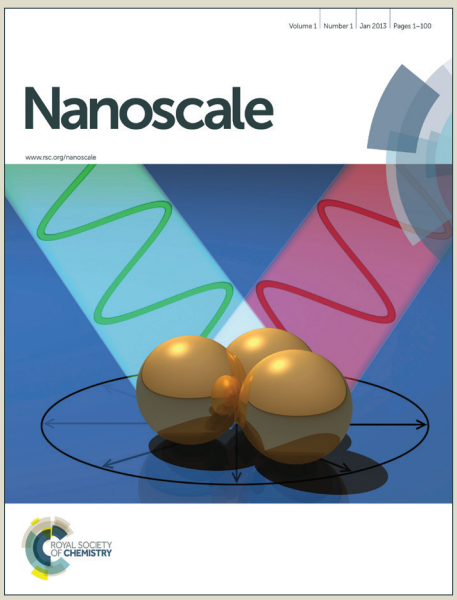

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Direct growth of patterned graphene on SiO_2 substrates without the use of catalysts or lithography†

Yong Seung Kim[1,2], Kisu Joo[3], Sahng-Kyoon Jerng[1,2], Jae Hong Lee[1,2], Euijoon Yoon[4], Seung-Hyun Chun[1,2,*]

1 Graphene Research Institute, Sejong University, Seoul 143-747, Korea

2 Department of Physics, Sejong University, Seoul 143-747, Korea

[3] Department of Nano Science and Technology, Graduate School of Convergence Science and Technology, Seoul National University, Suwon 443-270, Korea

[4] Department of Materials Science and Engineering, Seoul National University, Seoul 151-744, Korea

†Electronic supplementary information (ESI) is available: effect of growth time, methane flow, and plasma power on synthesized graphene.

* Author to whom correspondence should be addressed. Electronic mail: schun@sejong.ac.kr.

ABSTRACT

We demonstrate one-step fabrication of patterned graphene on SiO_2 substrates through a process free from catalysts, transfer, and lithography. By simply placing a shadow mask during the plasma enhanced chemical vapor deposition (PECVD) of graphene, an arbitrary shape of graphene can be obtained on SiO_2 substrate. The formation of graphene underneath the shadow mask was effectively forbidden by low-temperature, catalyst-free process. The growth conditions were optimized to form polycrystalline graphene on SiO_2 substrates and the crystalline structure was characterized by Raman spectroscopy and transmission electron microscopy (TEM). Patterned graphene on SiO_2 functions as a field-effect device by itself. Our method is compatible with present device processing techniques and should be highly desirable for the proliferation of graphene applications.

KEYWORDS: Graphene, catalyst-free synthesis, PECVD, low temperature, SiO_2

I. INTRODUCTION

Graphene is one of the most promising materials for applications in next-generation electronic devices because of its unique properties, such as high carrier mobility, high transmittance and excellent mechanical flexibility.[1] Large-area graphene, synthesized on metal surface by chemical vapor deposition (CVD), has spurred its applications in such devices.[2] However, the use of a metallic catalyst underneath the graphene layer inevitably requires a transfer process,[3-5] which is not compatible with standard processes in the semiconductor industry. Furthermore, multiple process steps, including coating with organic materials for catalyst etching and transfer, photo/e-beam lithography, and wet/dry etching, complicate the application of graphene to electronic devices. These processes are time consuming and, more importantly, cause degradation of graphene due to mechanical damage and chemical contamination which bring unwanted disorders to the devices. To achieve transfer-free synthesis of graphene, there have been attempts to grow graphene films at the interface between Cu[6] or Ni[7, 8] and the underlying dielectrics either by diffusing carbon atoms through the grain boundaries, or by using a self-assembled monolayer of carbon materials squeezed between a catalytic metal and a substrate[9]. However these methods still require catalytic metals that must be etched away. Therefore, it is desirable to pursue alternative fabrication method for graphene devices.

So far, the metal-catalyst-free synthesis of graphene has been tried by thermal CVD (or molecular beam epitaxy) on sapphire,[10-12] quartz,[11, 13] SiO_2,[13-16] MgO,[17-20] GaN,[21] ZrO_2,[18] Si_3N_4,[22] and HfO_2,[23] which result in graphitic carbon or nanocrystalline graphene. Recently, relatively high quality graphene films were synthesized by thermal CVD at atmospheric pressure[24-26], showing the possibility of catalyst-free graphene growth.

However, with these high growth temperatures (1100 ~ 1600 ºC) it is not possible to utilize the benefits of direct growth, *i.e.*, integration with existing technologies.

In this article, we demonstrate direct formation of patterned graphene on SiO_2 substrates without using catalysts or lithography. A pre-defined metal shadow mask is used as the pattern template in PECVD graphene growth. This process is transfer-free, catalyst-free, lithography-free, all dry, simple to implement, and scalable for batch production. This method also allows us to prepare multiple samples with different shapes in a matter of hours. The patterned graphene was characterized by Raman spectroscopy, TEM, and atomic force microscopy (AFM) to investigate its crystallinity and nanoscale morphology. The results were fed back to modify the growth conditions for improved graphene quality. Hall-bar patterned graphene, fabricated instantly on SiO_2, is investigated to assess the electrical properties of the graphene sheets with respect to the applied gate voltages and demonstrates the simplicity of our method.

II. EXPERIMENTAL PROCEDURES

Growth

The substrate used in this study is SiO_2(300 nm)/n-Si wafer purchased from Dasom RMS. As schematically illustrated in Figure 1a, a shadow mask made of stainless steel is placed on top of the substrate and the growth of graphene is done by flowing mixing gas of methane and hydrogen in a PECVD system. Prior to the graphene growth, O_2 gas was introduced into the chamber at a flow rate of 40 standard cubic centimeters per minute (sccm) and discharged at an RF power of 50 W for 3 minutes to remove any organic materials contaminating the surface. During the graphene growth stage, RF plasma was

generated under a continuous flow of hydrogen (H_2, 20 sccm) and methane (CH_4, 2 sccm), while the pressure was kept at 10 mTorr. The resolutions of mass flow controllers are 1 sccm for hydrogen and 0.1 sccm for methane, respectively. The growth temperature was varied from 500 to 900 ºC. Subsequently, the sample was cooled down rapidly to room temperature at a cooling rate of 3 °C/s by turning off the heating power.

Characterization

Raman spectroscopy (Renishaw, inVia) with an excitation wavelength of 514.5 nm was used to measure the crystallinity of graphene films. Surface morphology of the samples was evaluated by a commercial AFM (PSIA, XEI100). Scanning electron microscope (SEM) images were taken by a Tescan VEGA-3 system. High-resolution transmission electron microscopy (HR-TEM, JEOL JEM-2100F) was used to investigate the microstructure of graphene (operating at 200 kV). Electrical properties were measured by using standard four-probe method.

III. RESULTS AND DISCUSSION

Patterned few-layer graphene is obtained in one-go process by placing a shadow mask on the substrate during the graphene growth. Optical and SEM images of directly grown graphene on a SiO_2 substrate are presented in Figure 1b and 1c, respectively. Raman map of G band in Figure 1d indicates that the graphene growth is forbidden underneath the masked area. This is the salient feature of direct graphene growth without catalysts. In the typical CVD growth on metals, patterned graphene has been formed in two ways. One is by photo/e-beam lithography after a series of graphene growth, catalyst etching, and transfer processes. The other is by stamped-transfer after the growth on

lithographically-defined metal pattern.[27] Some variants of transfer-free synthesis[6, 7] still need patterns defined by lithography and the catalyst etching process. In contrast, our method for graphene pattern does not require any chemicals which are detrimental to graphene.

To investigate the growth mechanism in detail, a time-dependent growth study was performed. Figure 2a–c shows AFM images of the as-grown graphene with different growth durations. The line profile of graphene nucleated on the substrate (Figure 2a) illustrates that the step height of the graphene is about ~1.1 nm. Continued growth enlarges the size of graphene grains, and they coalesce into larger ones (Figure 2b). Finally, interconnected graphene networks are formed with thickness of ~1.5 nm (Figure 2c). In Raman spectroscopy, due to increased thickness and interaction between the layers, the ratio of 2D/G peak intensity decreased a bit with longer growth duration (Figure S1).[28] To investigate the microstructures, polycrystalline graphene films are transferred onto a TEM grid by etching the substrate. High-resolution TEM images in Figure 2d–e and selected-area electron diffraction (SAED) pattern in Figure 2f clearly show that layered and hexagonal crystalline structures of graphene films are synthesized on SiO_2 substrates.

The one-step fabricated graphene pattern on SiO_2 can be immediately used as field-effect devices. The upper inset of Figure 3 shows an optical image of Hall-bar patterned graphene on a SiO_2 substrate, prepared by simply placing a shadow mask during the growth. The channel width and the length of Hall-bar structure are well-defined as 100 μm and 300 μm, respectively (lower inset of Figure 3). The sheet resistance and corresponding optical transmittance of graphene is obtained as 1.4 kΩ/square and ~75 %,

respectively (a double-sided polished sapphire substrate was used as a reference for optical transmittance measurement). Since the graphene is already on SiO_2/Si, we can tune the electrical characteristics via a gate voltage (V_{gate}) applied to the bottom of the substrate. As shown in Figure 3, a change of curvature near V_{gate} = 100 V is noticed, which implies a possible ambipolar behavior of the film. At zero-bias, the hole density and the mobility are obtained as 1.3×10^{13} cm^{-2} and 105 cm^2/Vs, respectively. Although the mobility is still lower than that of graphene grown on a metal catalyst (~4,000 cm^2/Vs)[29] and on SiO_2 at 1100 °C (470–530 cm^2/Vs)[25], the value is much higher than those obtained from chemically reduced graphene oxide films (~1 cm^2/Vs)[30] and catalyst-free nanocrystalline graphene (1–40 cm^2/Vs).[12, 14]

Now that we have shown the merits of direct growth of patterned graphene, it is necessary to improve the graphene quality by optimizing the growth conditions. First, we investigated the temperature dependence of graphene synthesis on SiO_2 substrates. Figure 4a shows Raman spectra of graphene films grown without catalysts at various temperatures ranging from 500 to 900 ºC. When the temperature is higher than 600 ºC, the growth results in nanographene, which has been typically seen in other studies,[13, 15, 16, 22, 26, 31] as evidenced by the presence of D peak at ~1350 cm^{-1}, G at ~1580 cm^{-1}, D′ at ~1620 cm^{-1} and relatively smaller 2D at ~2680 cm^{-1}. On the other hand, when the growth temperature is lower than 600 ºC, there is a drastic enhancement of 2D peak intensity as the growth temperature decreases (Figure 4a, b). At 500 ºC, the intensity of 2D peak is much larger than that of G peak, indicating the transition of nanographene to polycrystalline graphene.[32, 33] The corresponding decrease of D peak intensity is another proof of improved graphene quality. The improved graphene quality at the lower growth

temperature is not consistent with what we have observed in typical CVD graphene grown on metallic catalysts, where the better graphene films are obtained at the higher growth temperatures. We note that the growth rate of graphene depends strongly on the growth temperature (Figure 4c). The fast growth rates at high temperatures may cause the nucleation sites to increase too fast and lead to three-dimensional growth rather than layer-by-layer growth. As a control, we reduced the flow of methane from 2 to 1 sccm at a growth temperature of 600 ºC. Surprisingly, in these conditions the Raman spectra show a significant enhancement of 2D peak intensity and a reduction of D peak intensity (Figure S2), implying that the growth rate of graphene could be the critical parameter for determining the quality of synthesized graphene on catalyst-free SiO_2 substrates. Interestingly our growth rate at 500 ºC is similar to that of direct thermal CVD growth at 1100 ºC[25]. Although all the growth parameters are totally different to ours, the results are similar to ours. This observation implies that the growth rate is an important factor for the synthesis of high-quality graphene directly on SiO_2. The AFM images (insets of Figure 4c) show that the surface of graphene synthesized at 800 and 900 ºC are very rough with average roughness about 2.5 and 3.2 nm, respectively. In contrast, relatively flat surface morphologies are observed at the low growth temperature of 500 and 600 ºC with average roughness about 0.25 and 0.20 nm, respectively. These observations imply that the growth rate is an important factor for the synthesis of graphene directly on SiO_2. When the temperature is lower than 500 ºC, the growth is so slow that a continuous layer of graphene is not formed within the growth time.

The plasma power is also an important parameter that affects the direct graphene growth. Initially the crystallinity increases with higher plasma powers (Figure 5a, b).

However, when the plasma power is higher than 70 W, no graphene is synthesized. The ICP reactor is known to offer high ionization efficiency compared to DC or RF capacitive discharges.[34] In our system, more than 40% of incoming methane is dissociated into various species, such as CH_x, C_2H_y, H, H_2, etc., at plasma powers of 50 W (Fig. S3a). The dissociation rate of methane can be tuned by plasma power, affecting the initial stage of graphene growth. High amount of carbon-containing radicals (CH_x, C_2H_y) increase the growth rate of graphene, but high amount of hydrogen species (H, H_2) decrease the growth rate by etching the carbon atoms.[35, 36] Fig. S3b–e show AFM images of graphene grains synthesized for 3 hours at 500 °C under different plasma powers. The sizes of the graphene grains are relatively smaller at lower (<10 W) and higher (>70 W) plasma powers, which can be attributed to the reduced supply of carbon-containing radicals and the etching effect of carbon atoms by hydrogen species, respectively. However, the growth becomes faster at optimal plasma powers (30–50 W) due to the increased supply of carbon-containing radicals and the weakened etching effect. These observations show the importance of fine tuning the growth parameters in catalyst-free PECVD and further growth optimization by the control of unexplored growth parameters, such as the partial pressure and flow of hydrocarbon, may lead to smaller defect density and higher crystallinity. Lowering the growth temperature even below 500 ºC is another direction so that direct graphene growth on flexible organic substrates is possible.

IV. CONCLUSION

In summary, we have demonstrated a transfer-free, catalyst-free, and lithography-free method to define graphene patterns on SiO_2/Si substrates by simply placing a shadow

mask during the growth. Since the underlying doped Si substrate functions as a back gate, the patterned graphene on SiO_2 can be directly used as field-effect devices. Our results suggest that graphene patterns can be incorporated into desired substrates by a single process. Therefore, in a variety of graphene applications, this method can replace the complex fabrication processes of graphene growth on metal catalysts, catalyst-etching, transfer to the substrate, and lithography. Relatively low mobility of our graphene indicates that further studies are required to improve the crystalline quality of synthesized graphene, which could be achieved by further growth optimization. We believe that our one-step method shows a promise for broad applications of graphene.

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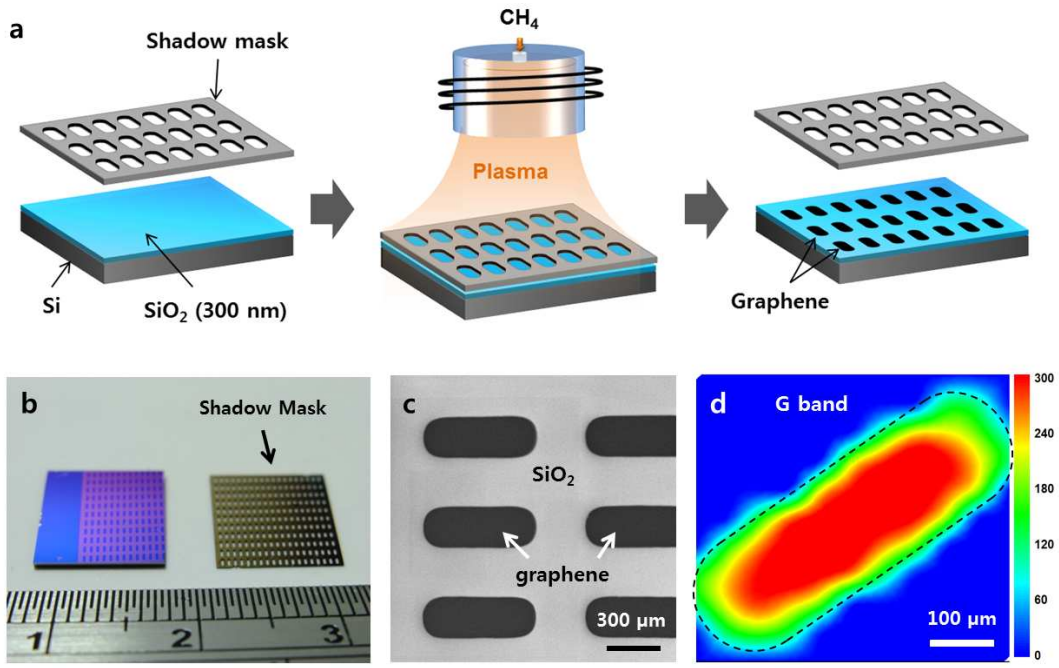

Figure 1. (a) Schematic diagram of one-step fabrication method to obtain patterned graphene on dielectric substrates without additional transfer or lithography process. (b) Photograph showing the shadow mask and the graphene on SiO_2 after the growth. The mask was made of 150 um-thick stainless steel. (c) SEM image and (d) Raman map of the graphene pattern.

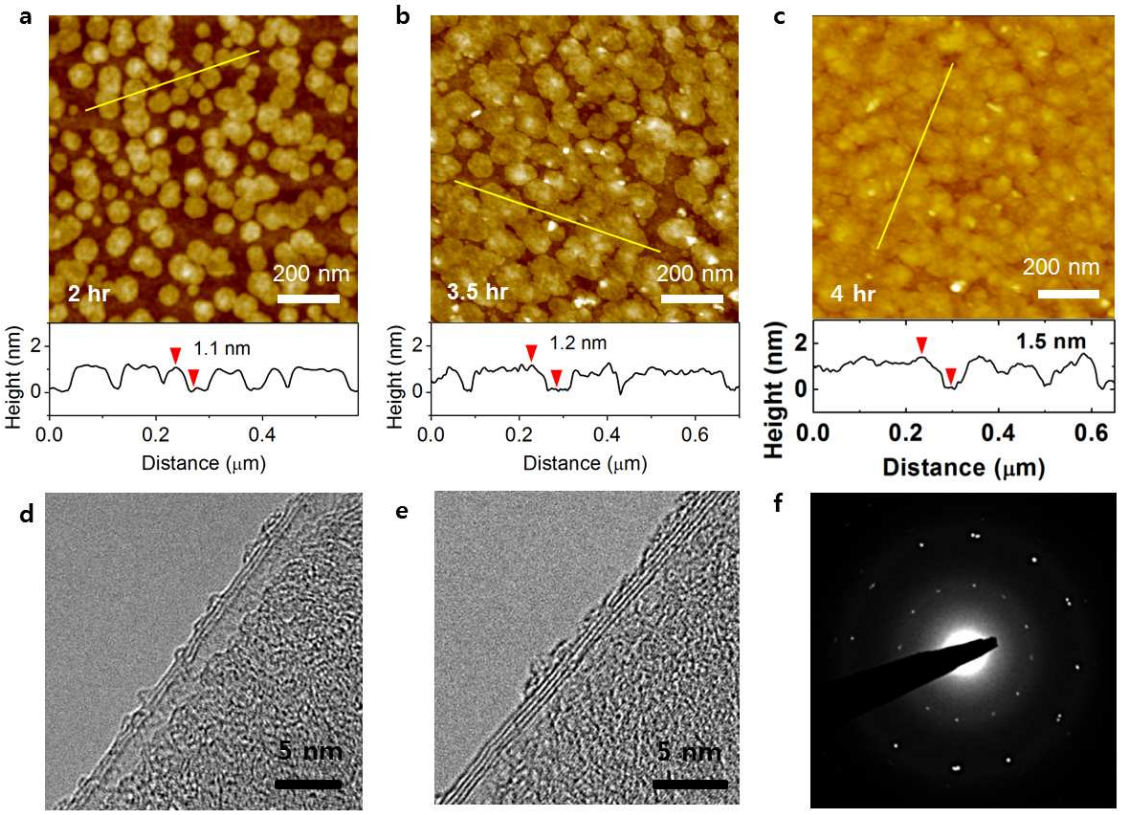

Figure 2. AFM height topography and height profile of graphene synthesized for (a) 2, (b) 3.5 and (c) 4 hours at 500 °C under plasma power of 50 W. (d), (e) HRTEM images of graphene edges on a TEM grid. (f) SAED pattern of graphene, showing hexagonal patterns.

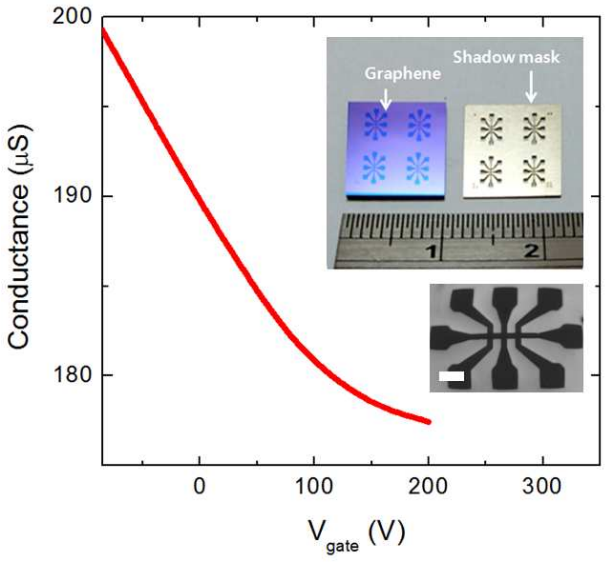

Figure 3. Back-gate voltage dependence of sheet conductance. At zero-bias, the hole density and the mobility are 1.3×10^{13} cm^{-2} and 105 cm^2/Vs, respectively. Upper inset shows photograph of shadow mask and patterned graphene on SiO_2 after the growth. Lower inset is a SEM image of the Hall-bar patterned graphene on SiO_2 defined by shadow mask. Scale bar = 500 μm.

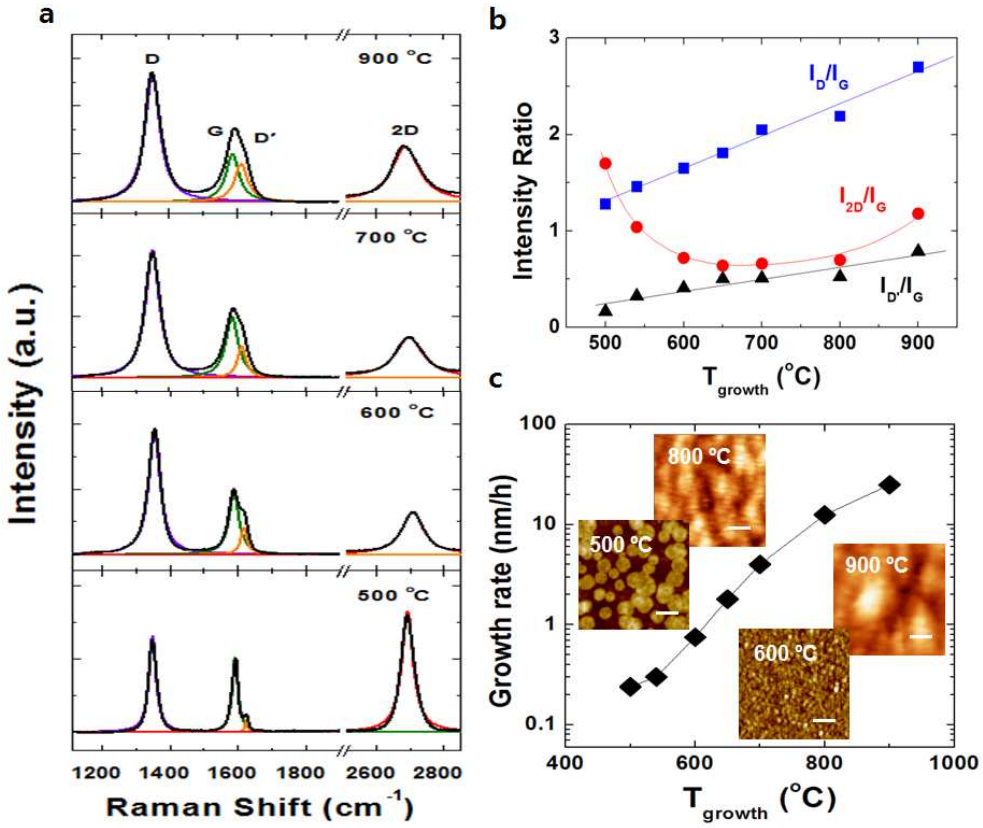

Figure 4. (a) Raman spectra (514 nm laser wavelength), (b) intensity ratios of D, D' and 2D peaks to the G peak of graphene films grown for 2 hours at various temperatures. (c) Temperature dependence of growth rate. Insets shows AFM image of synthesized graphene at various temperature. Scale bar = 100 nm.

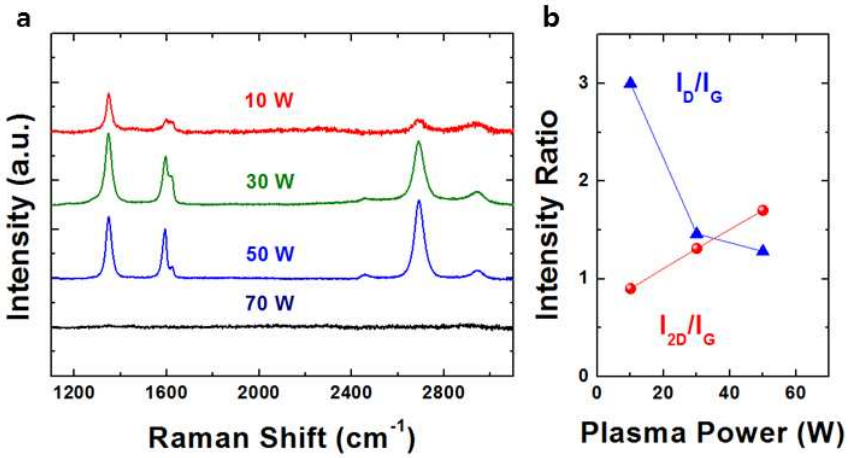

Figure 5. (a) Raman spectra and (b) intensity ratios of D and 2D peaks to the G peak of graphene films grown at 500 °C for 3 hours with different plasma power.

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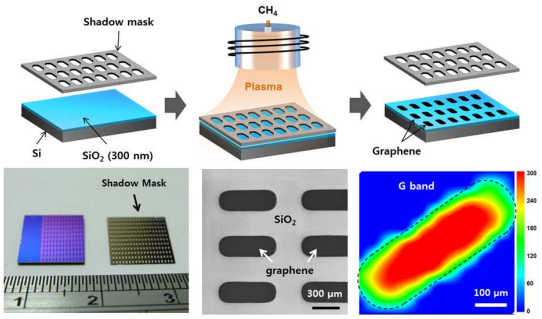

Patterned graphene is obtained on SiO_2 substrates without catalyst and lithography by simply placing a shadow mask during the growth process.