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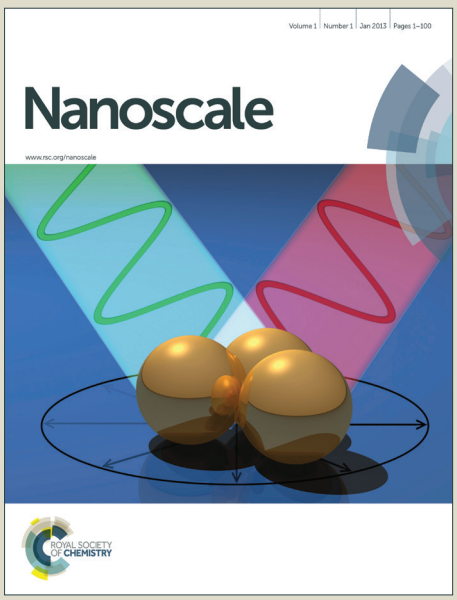

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ARTICLE

Asymmetrically-Gated Graphene Self-Switching Diodes as Negative Differential Resistance Devices

Cite this: DOI: 10.1039/x0xx00000x

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Received 00th January 2014,
Accepted 00th January 2014

DOI: 10.1039/x0xx00000x

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We present an asymmetrically-gated Graphene Self-Switching Diode (G-SSD) as a new negative differential resistance (NDR) device, and study its transport properties using Nonequilibrium Green's Function (NEGF) formalism and the Extended Huckel (EH) method. The device exhibits a new NDR mechanism, in which the very small quantum tunnelling current is used to control a much-larger channel conduction current, resulting in a very pronounced NDR effect. This NDR effect occurs at low bias voltages, below 1V, and results in a very high current peak in the μA range and a high peak-to-valley current ratio (PVCR) of 40. The device has an atomically-thin structure with sub-10 nm dimensions, and does not require any doping or external gating. These results suggest a potential for the device in applications such as high frequency oscillators, memory devices, and fast switches.

Introduction

Negative differential resistance[1] (NDR) devices exhibit interesting current-voltage (I-V) characteristics that result in a non-ohmic N-shaped I-V curve. This effect enables a number of very important applications, such as high-frequency oscillators[2-5], memory devices[6-8], multi-level logic[9-11] and fast switches[11, 12], and hence many efforts have been directed towards discovering transport mechanisms that lead to it.

The most common transport mechanism that gives rise to an NDR effect is quantum tunneling, which is present in resonant tunneling diodes (RTDs)[13] and transistors[14]. Quantum tunneling can achieve high peak-to-valley current ratios (PVCR), but results in very low peak current densities (PCD) due to the small current that can be transported by it. A high PCD is of great importance, as it determines the amount of power that can be provided by an NDR device. Other efforts have investigated the use of molecular electronics[15-20] for the realization of an NDR effect, but have also faced the challenge of limited PCD values and the difficulty of integration with electronics. Recently, Graphene has become of interest for the realization of NDR devices[21-30] due to its unique electronic properties[31, 32] including its high breakdown current density[33].

A new NDR mechanism based on the ambipolar behavior of Graphene field-effect transistors (FETs) has been reported[34], but although such a transport mechanisms can offer an NDR effect with a high PCD value, the effect is not very pronounced and is not able to provide a high PVCR comparable to that achieved by means of quantum tunneling effects.

Here we present a new Graphene nanodevice that can achieve an NDR effect based on a new mechanism that utilizes the quantum tunneling effect in controlling a much larger conduction mechanism; conventional carrier transport through a channel. Based on this, our proposed nano-device is able to achieve a high peak current value in the μA range, while still achieving a high PVCR. The device is based on the Graphene Self-Switching Diode[35] (G-SSD) geometry, shown in Fig. 1, but enhances it by exploiting a unique property of armchair Graphene nanoribbons (aGNRs) related to their widths.

Armchair Graphene Nanoribbons are generally semiconducting, with varying bandgaps depending on their width[36]. At certain widths, this band gap becomes vanishingly small making the aGNR almost metallic, and this occurs at widths of $3p$+2 carbon atoms, where p is an integer. Using this property, an enhanced version of a G-SSD, named a Graphene Self-Switching Metal-Insulator-Semiconductor Field-Effect Diode (G-SS MISFED) was proposed[37], in which the side-gates that are usually semiconducting aGNRs (Fig. 1(A)), are metallic (Fig. 1(B)). This allowed stronger field-effect control over the channel's conductance, and achieved enhanced rectification. Here, we present a new NDR device that also exploits this unique property of aGNRs, but differs from a G-SS MISFED in the fact that it has asymmetrical aGNR side-gates with different

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widths; one is semiconducting, while the other is metallic (Figs. 1(C) and 1(D)). These asymmetrical side-gates are the reason for the presence of this new NDR mechanism within this device. This new NDR mechanism is investigated by studying the device's transport properties using Nonequilibrium Green's Function (NEGF) and the Extended Huckel (EH) method.

The next section describes the used calculation method, while the following section presents the results that show the presence of this NDR effect within the device and then discusses a physical understanding of the mechanism that leads to it and the experimental feasibility of realizing the devices. Finally the conclusions are summarised in the last section.

Calculation Method

Based on the previously proposed concept, an asymmetrically-gated G-SSD was constructed and is shown in Fig. 1(E). The metallic and semiconducting side gates in the device were aGNR with widths of 8 and 7 carbon atoms, respectively, while the semiconducting channel was an aGNR with a width of 4 carbon atoms. All dangling bonds at the edges were passivated with hydrogen. The device geometry was optimized and the coordinates were relaxed using the Brenner potential[38] until forces on individual atoms were smaller than 0.05 eV/Å^2. The optimized device geometry is shown in Fig. 1(E).

Transport calculations were conducted on the device based on the Extended Huckel (EH)[39] method and Non-Equilibrium Green's Function (NEGF) formalism[40] as implemented in Atomistic Tool Kit (ATK) software package[41].

The device structure was partitioned as three regions: semi-infinite left electrode (L), central scattering region (C), and semi-infinite right electrode (R). The mesh points in real space calculation were defined as uniformly spaced k points of 1x10x50, with 50 sample points along the transport direction, and 10 points along the width (induced electric field direction).

In the used tight-binding model the tight-binding Hamiltonian is parameterized using a two-center approximation, where the matrix elements are described in terms of overlaps between Slater orbitals on each site. The used weighting scheme of the orbital energies of the offsite Hamiltonian was according to Wolfsburg[42]. Further details about the calculation method can be found in the ATK manual[41]. The electronic transport properties were then calculated using NEGF. Coherent transport of electrons was assumed to occur between (L) and (R) with Fermi levels μ_L and μ_R through (C) according to Landauer formula[43]. The coherent current is given by:

$$I(V) = \frac{2e}{h}\int_{\mu_R}^{\mu_L} T(E,V)[f_0(E-\mu_L) - f_0(E-\mu_R)]dE \qquad (1)$$

where $T(E,V)$ is the transmission probability of incident electrons with energy E from (L) to (R), $f_0(E-\mu_{L(R)})$ is the Fermi-Dirac distribution function of electrons in (L) and (R) respectively, and $V = (\mu_R - \mu_L)/e$ is the potential difference between (L) and (R).

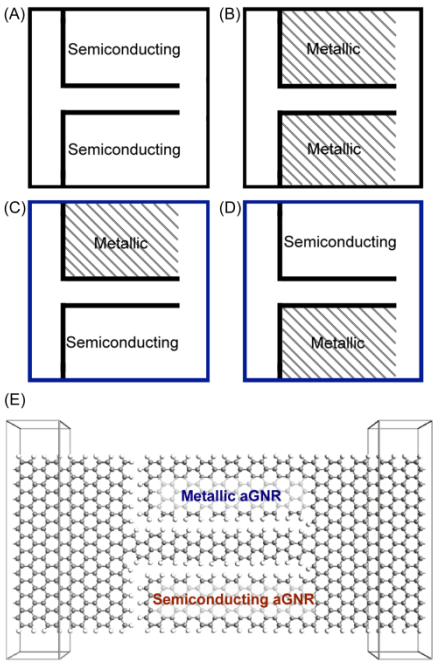

Fig. 1. An illustration of a Graphene Self-Switching Diode with (A) symmetrical semiconducting side-gates, (B) symmetrical metallic side-gates (MISFED), (C) and (D) asymmetrical side-gates (NDR Device). The shaded regions resemble metallic aGNRs, while the unshaded regions resemble semiconducting aGNRs. (E) The device structure of the simulated asymmetrically gated G-SSD after optimization, with labels to distinguish the metallic gate from the semiconducting gate.

The $T(E,V)$ is correlated with $\hat{G}^a(E)$ and $\hat{G}^r(E)$, the Green's function matrices reflected from (L) and (R) to (C) respectively, as:

$$T(E,V) = Tr\left[\mathrm{Im}\Sigma_L\left(E-\frac{eV}{2}\right)\hat{G}^r(E)\mathrm{Im}\Sigma_R\left(E+\frac{eV}{2}\right)\hat{G}^a(E)\right] \qquad (2)$$

where $\sum_{L(R)}$ are electrodes' self-energies describing coupling with (C).

In order to understand the variation of coherent electron transport through the system we need to express local current components at the atomic level along the chemical bonds. Local current components may be investigated by extracting local transmission components. The total transmission coefficient can be split into local bond contributions, T_{ij}, which are represented in ATK by lines along the bond lengths, called transmission pathways. The relationship between the total transmission coefficient and the local bond contributions can be described as:

$$T(E,V) = \sum_{i\in A, j\in B} T_{ij}(E,V) \qquad (3)$$

where A and B represent pairs of atoms separated by an imaginary surface perpendicular along the bond length. The total transmission coefficient is the sum of the local bond contributions between all pairs of atoms A and B. Further details can be found in Ref. 44[44].

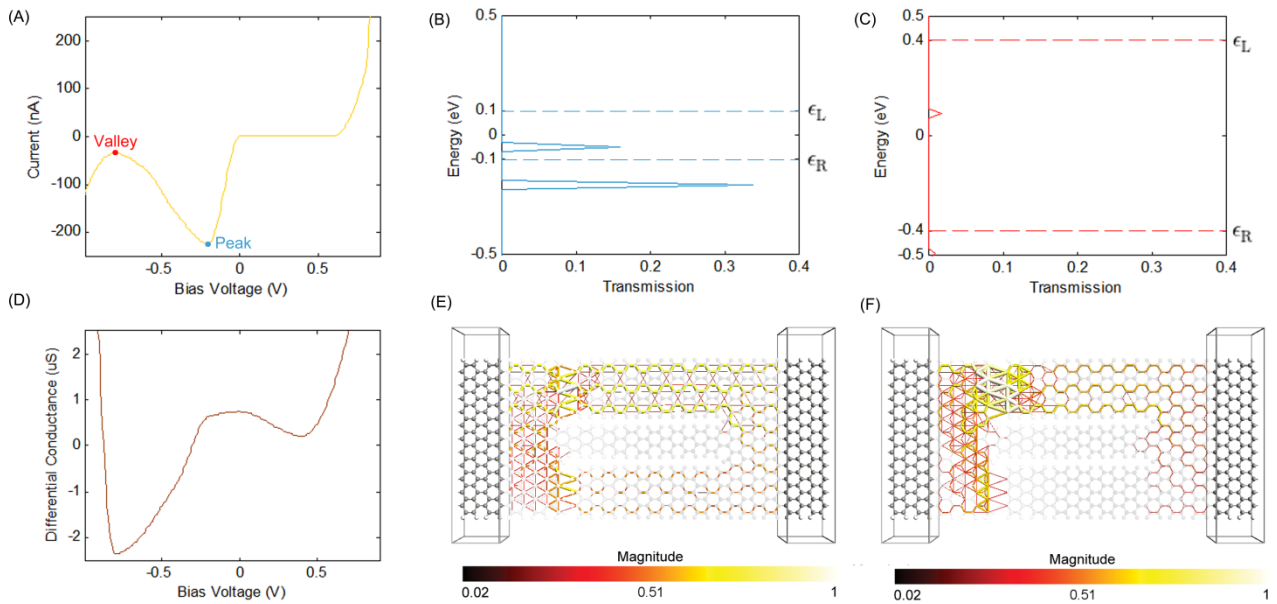

Fig. 2. (A) I-V Characteristics of the simulated asymmetrically-gated G-SSD of Fig. 1(E), (B) Transmission spectrum of the device at the peak (blue continuous line) and (C) the valley (red continuous line) of the reverse bias NDR region within the device's I-V curve (dotted lines show the bias window), (D) Differential conductance plotted against bias voltage for the device, (E) Transmission pathways plots for the device near the peak and (F) near the valley of the reverse bias NDR region (the central region of the device in both plots was drawn with 90% transparency in order to clarify the visualization of the transmission pathways).

Results and Discussions

Reverse Bias NDR Effect

Based on the above method, the I-V characteristics of the device were calculated and are shown in Fig. 2(A). As the figure suggests, the device exhibits a clear NDR effect in the reverse bias region. The NDR region shows a noticeable peak-to-valley transition that gives rise to the NDR effect, which results in the observed N-shaped curve. A plot of the differential conductance plotted against the bias voltage for the device is shown in Fig. 2(D), and further confirms the presence of this NDR region, where the differential conductance drops below zero.

Transmission spectrum plots for the device at the peak and the valley of the reverse bias NDR region are shown in Figs. 2(B) and 2(C) respectively. The two plots suggest that the decrease in current after the peak in the I-V curve may be attributed to the suppression of the transmission peak that lies within the bias window of the transmission spectrum plots.

In order to investigate the origins of the NDR effect, transmission pathways within the device were calculated, based on the previously mentioned methods. Transmission pathways within the device near the peak (-0.4 V) and near the valley (-0.6 V) of the reverse bias NDR region were calculated, and are plotted in Figs. 2(E) and 2(F) respectively.

At the peak, in Fig. 2(E), it is observed that there are no transmission pathways through the channel, as is expected from a G-SSD. This is because the negative voltage applied to the channel by the side gates depletes the channel from charge carriers and pinches off the channel. It is also shown that conduction occurs due to quantum tunneling current from the side gates to the left terminal of the device through the vertical insulating trenches. In a standard G-SSD it is desirable to eliminate this unwanted leakage current, while here it provides the mechanism for conduction at the peak of the NDR effect. It is noted that the transmission pathways in the metallic side-gate are larger than those in the semiconducting side-gate.

As the reverse bias voltage is increased, the transmission pathways through the semiconducting side gate disappear, preventing the flow of quantum tunneling current from it into the left terminal of the device, as shown in Fig. 2(F). This result suggests that the suppression of this tunneling current from the semiconducting side gate is the reason for the decrease in the current after the peak and the presence of the NDR effect. This may be explained by the fact that the increased negative voltage applied to the metallic side gate induces a greater electric field that does not only deplete the semiconducting channel from charge carriers, but further extends this effect to the semiconducting side gate, depleting it also from charge carriers, and hence preventing any conduction through it and suppressing the tunneling current component due to it.

Forward Bias NDR Effect

In order to verify the presence of this NDR effect in larger asymmetrically-gated G-SSDs, a larger device structure was constructed and relaxed according to the previously mentioned optimization method, until forces on individual atoms were smaller than 0.5 eV/Å^2. The optimized device structure is shown in Fig. 3(A).

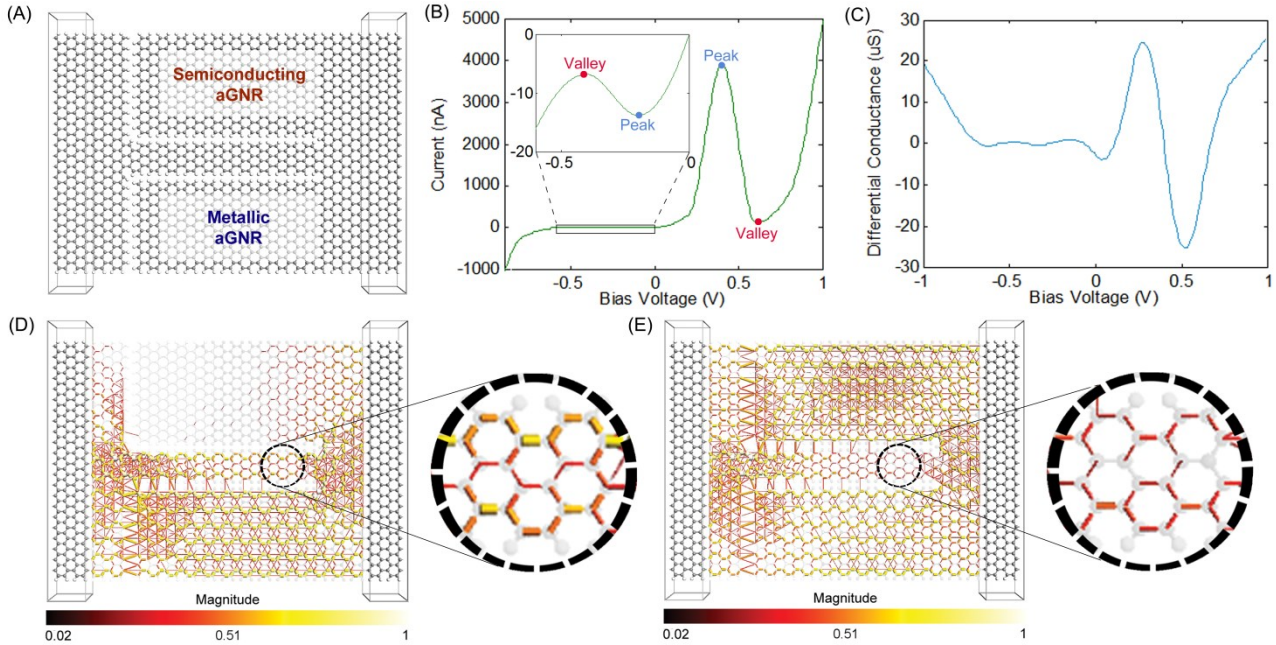

Fig. 3. (A) The device structure of the larger simulated asymmetrically-gated G-SSD after optimization, with labels to distinguish the metallic side-gate from the semiconducting side-gate, (B) I-V Characteristics of the device, (C) Differential conductance plotted against bias voltage for the device, (D) Transmission pathways plots for the device at the peak and (E) the valley of the forward bias NDR region of the device's I-V curve (the central region of the device in both plots was drawn with 90% transparency in order to clarify the visualization of the transmission pathways). (D) and (E) include an zoomed-in portion of the channel in order to highlight the suppression of the transmission pathways in it from the peak to the valley point.

The device has a semiconducting aGNR channel with a width of 6 carbon atoms. The semiconducting side gate is an aGNR with a width of 19 carbon atoms, while the metallic side gate is an aGNR with a width of 17 carbon atoms. Transport calculations based on the previously mentioned methods were conducted on the device structure to obtain its I-V characteristics and its differential conductance plot, and these are shown in Figs. 3(B) and 3(C) respectively.

The I-V curve of the larger device, shown in Fig. 3(B), looks qualitatively different than that of the smaller device in Fig. 2(A). A forward bias NDR effect occurs and is greatly enhanced, to the extent that the reverse bias NDR effect seems to be negligible compared to it. A closer look at the reverse bias region, shown in the inset of Fig. 3(B), confirms the presence of the reverse bias NDR effect, but here the peak current value is at least 2 orders of magnitude smaller than that of the forward bias NDR effect. This suggests that the NDR mechanism in forward bias is driven by a different transport mechanism.

In order to understand the origins of this new transport mechanism that gives rise to the enhanced forward bias NDR effect, the transmission pathways for the device at the peak and at the valley of this forward bias NDR region were calculated using the previously mentioned methods, and are plotted in Figs. 3(D) and 3(E) respectively.

At the peak, Fig. 3 (D) suggests that tunneling current tunnels from the metallic side-gate and not from the semiconducting side-gate, however, the channel shows continuous transmission pathways lines, some with values close to unity (illustrated by the yellowish color of the lines), suggesting that the channel is open and is strongly conducting, unlike the reverse bias case. The channel here is wider than that of the smaller device and hence it is expected that it will have a smaller threshold turn-on voltage. This conduction through the channel would dominate the total current, as tunneling current is much smaller than conduction current, and hence explains the very high peak current value of 4 μA at a very small bias voltage of only 0.4 V, which cannot be due to tunneling current only. On the other hand, after the bias voltage is increased to 0.6 V reaching the valley point, Fig. 3(E) suggests that the semiconducting side gate starts to tunnel current. However, this does not explain the sudden drop in current down to 100 nA (2.5 % of the peak).

A closer look at the figure shows that when both side gates tunnel simultaneously, the transmission pathways through the channel is significantly suppressed, especially towards the right end close to the right electrode (as highlighted by the zoomed-in portions of Figs. 3(D) and 3(E)), suggesting that the channel conduction current, which dominates the total current, might have been greatly suppressed. This explains the reason for the sudden drop in current flow through the device, which gives rise to the pronounced positive bias NDR effect. The peak-to-valley current ratio (PVCR) achieved by this new NDR mechanism reaches a high value of 40.

New NDR Mechanism

In order to understand this new NDR mechanism, which occurs in forward bias, a discussion of the operation principle of the device under forward bias is presented, and is clarified through the illustrations in Fig. 4.

With no applied bias across the device, the semiconducting channel would have natural depletion regions at the edges of the insulating trenches due to repulsion between electrons on either side of the trench[45]. In SSDs these depletion regions are generally small, but since the channel in our device is narrow, it is expected that these depletion regions would have the channel completely pinched-off[45, 46], even with no bias voltage applied, as illustrated in Fig. 4(A). However, when a positive bias is applied across the device, it is expected that positive charges would start to accumulate at the edges of the insulating trenches inside the side-gates. However, since the metallic gate does not have any depletion regions within it, positive charges are able to tunnel through the insulating trenches from it earlier than from the semiconducting side gate, which does have depletion regions extending in it. This tunneling current from the metallic side-gate provides a discharge path for holes in it, and hence holes do not accumulate, contrary to the semiconducting side-gate case, where positive charges begin to accumulate near the trench. These positive charges attract electrons on the other side inside the channel, and hence narrow the depletion regions, eventually opening up the channel. This effect is illustrated in Fig. 4(B). This explains what happens at the positive bias NDR peak, where the channel is open due to the accumulation of positive charges within the semiconducting side-gate, and hence conduction occurs through this open channel, resulting in a large current in the μA range.

As the bias voltage is further increased, the bias voltage becomes high enough for the holes accumulated in the semiconducting side-gate to also begin tunneling across the vertical insulating trench and into the left terminal of the device, providing a discharge path for the accumulated positive charges inside the semiconducting side gate. This discharge allows the channel to return back towards its depleted state, as illustrated in Fig. 4(C). As the channel is depleted, the current flow through it is suppressed, and this causes the drop in the overall current through the device during the NDR region (the region between the peak and the valley).

Increasing the bias voltage further, increases the tunneling current from the semiconducting side-gate, discharging more of the accumulated positive charges at the trenches, and allowing the channel to become more depleted, until it is completely pinched-off again, as illustrated in Fig. 4(D). At this point the current through the device reaches the valley point. Any further increase in bias voltage afterwards results in an increase in the overall current through the device because it would be dominated by tunneling current through the insulating trenches.

In order for this NDR effect to take place, the threshold voltage of the device (the voltage at which the channel opens up and starts to conduct) should be less than the onset voltage of tunneling current from the semiconducting side-gate. This explains why this enhanced forward bias effect was not observed for the device of Fig. 1(E), which had a narrow channel and hence a high threshold voltage, but was observed for the device of Fig. 3(A), which had a wider channel and hence a lower threshold voltage.

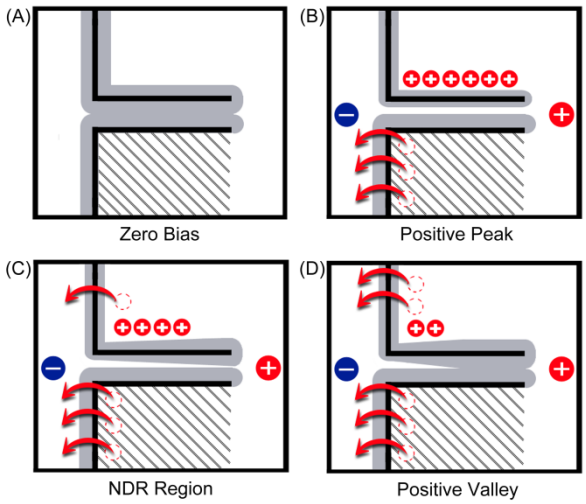

Fig. 4. Schematic illustrations of the new NDR mechanism in asymmetrically-gated G-SSDs, illustrating how the asymmetrical tunneling mechanism affects the opening and closure of the channel. The sub-figures in increasing positive bias voltage order show the device (A) with no bias voltage applied, (B) at the peak current point, (C) in the region between the peak and the valley current points (the NDR region) and (D) at the valley current point. In all sub-figures, the shaded side-gate resembles the metallic side-gate.

Experimental Feasibility

Asymmetrically-gated G-SSDs require the concurrent realization of semiconducting and metallic GNRs in order to achieve asymmetrical gating. This can be achieved through tuning the bandgap of the GNRs by varying their widths. At the atomistic scale, GNRs need to have smooth edges to achieve precise control and effective tuning of their bandgap. This has proven to be a challenging task. However, recent work has shown promising results towards achieving this goal[47-53] where the experimental fabrication of Graphene Nanoribbons (GNRs) with smooth edges has been reported[49-51]. Other methods, using Helium Ion Beam lithography[54-56] and single-atom catalyst chiselling[52], are also promising candidates for the fabrication of GNRs with smooth edges.

In addition to the methods described above, a photo lithographic method, more conducive to mass fabrication, is also possible. This approach is based on the fact that photo lithographically etched GNRs are always semiconducting when made narrower than 20 nm in width, due to their edge roughness, and are always semi-metallic when made wider than 50 nm in width[36, 57]. Based on this concept, Asymmetrically-gated G-SSDs can be realized without the need for GNRs with perfect edges, given that the semiconducting channel and side-gate are lithographically defined narrower than 20 nm, while the metallic side gate is lithographically defined and wider than 50 nm.

Conclusions

In summary, we presented a new type of Graphene nanodevice, based on an asymmetrically-gated self-switching diode geometry, which achieves an NDR effect based on a new

mechanism that allows very high peak current values, while still achieving a significant peak-to-valley current ratio. The calculated I-V characteristics of the device suggested the presence of two NDR effects, one in reverse bias and the other in forward bias, and the origins of these two effects were investigated using transmission pathways mapping within the device. It was found that the reverse bias NDR effect is due to asymmetrical tunneling from the asymmetrical side-gates, while the forward bias NDR effect arises due to a different mechanism. In this mechanism, the asymmetrical tunneling current from the side-gates is used to control a much larger conduction current through the channel, resulting in a much more pronounced effect with a peak current value two orders of magnitude higher than that attributed to tunneling current only. The results show a calculated peak-to-valley current ratio (PVCR) of 40 for an atomically-thin device that can be realized within a single aGNR and with sub-10 nm dimensions.

Acknowledgements

Feras Al-Dirini would like to thank Dana Hirzalla for helping in the production of figures and would like to thank the NICTA Optics and Nanoelectronics (ONE) research group members for their valuable feedback and discussions.

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