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A Facile Room Temperature Iodination Route to in-situ Fabrication of Patterned Copper-Iodide/Silicon Quasi-Bulk-Heterojunction Thin Films for Photovoltaic Application

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Fabrication of a monocrystalline silicon based heterojunction film at room-temperature in a time-efficient manner is desirable for energy and environmental considerations. In this report, a gas-solid phase direct elemental reaction (DER) route to realize this aim by firstly depositing an elemental copper layer on monocrystalline silicon surface followed by a reaction with iodine vapor is described. The samples were characterized by X-ray diffraction (XRD), scanning electron microscopy (SEM), transmission electron microscopy (TEM), raman spectroscopy, photoelectrochemical measurements, and transient photovltage (TPV) technique. The novelty of the current work lies in the following three aspects: (1) Formation of in-situ CuI/Si quasi-bulk-heterojunction at room temperature is assisted by the infiltrated elemental copper layer being completely transformed into γ phase Copper Iodide (γ-CuI) thin film; (2) The virgin monocrystalline silicon is pretreated to ensure a pyramidally patterned rough surface which facilitates the construction of quasi-bulk-heterojunction thin films and enhances their chemical stability and mechanical stability; (3) The photovoltaic performance and mechanism of the resulting CuI/Si quasi-bulk-heterojunction based solar cell was detected and evaluated for the first time by combination of photoelectrochemical and TPV techniques, which demonstrates that the intensity of the interface electric field as well as the open circuit potential can be adjusted by tuning the amount of CuI coated on the pyramidally patterned n-Si substrate.

1. Introduction

The traditional monocrystalline silicon based solar cells which are characterized by both comprehensive stability and high photoelectric conversion efficiency have been facing challenges from other alternative solar energy conversion materials.[1] One of the important reasons is that the fabrication of p-n junctions requires high temperatures.[2-5] To overcome this high temperature restriction, construction of inorganic/Si compound heterojunctions is an alternative way to build solar cells with relatively low temperature requirements. For example, a solar cell device based on the n-ZnO/p-Si heterojunction has been reported with three dimensional structure, in which ZnO nanowires are uniformly distributed on the surface of Si nanowires.[6] This device exhibited good optical performance and photovoltaic performance. Yet, the preparation of the p-n junction still necessitated the relatively higher temperature of 500 ° C as well as argon protection. In addition, other heterojunction solar cells based on Si/compound semiconductor have been extensively studied, such as CdS/Si,[7,8] which resulted to an efficient charge separation in heterojunction structures due to the well aligned band structure.

Considering that the organic polymer semiconductor materials can be assembled to form p-n junctions at lower temperatures, Avasthi and colleagues[9] recently prepared a novel p-P3HT/n-Si heterojunction by spin-coating the p-type conjugated P3HT on Si surface at room temperature, which indeed realized the low temperature fabrication of single crystal Si based p-n heterojunction. At the same time, the utilization of rigid Si substrate suppressed flexibility of the organic polymer semiconductor and rendered it impractical for solar cell use. In addition, the high cost, low charge transfer rate, and complex preparation process of the specialized organic polymer semiconductor material add to the inapplicability of this system. Thus the challenge remains to find a new route to form p-n junctions with single crystal Si that satisfies the following criteria: 1) the inorganic compound semiconductors and the p-n junction can be prepared at room temperature and 2) the corresponding energy level of the inorganic compound matches well with that of the single crystal silicon so that photo generated carriers can be efficiently separated and the performance of photovoltaic devices is expected to be enhanced.

Among various common p-type inorganic semiconductor materials, CuI is attracting more and more attention because it possesses good electrical conductivity and larger band gap.[10,11] Especially, CuI thin film is completely transparent in visible and near infrared region due to its larger band gap. The top of the valence band and the bottom of the conduction band for CuI are located at -5.2 eV and -2.2 eV, respectively, resulting in a bandgap of ~ 3.0 eV, which corresponds well with the energy level of monocrystalline silicon;[12] thus Si/CuI meets the parameters for forming a heterojunction for effective photovoltaic conversion.

Multiple preparation methods for CuI semiconductor thin films are available, including thermal evaporation,[13] hydrothermal method,[14,15] electrodeposition,[16] and photoelectrochemical copper nanoparticle deposition method[17]. For example, Akihito *et al.* prepared a CuI thin film with lamellar structure on silicon substrate by thermal evaporating 99.99% CuI powder at 600 °C and 1.0×10^{-3} Pa for solar cell devices fabrication. In our previous work[18], we have successfully fabricated highly (110) oriented CuI thin films with sharp exciton bands on copper foil substrates in the solvothermal condition of 160 °C. All these methods require harsh conditions such as high temperature, high pressure, high vacuum, or elaborate equipment set-up.

Fabrication of CuI/Si quasi-bulk-heterojunction film in an alternative and straightforward way at room-temperature is highly desirable. Here, we report the development of a facile gas-solid phase route to realize this aim by firstly depositing an elemental copper layer on monocrystalline silicon surface followed by iodination with iodine vapor at room temperature. The current iodination process is an alternative for preparing CuI thin films. The virgin monocrystalline silicon is pretreated to form a pyramidally patterned surface which enhances the chemical and mechanical stability of the ensuing bulk-heterojunction as the building frame for infiltrated elemental copper layer that then react in-situ with iodine to form CuI/Si heterojunction thin film. The elemental Cu thin film can also be deposited by some other methods such as electroplating or electroless copper plating at air condition. The result is the production of in-situ CuI/Si quasi-bulk-heterojunction at room temperature.

2. Experimental section

2.1 Silicon substrate pretreatment

N-type silicon wafer (1.0 cm×0.5 cm, thickness 170±5μm, 0.015~0.019Ω•cm^{-1}, (100)) was first cleaned with acetone and then deionized water (DI water) for about 1 min, and then treated with anhydrous ethanol in an ultrasonic bath for about 10 min, and stored in anhydrous ethanol. To obtain a textured surface on the pre-treated wafer, it was then corroded in an alkaline solution prepared by mixing 75 mL KOH solution (3.0% w/w ~ 4.0% w/w) and 10 mL isopropyl alcohol at 90 °C for approximately 40 min, and then treated with HF solution (volume ratio of 1:50) for 30 s. The resulting textured wafer was cleaned with DI water and dried at 70 °C for further use.

2.2 Heterojunction thin film preparation

First, 100 nm or 200 nm elemental Cu thin film was deposited on the n-type Si textured surface by magnetron sputtering with film thickness monitor (FTM); second, this sample was treated with iodine vapor at 15 ~ 25 °C for about 40 min until the Cu thin film converted to white CuI completely. Using this simple method, a CuI/Si heterojunction thin film with a large surface area was prepared. The CuI/Si heterojunction thin film surface was spin coated with PEDOT:PSS (poly(3,4-ethylene dioxythiophene):poly(styrene sulfonate)) at 1800 rmp to form the Si/CuI/PEDOT:PSS structure and dried in an oven at 70 °C. The resulting sample was stored in a clean and dry container keep away from light.

2.3 Solar cell device fabrication

A quasi-bulk-heterojunction solar cell device was fabricated on the basis of the Si/CuI/PEDOT:PSS structure. Both of the silicon and PEDOT:PSS surface was covered with silver as cathode and anode respectively by thermal evaporation method.

2.4 Characterization

The structure of the resulting thin films was characterized by Bruker D8 Advance X-ray diffractometer with nickel-filtered Cu-Kα radiation, 40 kV, 40 mA, and a scanning step of 0.02° per second. SEM images were recorded from a Zeiss EVO LS-15 scanning electron microscope. The raman spectrum was studied by a Renishaw Invia Reflex Micro-Raman Spectroscopy System with a 532 nm line laser as the excitation source. Photoelectrochemical measurements were carried out by CHI660E. As reported[19], a transient photovoltage (TPV) curve was recorded by a 500 MHz digital oscilloscope (TDS 3054C, Tektronix) and excited with a third-harmonic Nd:YAG laser (Quantel Brilliant Eazy: BRILEZ/IR-10). Photovoltaic performance of the final solar cell device was tested by a Newport solar simulator with 100 mW•cm^{-2} AM 1.5G irradiation, and the light intensity was calibrated by a standard silicon solar cell.

3. Results and Discussion

3.1 Preparation of pyramidally patterned monocrystalline silicon surface

In order to enhance the surface area of monocrystalline silicon wafer so as to construct quasi-bulk-heterojunction and improve the chemical stability and mechanical stability of the heterojunction films, we pretreated the virgin Si surface with a potassium hydroxide/isopropyl alcohol solution and dilute HF solution. At the same time, the pretreatment did not change the orientation of the Si crystalline structure, as both the virgin and pretreated Si surface had a highly oriented surface (400).

The corresponding SEM images in Figure 1 clearly show pyramidally patterned arrays of the pretreated silicon surface (treated in mixed solution with 3.0% w/w and 4.0% w/w KOH, respectively). Both of the two treatments resulted in a unique pyramidal structure with different pyramidal Si crystal size. We can clearly see that the Si surface treated with 4.0% w/w KOH resulted in larger Si pyramidal crystals but relatively sparse surface structure than that treated with 3.0% w/w KOH mixed solution. The difference in size and density of the pyramidal Si crystals is attributed to the effect of alkaline concentration on the anisotropic silicon. Higher corrosion intensity may produce pyramidally patterned Si with larger size and less density. The concentration of KOH mixed solution play a key role in constructing the patterned pyramidal Si structure. When the concentration of KOH mixed solution was less than 3.0% w/w, the preferred pyramidal structures could not be obtained, while higher concentrations may lead to a sparse surface structure.

We have found that 3.0% w/w KOH and an etching time of 40 minute are the optimal conditions for constructing the ideal pyramidal Si structure.

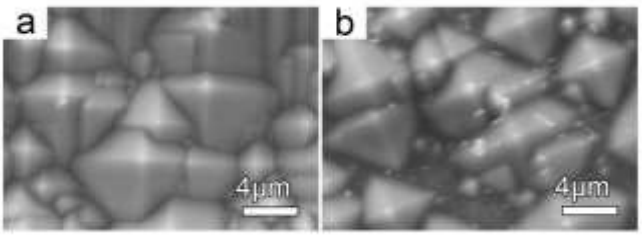

Figure 1. SEM images of the pretreated silicon substrates etched with 3.0% w/w KOH solution (a) and 4.0% w/w KOH solution (b). The corresponding XRD pattern of n-Si was illustrated in supporting information (Figure S1).

3.2 In-situ iodination to form CuI/Si quasi-bulk-heterojunction thin films at room temperature

Elemental Cu was deposited on the above pretreated rough surface of pyramidally patterned monocrystalline silicon, which facilitates and improves the contact of Si/Cu interfaces. Reaction of the above Cu deposition layers with iodine vapor at room temperature yields the γ-CuI nanopartcle layer in-situ. The corresponding XRD patterns of the CuI thin film transformed from 200 nm Cu (denoted as CuI/Si-200) is shown in Figure 2a. The diffraction peaks of (111), (200), (220), and (311) correspond to the literature values of CuI crystal face (PDF No. 75-831). The relatively sharp peaks suggest an expected high crystallinity in the CuI crystal. We can clearly see that the (111) face is predominant and there are no other noticeable peaks except those from Si substrate, indicating the high purity and preferential (111) growth of the obtained CuI crystal. For the 100 nm Cu transformed CuI sample (denoted as CuI/Si-100), there are no obvious changes in XRD except the relative decrease of CuI signal due to the thinner CuI film formation (Supporting information Figure S2). Figure 2b displays the Raman spectra of the CuI/Si-200 sample with a relatively strong transverse-optic (TO) and weak longitudinal-optic (LO) model of CuI. The TO model was recorded at about 123 cm^{-1}, which further confirmed that the in-situ synthesized crystal thin films are γ-CuI with high purity.[20]

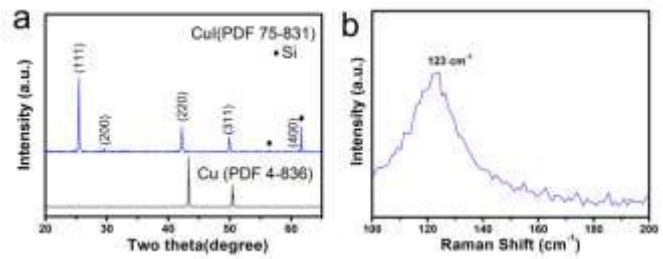

Figure 2. (a) XRD pattern and (b) Raman spectrum of the resulting CuI/Si sample. The standard Cu XRD pattern was illustrated as reference.

Figure 3 shows the corresponding SEM and TEM images of the resulting CuI/Si samples. Based on the current gas-solid phase direct elemental reaction (DER) strategy, pyramidally patterned CuI/Si heterojunction films with large area can be obtained. Figure 3a shows the SEM image of a uniform pyramidal CuI/Si-200 surface fully coated with CuI nanoparticles. The cross-section SEM image of the CuI/Si-200 sample, which exhibited a dense CuI layer with about 200 nm in thickness, nearly the size of an individual CuI crystal, is shown in Figure 3b. Figure 3c and 3d show the enlarged SEM surface morphologies of both CuI/Si-100 and CuI/Si-200 samples with uniformly coated CuI nano-particles on pyramidal Si crystal surface, which may provide a larger interface area for construction of CuI/Si quasi-bulk-heterojunction structure. The surface thickness and roughness of the CuI/Si bulk heterojunction films can be easily controlled by adjusting the thickness of the initial elemental copper layer in our strategy. A thicker copper layer may result in a relatively thicker and rougher pyramidal surface. The CuI particles were peeled off from Si wafer by ultrasonic treatment and the corresponding TEM image was shown in Figure 3e. From the HRTEM images (Figure 3f) we can see the well-resolved 2D lattice fringes of the CuI particle clearly. The lattice spacing of 0.348 nm and 0.301 nm corresponds to the (111) and (200) planes of the cubic γ-CuI, respectively. The lattice spacing demonstrates that our current gas-solid phase direct elemental reaction (DER) strategy can result in a well crystallized CuI thin film at room temperature.

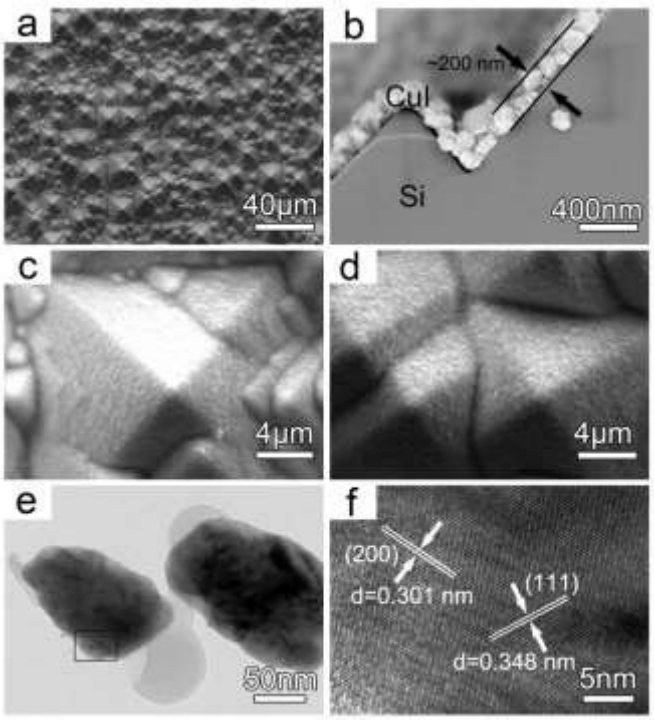

Figure 3. SEM images of CuI/Si-100 sample (a); cross-section SEM images of CuI/Si-100 sample (b); enlarged surface morphologies with various thickness of CuI/Si-100 and CuI/Si-200 samples (c, d); TEM images of individual CuI nanoparticles peeled off from the as-prepared CuI/Si-200 sample (e); HRTEM image recorded from the rectangle zone in the Figure 3e (f).

3.3 Diffuse reflection of different CuI/Si heterojunction films

The reflectance is an important parameter for photovoltaic applications because it reflects light absorption ability of the semiconductor films. The diffuse reflectance data of the CuI/Si samples with different CuI thickness was collected and the

corresponding reflectance curves were shown in Figure 4. Apparently, the corresponding average reflectance only increased slightly along with the increase of CuI film thickness, indicating that the CuI film thickness just slightly influence the light absorption in a reasonable thickness range. As comparison, the CuI/plane Si sample (without the pretreated pyramidal feature) was prepared and exhibited a significantly increased reflectance. This phenomenon definitely demonstrated the efficiently antireflective effect induced by the pretreated pyramidal Si surface.

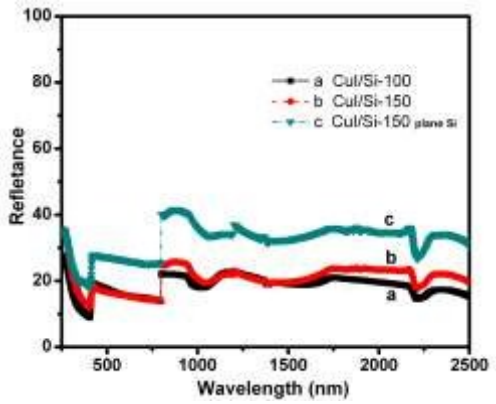

Figure 4. Diffuse reflection curves of different CuI/Si heterojunction films.

3.4 Photovoltaic performance of the CuI/Si quasi-bulk-heterojunction thin films

3.4.1 Photoelectrochemical measurements

For understanding the performance of p-CuI/n-Si heterojunction thin films, photoelectrochemical measurements were carried out under chopped light (300W Xe lamp) in 0.1 M Na_2SO_4 solution. Figure 5a shows the current-time (I-t) curves for each of the following samples: untreated n-Si, CuI/Si-100, and CuI/Si-200. The photocurrent density of the CuI/Si-100 sample increased relative to the bare n-Si sample, and the CuI/Si-200 sample had an even greater photocurrent density with a value of nearly 0.9 mA/cm^2. Open circuit potential (OCP) was studied with chopped light (as shown in Figure 5b). The corresponding I-V curves of both CuI/Si-100 and CuI/Si-200 samples showed significant difference of open circuit potentials (about 0.18 V and 0.3 V) between dark and light conditions. Such a difference may be induced by the higher interface electric field between the p-CuI and n-Si in the CuI/Si-200 sample. The results indicate that p-CuI of a suitable thickness coated on the n-type Si surface will improve the performance of the p-CuI/n-Si heterojunction film.

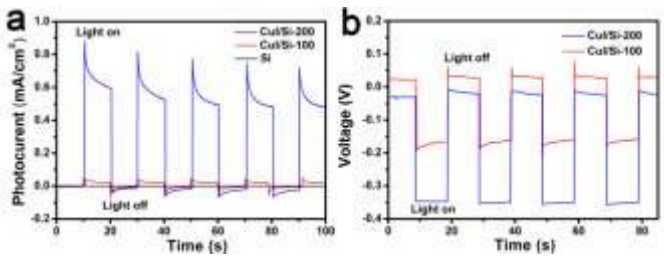

Figure 5. I-t curves recorded at 0V *vs.* SCE (a) and V-t curves of the thin films in 0.1M Na_2SO_4 solution *vs.* SCE under 300 W Xe lamp (b).

The photocurrent and photovoltage enhancement in CuI/Si-200 was further studied by photocurrent-potential method with chopped light in 0.1 M Na_2SO_4 solution. The charge separation efficiency can be well illustrated from onset potential and photocurrent intensity variation. The onset potential can be defined as the photocurrent where the signal changes from negative to positive.[21] The photovoltage generated after irradiation was defined as ΔV, and $\Delta V = \Delta V_{sur} - \Delta V_{int}$, where ΔV_{sur} is the photovoltage of the surface and $-\Delta V_{int}$ is the photovoltage of the interface. The negative sign indicates opposing directions of the surface and interface potentials.[22] As shown in Figure 6, the onset potential was about -0.5 V in CuI/Si-200 and -0.25 V in CuI/Si-100. Considering that there are no considerable morphology differences in the surface of CuI/Si-200 and CuI/Si-100 samples (see Figure 3c and 3d), the ΔV_{sur} of each of the two samples can be disregarded, and thus the variation of the onset potentials of CuI/Si-200 and CuI/Si-100 are dictated by their respective interface electric fields.[22] Under illumination, the charge carriers are generated in n-Si and separated by the interface electric field, and photoinduced holes transfer to CuI layer. As reported, the large magnitude of interface electric field intensity will result in a negative shift of the photocurrent.[23] The -0.25 V onset potential shift between CuI/Si-200 and CuI/Si-100 samples indicates a stronger p-CuI and n-Si interface electric field for CuI/Si-200. Therefore, we believe that the intensity of the interface electric field can be tuned by controlling the thickness of CuI thin film in the CuI/Si structures.

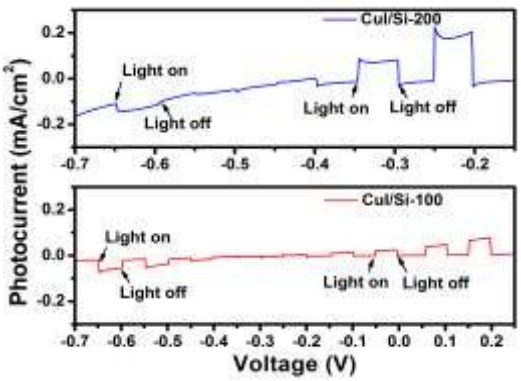

Figure 6. Photocurrent−potential characteristics of the CuI/Si thin films in 0.1 M Na_2SO_4 solution under 300W Xe lamp.

3.4.2 Transient photovoltaic (TPV) study

For further understanding of the behaviour of the p-CuI/n-Si quasi-bulk-heterojunction thin films, transient photovoltage (TPV) measurements were carried out. Figure 7 shows the TPV curves of the CuI/Si-100 and CuI/Si-200 samples with top electrode illumination. The light passed through the CuI layer and was mainly absorbed by the n-Si layer due to the limitation of the band gap. Consequently, the photo generated carriers were separated at the p-n junction of the CuI/Si interface, while photoinduced holes were transferred to the CuI layer (irradiation side) and led to a positive signal during the

response range. The intensity of the photovoltage of CuI/Si-100 was higher than CuI/Si-200 due to the amount of the separated charges in space.[24,25] However, the decay of the surface photovoltge intensity of the CuI/Si-200 sample was significantly slower than that of CuI/Si-100 sample, indicating that the carrier life time in CuI/Si-200 sample was prolonged. This observation is in accordance with the large magnitude of interfacial electric field and efficient charge separation in Figure 6.

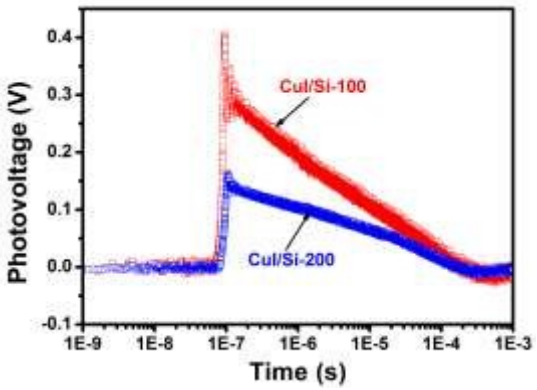

Figure 7. TPV measurements of CuI/Si-100 and CuI/Si-200 with 532 nm laser pulse.

3.4.3 Device fabrication

Energy bands play a critical role in carrier transportation. High energy barriers will limit the electron or hole transport. For improving hole transportation from CuI to the electrode, PEDOT:PSS was used as the interface modification material to match the energy band gap. Figure 8a shows the SEM image of the Si/CuI/PEDOT:PSS active layer and schematic picture of the assembled solar cell device (inset). As we expected, the CuI surface was fully covered by PEDOT:PSS not only on the pyramidal crystal surface but also in the gap between them.

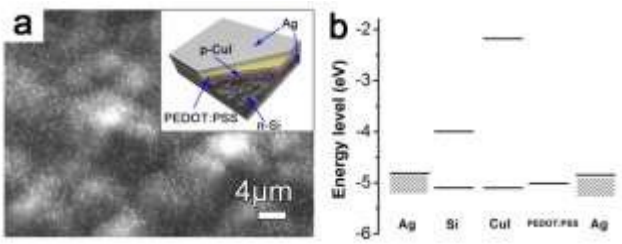

Figure 8. SEM images of Si/CuI/PEDOT:PSS bulk heterojunction thin film (a) and corresponding energy level (b). The insert is the schematic picture of the Si/CuI/PEDOT:PSS bulk heterojunction solar cell device.

The corresponding energy level is plotted in Figure 8b according to the literature.[26] In such devices CuI is a p-type semiconductor and the photo-generated hole carriers transfer the positive charges in this layer. The difference of the energy level between CuI and Ag is relatively large, resulting in a barrier to the hole transport process. The work function of PEDOT:PSS is between -4.8 eV ~ -5.2 eV. Although the separated holes can be collected by Ag electrode, with this interlayer the photo-generated holes will go through a relatively low barrier to the Ag electrode. The resulting photovoltaic region has an active area of 0.2 cm^2 (defined by the silver electrode area). For investigating the performance of such quasi-bulk-heterojunction thin film solar cells, we further conducted preliminarily measurements on the resulting Si/CuI/PEDOT:PSS solar cell device under a sunlight simulator with AM 1.5G illumination (100 mW•cm^{-2}) (see Figure S3 in supporting information). We preliminary obtained a short circuit current density (Jsc) of 3.36 mA•cm^{-2}, an open circuit voltage (Voc) of 0.33 V, a fill factor (FF) of 19.12%, and power conversion efficiency (PCE) of 0.32% with an un-optimized sample. It is expected that the PCE of the CuI/Si solar cell device which fabricated at room temperature may be improved by decreasing the n-Si thickness and optimizing the CuI/Si interface.

Conclusions

We developed a facile room temperature iodination approach to in-situ fabrication of monocrystalline CuI/ Si quasi-bulk-heterojunction thin films by firstly depositing an elemental copper layer on pretreated monocrystalline silicon surface followed by a direct elemental reaction with iodine vapour. We demonstrated that the pretreated silicon exhibits pyramidally patterned surface which facilitates the construction of quasi-bulk-heterojunction thin films and enhances the surface roughness, chemical stability, and mechanical stability of the resulting heterojunction films. The infiltrated elemental copper layer can be well controlled and completely transformed into crystallized CuI thin film for in-situ construction of CuI/Si quasi-bulk-heterojunction at room temperature. The thickness of the upper CuI layer can be controlled by simply controlling the initial elemental Cu layer. The photoelectrochemical and transient photovoltage (TPV) measurements determined that the intensity of the interface electric field as well as the open circuit potential can be adjusted by tuning the amount of CuI coated on the pyramidally patterned n-Si substrate. We assembled a solar cell device with CuI/Si as the active layer and preliminarily checked the photovoltaic performance of an un-optimized solar cell device. Significantly, the direct elemental reaction route reported here can be extended to construct other p-CuI based heterojunction thin films for industrial photovoltaic applications.

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Notes and references

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Electronic Supplementary Information (ESI) available: XRD patterns of virgin, pretreated Si substrate and CuI/Si-100 sample, and I-V curve of the CuI/Si solar cell device. See DOI:10.1039/b000000x/

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