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Sodium Ion-Assisted Memory Behaviour of Silicon Nanowire Partial Composite Field-Effect Transistor

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A partial composite consisting of rough silicon nanowires and a polymer dielectric layer with sufficient Na^+ ions was used to create a field-effect transistor based memory device. Addition of Na^+ ions helped compensate for water molecule trapped charges led to narrow hysteresis characteristics and stable memory retention stability of the resulting device.

One-dimensional (1D) nanostructures such as nanowires (NWs),[1–3] nanotubes,[4,5] and nanoribbons[6,7] have attracted considerable interest because of their unique physical properties for next generation electronic applications given their ability to overcome the limitations of conventional semiconductors. Over the past decade, field-effect transistors (FETs),[8–10] diodes,[11,12] sensors,[13,14] and logic circuits[15,16] based on 1D semiconductor nanostructures have been introduced along with the various strategies for utilising their novel characteristics. Recently, non-volatile memory devices fabricated with nanomaterial based FETs have been achieved (e.g. carbon nanotube (CNT) FETs[17,18] and various inorganic NW FETs[19,20]) with their memory behaviour based on the large hysteresis originating from charge-trapping by water molecules at the active surface.

However, memory devices depending on attached water molecules have vulnerable retention stability and relatively low speeds for write/erase operations.[21] In an effort to improve this shortcoming, a nano sized floating gate site has been introduced to assist with additional charge storage;[22,23] however, fabricating a floating gate is too complex to adopt in commercial memory device fabrication processes.

In this work, a FET-based memory device with a partial composite[24] of rough silicon (Si) NWs and a mobile Na^+-ion-rich organic gate dielectric layer is introduced to solve the above issue. It was hypothesized that the magnitude of hysteresis in rough Si NW FETs with a counter-clockwise rotation would be reduced by attaching water molecules with a high concentration of Na^+ ions with clockwise hysteresis. Therefore, Si NW FETs with sufficient Na^+ ions in the dielectric layer could show narrow hysteresis characteristics.

Additionally, the large interfacial area between the semiconductor and dielectric layer could maximize the electrochemical reaction between the Na^+ ions and the rough Si NWs. Unlike conventional memory devices, which use charge traps activated by an electric field and which have large hysteresis, the combination of diffused Na^+ ions and water molecules on rough Si NWs could enable novel and stable memory behaviour by creating narrow hysteresis in the FETs.

Furthermore, the partial composite based on transfer implantation for fabricating the FETs enables high-performance flexible and printable memory devices.[24] Additionally, the large area interfacial interactions between the rough NWs and polymer dielectric layer could enable a number of novel characteristics and various applications. Generally, the high surface-to-volume ratio of the NWs strongly influence the characteristics of NW-based devices based on the surface properties, which depend on interactions with the surrounding environment.
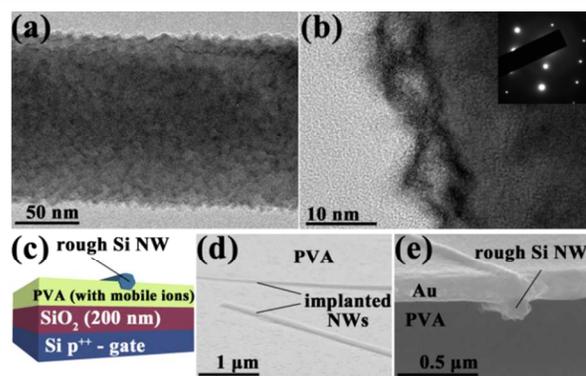

FIG. 1. (a) TEM contrast image and (b) HR TEM image show a representative rough surface of the Si NW. The synthesized Si NW that is single-crystalline with the <100> direction has a rough surface at the nanoscale. An Inset image represents SAED pattern of the Si NW.(c) The schematic illustrates the cross-section through the thin-film partial composite of Si NW on PVA. (d) and (e) show SEM images of the implanted states of NWs on PVA and cross-sectional features of the final device deposited an Au electrode, respectively.

Fig. 1(a) shows a transmission electron microscopy (TEM) contrast image. In this TEM image, the Si NW surface was well distinguished with roughness period of several nanometres. In Fig. 1(b), a high-resolution (HR) image of the rough NW is shown. Further, it is noticed that the single crystalline lattice fringes of the NWs were maintained. Fig. 1(c) shows a schematic cross-section illustration of the FET fabricated with a Si NW thin-film partial composite on a Poly(vinyl alcohol) (PVA) layer. A representative field-emission scanning electron microscopy (FESEM) image of the embedded states of the NWs on PVA, and the cross-sectional features of the final device fabricated on an Au electrode (for Ohmic contact to the p-type Si NWs) are shown in Fig. 1(d), and (e), respectively. Over 50% of the NW appears to be embedded in the PVA layer.

The PVA solution was categorized into three major types: a blend of 5 wt% PVA and sodium acetate (NaAc) (Sample I. 1:0, Sample II. 1:0.05, and Sample III. 1:0.1 wt. ratios) in H_2O. PVA is the polymer dielectric without intrinsic hysteresis, whereas the hysteresis in gate bias of devices is often observed with an electric field between the gate and the source/drain electrodes. Because conventional industrial production of PVA produces dilute NaAc during the synthesis reaction, residual mobile Na^+ ions in the PVA dielectric film are known to affect the hysteresis through field-induced polarization during FET operation.[25] Further, the rough Si NWs show a similarly significant hysteresis loop because of the water molecules. The NWs considerably increase the surface area owing to their roughness, which provides more adsorption sites on the NW surface and induces strong charge trapping. However, the duration of charge storage owing to the water molecules is very short and therefore creates vulnerability as memory elements.[21,23] In response to this we incorporated mobile Na^+ ions and water molecules on the rough Si NWs to greatly enhance memory performance.
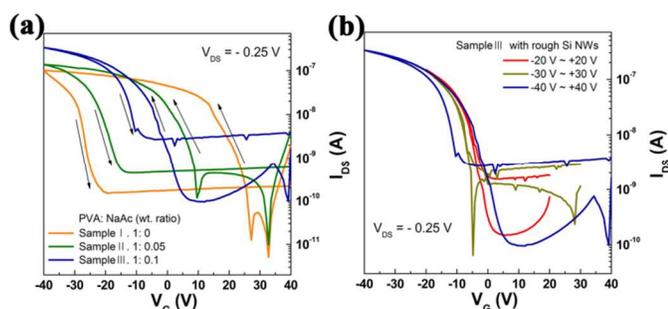

FIG. 2. (a) The transfer curves with rough Si NWs at different concentrations of NaAc in the PVA dielectric layer. Transfer curves of forward sweep and backward sweep are shown for the hysteresis measurements. The directions of the forward and backward sweeps are indicated. (b) The transfer curves in Sample III with rough Si NWs at different ranges of V_G sweeping from ±20 V to ±40 V.

Fig. 2(a) shows the drain-current-gate-voltage (I_{DS}–V_G) transfer characteristics, which were obtained from the rough Si NW FETs on a PVA gate dielectric. Forward and backward sweeps of the gate voltage from 40 V to −40 V at a fixed V_{DS} of −0.25 V are included in the figure. For Sample I, without additional mobile ions in the PVA dielectric, a threshold voltage shift of 50 V was attained. The hysteresis in this type of the device results from the water molecule charge trap sites on the rough Si NWs. As the concentration of NaAc in the PVA gate dielectric increases, the threshold voltage shifts. For

Sample II and Sample III it dramatically decreases to 24 V and 4.8 V, respectively. The on-off ratio of the devices reduces from Sample I to Sample III because the off-state current increases owing to the high conductivity of the mobile ions. We can speculate that some transition of charge trapping is brought on by the mobile Na^+ ions at the semiconductor/dielectric interface. The hysteresis loops owing to the water molecules on the rough Si NW and to the mobile ions in the dielectric layer have opposite directions: the former is clockwise, and the latter is counter-clockwise in the p-type FETs.[26] Rapid polarization relaxation and rising dielectric constants (k) induced by the mobile ions in the PVA dielectric layer also assist the rapid switching behaviour by the electric field (Fig. S1, ESI†). As a result, the magnitude of hysteresis in the rough NW FETs can be controlled by the concentration of mobile ions. On the other hand, the electrical properties of semiconductors having relatively less surface area between the channel and dielectric interface such as smooth Si NWs or organic thin film structures did not change appreciably with the addition of mobile ions (Figs. S2 and S3, ESI†). From these results, we can conclude that the high surface-to-volume ratio of the rough NWs and the dispersed mobile ions over the large interfacial area strongly influence the electrical characteristics. The transfer characteristics of Sample III at different sweep ranges of V_G from ±20 V to ±40 V at a fixed V_{DS} of −0.25 V are shown in Fig. 2(b). The transfer curves with V_G sweep below ±30 V indicate nearly narrow hysteresis characteristics. The details of the electrical properties of each device are summarized in Table S4 in the ESI†.

The water molecule charge traps on the rough Si NWs lead to large hysteresis, although its utility in memory applications is limited owing to very short charge storage without any additional processing.[23] However, if there are Na^+ ions at the interface between the rough Si NWs and PVA dielectric layer, creating a high density of charge distribution, we can expect an improved memory effect enabled by this simple process. Since the Na^+ ions electrochemically intercalate into the rough Si NWs, the memory behaviour enabled by charge trapping is efficiently maximized.[27] While standard memory behaviour *via* charge-trapping and the gate-field effect has been reported based on large hysteresis,[23,28,29] the synergy of combining water molecules and Na^+ ions enables a memory effect by effectively utilizing narrow hysteresis.
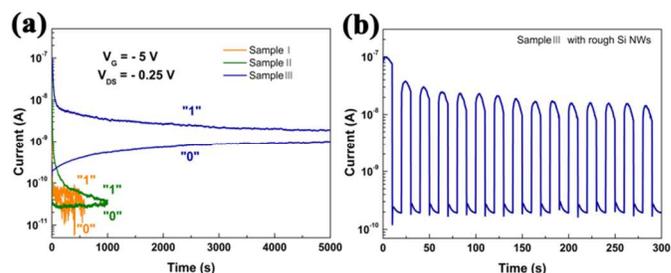

FIG. 3. (a) Time dependent stability of conductance in the two states at different concentrations of mobile ions. The on-state "1" with a V_G of 40 V and off-state "0" was obtained with a V_G of −40 V for 1 s. (b) Memory operation in Sample III with rough Si NWs, where writing and erasing were performed with 1 s gate pulsing of 40 V and −40 V, respectively. The currents of on and off states were read with V_{DS} = −0.25 V at V_G = −5 V for 10 s.

Fig. 3(a) shows the charge retention behaviour of the rough Si NW FETs incorporated with mobile ions in the dielectric layer and water molecules on the rough Si NWs. The measurements of drain currents were taken after applying on and off operations under gate voltages of −40 V and 40 V, respectively, for 1 s. The performance of the memory devices as a function of increasing mobile ion concentration was greatly improved. In the sample without additional NaAc (Sample I), large hysteresis in the NW FETs failed to help the retention performance because the water molecule charge traps faded exponentially with time. In Sample II, with a wt. ratio of 1:0.05 PVA to NaAc, the on drain current significantly decayed within a period of 1000 s. Meanwhile, Sample III, with sufficient concentration of the mobile Na^+ ions, maintained and continued the retention behaviour over the entire measured period. To confirm that these improvements were caused by the partial composite between the large surface area of the rough NWs and the mobile ions in the dielectric layer, the memory behaviours of smooth Si NWs with Na^+ concentration identical to Sample III are shown in Fig. S5 in the ESI†. The smooth NW devices show imperceptible retention characteristics, and the memory margin is too low since there are too few water molecule charge traps.

Fig. 3(b) shows the memory operation of Sample III with rough Si NWs, where writing and erasing operations were achieved by a gate field of −40 V and 40 V, respectively, and reading was performed for 10 s. The duration of the on/off switching was quite stable for more than 300 cycles (extended data is shown in Fig. S6, ESI†).

In conclusion, stable memory devices were fabricated using a partial composite consisting of rough Si NWs and a dielectric layer with Na^+ ions. This partial composite structure was introduced to increase the interfacial interactions between the rough NW and PVA gate dielectric material. The transfer curves with sufficient concentration of Na^+ ions indicate nearly narrow hysteresis characteristics. The combination of water molecules and mobile ions at the semiconductor/dielectric interface enables a memory effect without large hysteresis.

Acknowledgments

Notes and references

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