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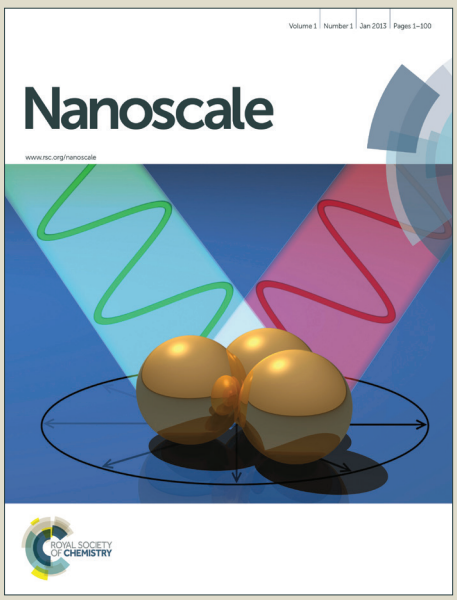

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Fabrication of sub-20 nm Nanopore Arrays in Membranes with Embedded Metal Electrodes at Wafer Scales

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Abstract:

We introduce a method to fabricate solid-state nanopores at sub-20 nm diameter in membranes with embedded metal electrodes across a 200 mm wafer with CMOS compatible semiconductor processes. Multi-layer (metal-dielectric) structures embedded in membranes were demonstrated with high uniformity (± 0.5 nm) across the wafer. Arrays of nanopores were fabricated with average size of 18 ± 2 nm in diameter using a Reactive Ion Etching (RIE) method in lieu of TEM drilling. Shorts between the membrane-embedded metals were occasionally created after pore formation, but the RIE based pores had a much better yield (99%) of unshorted electrodes compared to TEM drilled pores (<10%). Double-stranded DNA of length 1 kbp was translocated through the multi-layer structure RIE-based nanopore demonstrating that the pores were open. The ionic current through the pore can be modulated with a gain of 3 using embedded electrodes functioning as a gate in 0.1 mM KCl aqueous solution. This fabrication approach can potentially pave the way to manufacturable nanopore arrays with the ability to electrically control the movement of single or double-stranded DNA inside the pore with embedded electrodes.

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In 2001, the first Solid-State Nanopore (SSN) at 1.8 nm in diameter was made in a thin insulating silicon nitride membrane by the method called "Ion-Beam sculpting".[1] The resulting structure triggered a large number of biophysics studies. In such system the insulating membrane separates the electrolyte solution into two regions (known as *cis* and *trans*), and fluid or molecules could translocate from one region to the other only through the nanopore. The realization that single or double-stranded DNA can be driven through a nanopore by a small bias voltage across the membrane, made solid-state nanopores (SSN) hold great promise for single-molecule DNA sequencing.[2,3] Compared to their counterpart of proteinaceous pores[4], SSNs have unprecedented properties, such as a controllable pore size and thickness[5,6] ,stability under high voltage[7], and tunable surface properties[8] which can alter the surface charge in the pore and the subsequent counter-ion sheath formation. SSNs have been widely used to detect DNA translocation[1], methylated DNA[9,10], RNA[11], and Protein. [12,13] Several kinds of insulating thin membranes have been explored to make SSNs, including graphene[14], SiNx[1,15], SiO_2[5], Al_2O_3[16], mixed dielectric/metal structures[17,18,19] and other[20,21].

The fabrication methods for SSN have relied on energized beam drilling, for example, with an electron beam in a Transmission Electron Microscope (TEM)[5], a Ga ion beam in a Focused Ion Beam (FIB)[22,23]and a Helium Ion Beam (HIB)[24]. These approaches are useful for research applications on a single chip scale, but difficult to scale to the 200 or 300 mm diameter wafer dimensions appropriate for scale-up and manufacturing. The most widely used technique, TEM drilling, also limits the sample size to a few mm in width due to the nature of the sample holder in most TEMs. In these fabrication approaches, the nanopore is formed after the membrane is released from the Si substrate by etching through the backside of the sample. This integration approach can be called a 'pore-last' scheme since it

is not advisable to do any additional fabrication steps on the very fragile membrane after it is released and a pore has been drilled through it. In addition, for relatively complex membrane structures with multiple metal and dielectric layers, energized beam drilling of the nanopore has been observed to cause smearing of the nanometer-thick metal-dielectric-metal stacks due to the atom migration, heating, agglomeration or sputtering.[25] This is not favorable for the application of single molecular motion control or sensing in these nanopores due to high levels of electrical leakage current between electrode layers which comes from diffuse metal-dielectric-metal boundary inside the nanopore caused by such thermal and re-deposition effects during directed beam drilling in the TEM. Here, we demonstrate an alternative fabrication approach based on reactive ion etching (RIE) nanopore fabrication using a 'pore-first' approach through a membrane with an embedded 3-level metal, which is compatible with wafer scale production of electrically and structurally functional nanopore devices.

Figure 1 shows the concept and implementation of manufacturable, pore-first RIE based nanopore fabrication. A schematic of the fabrication process is shown in Fig. 1(a). A wafer with a Si_3N_4 coating at both of its sides is used as the starting substrate (Fig. 1(a) top diagram), followed by multi-level metal/dielectrics deposition and patterning on both sides of the wafer. At the region where the single nanopore will be located, the material stack comprises 3 metal layers of 5 nm Titanium Nitride (TiNx) separated by 5 nm Plasma-Enhanced Chemical Vapor Deposition (PECVD) SiO_2 (Fig. 1(a) second diagram). Figure 1(b) shows a TEM image of the 3-metal stack region, which are M3, M2 and M1 from top to bottom. In Figure 1(c), a TEM cross-section image shows the extremely uniform multi-layer structures, corresponding to a cut along the black line in Figure 1(b). Zoomed-in TEM cross-section shows the detailed multi-layer structures with a precise control thickness of each layer of 5.5 ± 0.5 nm (Figure 1(d)). Each TiNx electrode is formed by Physical Vapor Deposition (PVD) and then patterned

into 400 nm wide strip by Deep Ultraviolet (DUV) lithography and RIE. Additional top metal thicker levels (50 nm) are used to connect each thin (5 nm) metal layer in the stack to the contact pads. A Tri-layer Electron Beam Lithography (EBL) mask was used to precisely pattern the nanopore etch mask on top of the 3-metal stack region. The tri-layer mask consists of an e-beam sensitive resist on top of a thin SiARC layer on top of a thick organic planarizing layer[26]. Sub-20nm holes were patterned in the e-beam resist and transferred into the underlying two layers. This enabled a thick, high aspect ratio and highly selective mask to transfer the pattern into the metal oxide stack. After the sub-20nm e-beam pattern was transferred into the thick tri-layer mask, a multi-step RIE was adapted to etch through of the 55 nm thick metal/dielectric stacks. A Cl_2-based plasma discharge chemistry was used to etch the pattern through the metal oxide stack. The highly selective tri-layer mask enabled pattern transfer completely through the metal oxide stack, while preserving the sub-20nm diameter nanopore (Fig. 1(a) third diagram). After the nanopore formation, a protective 150 nm PECVD Si_3N_4 layer was used to cover and protect the pore, together with an additional 200nm SiO_2/ 200nm Si_3N_4 bilayer (Fig. 1(a) fourth diagram) to reduce any stray electrical current leakage from metal line to electrolyte under nanopore working conditions. After these coatings and suitable lithography, RIE is used to open a 6μm well through the top 200nm Si_3N_4 and land on the 200nm SiO_2, after which a second RIE step selective to Si_3N_4 is used to etch through 200nm SiO_2 (Fig. 1(a) bottom diagram). Tetramethylammonium hydroxide (TMAH) was used to etch the Si substrate from the back side of the wafer. This etch stopped on the thin Si_3N_4 layer under the nanopore, forming a 55 nm thick membrane window underneath the nanopore region. Finally, the nanopore is uncovered with a hot phosphoric acid to remove the protective Si_3N_4 both underneath and on top of the metal-dielectric stack and embedded nanopore (Fig. 1(a) bottom diagram). The final membrane device structure consists of (from the bottom up) a 10 nm thick SiO_2 layer, with three 5 nm thick TiN electrodes which are separated by 5 nm silicon dioxide layers (25 nm total) and a final top 20

nm thick silicon dioxide layer. The goal of the top and bottom silicon dioxide layers is to reduce noise and coupling of the metal electrodes to the two fluidic cells (Cis and Trans) located above and below the nanopore membrane. As mentioned before, the thick (400 nm) SiO_2/Si_3N_4 dielectric layer deposited above the membrane stack, with only a 6 μm diameter opening made at the nanopore region for electrolyte assessment, substantially reduce noise and leakage. When completed, the wafer was diced into 10 mm x 10 mm single chips for usage in fluid cells.

A RIE etched nanopore can be fabricated through the metal overlaps. A high magnification top-down TEM imaging shows a single pore with 20 nm in diameter in Figure 1(e), which has concentric ring structure with inner ring composed of amorphous SiO_2 and out ring of cross-section polycrystalline TiN. This is further confirmed by (Figure 2(b)) which clearly shows a tapered profile with top opening ~40 nm and bottom opening ~20 nm. The tapered nanopore is the result of the RIE process, due to the multiple chemistries used to etch both the TiN and SiO_2 layers. With this highly integrated process, the RIE based nanopore fabrication also allows the fabrication of nanopore arrays of densely packed nanopores with uniform pore size, 18 ± 2 nm and single conical angle 12.7 ± 5.4° (N = 19), as shown in Figure 1(f). Please see more TEM and SEM cross-sections of nanopore arrays in Figure S1, Supporting Information. Compared to previously reported nanopore fabrication protocols by FIB or TEM, where nanopores are drilled after the membrane formation (pore-last process) on individual, small chips, the pore-first RIE strategy used here avoids processing of a membrane-containing wafer. This allows the use of a wide range of semiconductor processing and integration steps, in conjunction with and following the nanopore etching process, as well as the use of full-size wafer substrates (200 and 300 mm diameter) throughout the entire fabrication process. This enhances both process reproducibility and safety. Therefore, the pore-first strategy is compatible with VLSI integration allowing for integration options

such as on-chip circuits or the integration of nanopores with existing FET devices on the Si substrate. As illustrated in Figure 1(g), 200 mm wafers of patterned in a matrix of 11 by 11 3-metal nanopore devices are routinely produced in quantity using this strategy, resulting in 121 devices per wafer. The achievement of RIE based nanopore array production at a wafer scale is of great significant towards high throughput parallel processing in DNA sequencing as well as other single molecule applications.

The mechanism of energetic-beam-based nanopore formation is fundamentally different from the RIE-based nanopore formation. In the energetic-beam-based process, it appears that fairly little material is actually removed by electron bombardment. The high energy density of the beam distorts the sample and pore formation may be partially driven by surface tension of the heated material in the beam and the momentum transfer between the beam with high energy and the heated material. Though the drilling mechanism in the TEM is not completely understood, the high energy electron beam can cause knock-on or radiolysis damage in samples [27]. Knock-on is direct displacement of sample atoms by the electron beam. Radiolysis is e-beam induced sample heating. Both damage mechanisms could lead to mixing of the metal and dielectric layers in this hot region, which will result in significant leakage current between the metal layers, on the order of nA to μA. This is verified in the cross-sectional view of the multilayer metal/dielectric stacks with a TEM drilled nanopore. As shown in Figure 2(a), the trajectory of ~5 nm nanopore embedded in 100 nm thick FIB prepared sample can be roughly distinguished under TEM. The metal/dielectric interface is clearly distinguishable at most of the interface area. However, it becomes smeared at the nanopore region. Clear fencing structures arise at the nanopore edge from each layer of the metals. Interestingly, all fencing points upwards, which is in the same direction as the transmission electron beam when the nanopore is drilled. (The sample is drilled from the backside of the chip.) The intermixing of metal and dielectric materials can severely degrade the dielectric insulating property. Moreover, at relative small metal separation, for example the 5 nm in our device, the migration of

metallic composite along with nanopore formation may directly bridge two metal electrodes. In our cross-sectional TEM image, this is clearly evidenced by a metal nanostructure reached from the bottom electrode and to the middle electrode. The degradation of the dielectric/metal interface and the growth of metal protrusion introduced large leakage current between adjacent metal stacks. This mixed-material leakage path was not successfully removed by etching or other chemical reduction paths, nor has it been possible to disrupt the leakage path by high current fusing. In addition, these TEM-drilled nanopores were not stable over time or in the presence of an electron beam (such as in a TEM or SEM). The nanopore would close, presumably due to relaxation of the stressed material, in hours to days at room temperature, or in seconds under electron beam exposure.

Unlike TEM or HIB pore formation, a RIE approach results in the complete removal of substrate atoms in the form of volatile molecules that are pumped away. This avoids the concerns relating to later closing of the pores due to relaxation of agglomerated, compressed layers, and more importantly, it maintains the integrity of the metal-dielectric interface. Figure 2(b) shows the TEM cross-section of the same pore in Fig. 1(e). Figure S2 (Supporting Information) shows the element analysis at two spots inside nanopore, which shows there is no TiN at the inside nanopore surface. The fundamental difference between the energetic-beam-based nanopore formation and the RIE-based formation leads to a significantly higher yield of low electric-leakage devices for the RIE approach. Figure 2(c) plots the statistics of leakage currents between two adjacent metal electrodes for TEM derived and RIE-based 3-metal nanopores at 50 mV. There are only 3 out of 46 devices with acceptable leakage current of less than 2 nA at 50 mV for TEM drilled nanopores. About 50% of them have level-to-level leakage current above 1 μA. The same plot also shows the leakage level of the 121 RIE-based nanopores from one whole wafer. The leakage current distribution of RIE-based nanopores is much tighter and significantly

lower than with the TEM method. The electrical yield (< 2 nA) across the wafer is over 99% without process optimization. Figure S3 (Supporting Information) shows the background leakage current before nanopore formed by RIE and TEM. These devices have less leakage current after the nanopore has been formed with RIE, which seems to indicate that semiconductor processes may slightly alter the insulation between metal layers. This high electrical yield is consistent from wafer-to-wafer and over a wide range of pore diameters, suggesting that the RIE pore-formation process is appropriate for large scale manufacturing of nanopore devices.

Compared to the high energy beam drilling method, the most significant challenge for RIE based nanopore formation is the relatively large pore size through the desired stacks. In the semiconductor industry, RIE is widely used for the formation of vias and trenches at dimensions down to the low 10s of nm [28]. While the ultimate spatial limit of RIE is not known, it is thought to be typically on the order of 5 nm. We explored the limit of the pore size produced by lithography followed by RIE through the 3-metal electrode stacks. In order to rule out post-pore formation processing effects (such as pore protection and uncover process) on the size and structure of the pore, we developed a decoration method to evaluate the pore size before membrane formation and determine whether the RIE-based pore goes through the material stacks. Figure 3(a) illustrates the decoration method. The multi-stack metal/dielectric structures are deposited on top of 400 °C growth PECVD amorphous carbon film. After the nanopore RIE, the wafer is treated with O_2 plasma. If the nanopore etch has reach the amorphous carbon layer, the subsequent O_2 plasma treatment would create a cavity underneath the nanopore region. This cavity can be easily observed with automated top-down SEM inspection tools, bypassing the need of the otherwise labor intensive TEM sample preparation and imaging processes. Figure 3(b) shows top-down SEM images for nanopores with different diameters and corresponding cavity sizes after the O_2 plasma treatment. The smallest top critical dimension (CD) through stacks nanopore obtained in this

way was 18 nm. A comparable cross-section SEM through a nanopore array under similar etching condition, yielded a top CD ~18 nm and a bottom CD ~12 nm (see Fig. S1 in Supporting Information). Fig. 3(c) shows a linear dependence between the top CD and the size of the halo, which is a proxy for the bottom CD. A linear fit of the halo size versus the top nanopore diameter intersects the y=0 axis at a top CD of 7.2 nm. At this pore diameter there is no observed cavity formed under SEM. In order to further shrink the size of the nanopore top CD, a thinner membrane can be used resulting in less etch depth for RIE. This has been proved in experiments of shorter etch time in which smaller top CDs (5~10 nm) are observed with no cavity formation after the plasma treatment- indicating an incomplete etching through the stacks. As a consequence, redesign the device stacks for reduced film thickness will be one option towards a smaller RIE based nanopore.

To investigate ionic-transport behavior of RIE-drilled nanopores, we characterized the electrical conductance of the nanopore with a KCl liquid electrolyte. In the experiments reported below we used 10 mm by 10 mm chips diced out of wafers such as those shown in Figure 1(f) with 121 single-nanopore chips. Each chip used in our experiments had only one nanopore at the center of suspended membrane. We used Ag/AgCl electrodes and connected them to a KCl solution in the *cis*- and *trans*- reservoirs. For different KCl molarities, I-V curves were obtained (Fig. 4a) and the electrical resistances were plotted as a function of KCl molarity (Fig. 4b). We identified the presence of surface-charge effects, which induced a saturation of the electrical-conductance at low molarity regime. The surface charge estimated by applying an electro-hydrodynamic model[29] was 0.057 mC/m^2, which is less than the conventional hydroxide (OH-) passivated SiO_2 (25~50 mC/m^2).[30] EELS (electron-energy-loss-spectroscopy) (Figure S2, in Supporting Information) shows that our nanopore structure is surrounded by SiO_2 even on the TiN-electrode region. Interestingly, the RIE-drilling process is likely to result in an effective passivation

of TiN electrode by silicon-oxide, while the reactive-ion physically drilled the nanopore through TiN/SiO_2 multi-layers films by ion-bombardment. However, the surface states of RIE pore wall are different from those of normal SiO_2, which implies that the by-product of gas reactions by fluorine- or chlorine-based gases may make the surface more or less hydrophobic after the RIE process. Then the surface is subjected to an oxygen-based strip process. Subsequently, the pore surface is also exposed to wet processes such as a phosphoric acid dip, a DIW rinse, and a 70% ethanol wash, which may further modify the surface. The detailed evolution of surface properties during such process steps is not known.

We also characterized the ionic current modulation produced by gate voltage biases. A conventional field-effect-transistor (FET) configuration was used, in which source and drain probes were connected to *cis*- and *trans*- reservoirs while a gate probe was connected to the embedded TiN electrode (the M2 electrode was used).[31] Electrodes M1 and M3 were left unconnected to the rest of the circuit. As shown in Fig. 4(c), a negative gate-voltage bias (Vg) induced an increase of ionic current (Id), exhibiting a conventional p-type transistor behavior, implying that the majority carriers are positive ions which screen the surface charges of the nanopore wall. This is consistent with a negative surface charge on the SiO2 surfaces. To rule out that this effect was dominated by leakage currents, we monitored gate-currents while gate-modulation was characterized (Fig 4(d)). We identified that the effect of leakage (Ig) is not very significant compared to the increase of current of drain (Id) and source currents (Is).

In order to further verify that the RIE based pores connect the cis and trans reservoirs and to verify that they have the expected functionalities of solid-state nanopore we performed a series of DNA translocation experiments. 50 nM 2K double-stranded DNA was used to perform translocation

experiments with 20-nm diameter solid-state pore fabricated using the RIE method. Translocation events were characterized by monitoring the ionic current signal through the nanopore. The current traces are shown in Figure 5(a) and the blockade amplitude-versus-dwell time of typical events are shown in Fig. 5(b). All data is acquired and analyzed at 20 KHz sampling rate using a 1 KHz low-pass filter at 10 mM KCl and pH of 5.5. The bias voltage was set at 600 mV. The detailed configuration of these measurements is shown in Fig. S4 (Supporting Information). M1 and M3 are always kept at zero volts. M2 can be switched between 0 V and 1V. The linear current-voltage curve is shown in Fig. S5 (Supporting Information). The conductance of the nanopore is about 3.87 ± 0.22 nS at 10 mM KCL aqueous solution when M2 is 0 V.

The translocation dwell time and blockade-current amplitude[19]are employed to analyze the translocation properties of dsDNA through the nanopore. Figure 5(b) shows the scatter plot of dwell time versus amplitude for the all measured translocation events for the voltage at the M2 electrode set at 0V. From the scatter plot we can see that the dwell time has a broad distribution ranging from from 0 to 100 ms, but most events are located around 3.15 ± 0.23 ms with M2 = 0 V (N = 132). Histograms of dwell times confirm the same behavior (Fig 5(d)). These results are comparable those observed for bare silicon nitride pores.[3]. The zoomed-out curve of dwell time is shown in Fig. S5 (Supporting Information). From the Gaussian fitting of histogram of amplitude (Fig. 5(e)), we observe that the average amplitude is about 144.73 ± 11.02 pA.

Dwell time and blockage amplitude statistics are similar when the voltage at the M2 electrode is set at 1V. In this case the dwell time is about 4.25 ± 0.14 ms while the amplitude is about 142.48 ± 9.43 pA (N = 110). A histogram of dwell time and amplitude for both 0 and 1V states are shown in Fig. S6 (Supporting Information).

A comparison between the dwell time and blockade amplitude when the voltage at the M2 electrode is set at 0V and 1V shows no statistically significant differences. This is to be expected given that the pore size is around 20 to 30 nm in diameter, about one order of magnitude larger than the Debye length at this ionic concentration. A modulation of dwell time and blockade current with different M2 voltages would require the pore size to have dimensions comparable to the Debye length in order for the electric field created by the middle electrodes to penetrate to the center of the pore.[25]

In summary, a functional sub-20nm diameter nanopore with multi-layer electrode structure has been successfully demonstrated using a RIE-based, pore-first fabrication approach at full-wafer scales with over 99% electrical yield. The ionic current can be modulated at 0.1 mM KCl with a biasing electrode for this nanopore device. Double-stranded DNA can translocate through this RIE-formed nanopore showing that the pore is open and that the translocation statistics is similar to previously observed SSNs. This translocation statistics, however, don't show significant differences at 10mM KCl and pore diameter of 20 nm when different voltages are applied on the membrane-embedded electrodes. Our current efforts are focusing on reducing the pore size to dimensions close the diameter of double-stranded DNA and explore the possibility of controlling the movement of charged molecules inside the nanopore.

Associated Content

Supporting information

Additional data, instrumentation and data analysis methods.

Author information

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Figure Captions

Figure 1. Schematics of (a) pore-first fabrication flow of 3-metal layers embedded in a nanopore membrane by reactive-ion-etching; the top diagram shows the substrate with nitride layers on top and bottom sides; the 2nd diagram shows the patterned electrodes; the 3rd diagram shows the nanopore formation by RIE; the 4th diagram shows the protection layers encapsulating the nanopore; the 5th diagram shows the formation of the membrane by removal of the Si substrate. (b) Top-down SEM image of crossed region of three metal layers. From top to down, they are M3, M2, and M1. (c) Cross-sectional TEM image along the black line in (b). It shows the extreme uniformity of the multi layers along 400nm. (d) Zoom-in of the red rectangular region in (c) shows the precise control of each layer thickness around 5 nm. (e) TEM image showing one single nanopore formed with RIE method in the center of crossed-metal region. (f) SEM image showing an array of nanopores fabricated with the RIE method; the average diameter of nanopores is about 18 ± 2 nm. (g) A demonstration of the integration of functional nanopore devices on 8-inch wafer.

Figure 2. (a) TEM cross-sectional image of a TEM drilled nanopore showing metal migration and mixing at the nanopore region, which may contribute to the large leakage currents; the inset shows the top-down TEM image of the same 5 nm diameter pore. (b) Cross-sectional TEM image of a RIE based nanopore, showing well-separated metal levels approaching the edge of the nanopore. The fading of metals towards the nanopore wall may be caused by RIE damage. (c) Scatter plot of leakage characteristic of RIE based (Blue, N = 121) and TEM drilled (Red, N = 46) nanopores.

Figure 3. (a) Illustration of O2 plasma decoration method to explore whether the RIE complete etch through the material stacks; (b) Top-down SEM images of RIE based nanopores with different diameter: 18 nm, 24 nm, 29 nm, 34 nm and the respective e-beam exposure conditions; The lower column images show the corresponding halo (cavity) generated by O2 plasma diffused through the nanopore. (c) Linear fit of the cavity size with the nanopore critical dimension (CD).

Figure 4. Gate-modulations of a metal-embedded nanopore. (a) Electrical conductance of nanopore at different KCl electrolyte molarities. (b) A plot of pore conductance as a function of KCl molarity. Pore conductance is saturated as the molarities of KCl electrolyte becomes less than 10^{-4} M. (c) Measurement of drain current (Id), as gate voltage-bias (Vg) applications at 10^{-4} M. Negative (-) gate voltage-bias increases the pore conductance implying that the majority carrier is positively (+) charged ions. (d) Simultaneous measurement of gate-current (Ig), drain current (Id) and source current (Is) while the gate-modulation was characterized.

Figure 5. Experimental results on dsDNA translocation through a single solid-state nanopore fabricated using the pore-first RIE method. (a) 10 seconds current trace for 50 nM dsDNA in 10mM KCL aqueous solution at 600 mV. (b) Scatter plots (dwell time versus amplitude) for dsDNA translocations through one single solid-state nanopore. (c) Three typical events from current trace (a) are shown.(d) Histogram of dwell time and fitting results, the average dwell time is about 3.15 ms (Black--histogram, red--fitting). (e) Histogram of amplitude and Gaussian fitting results (red--histogram, Green--fitting).

Figure 1

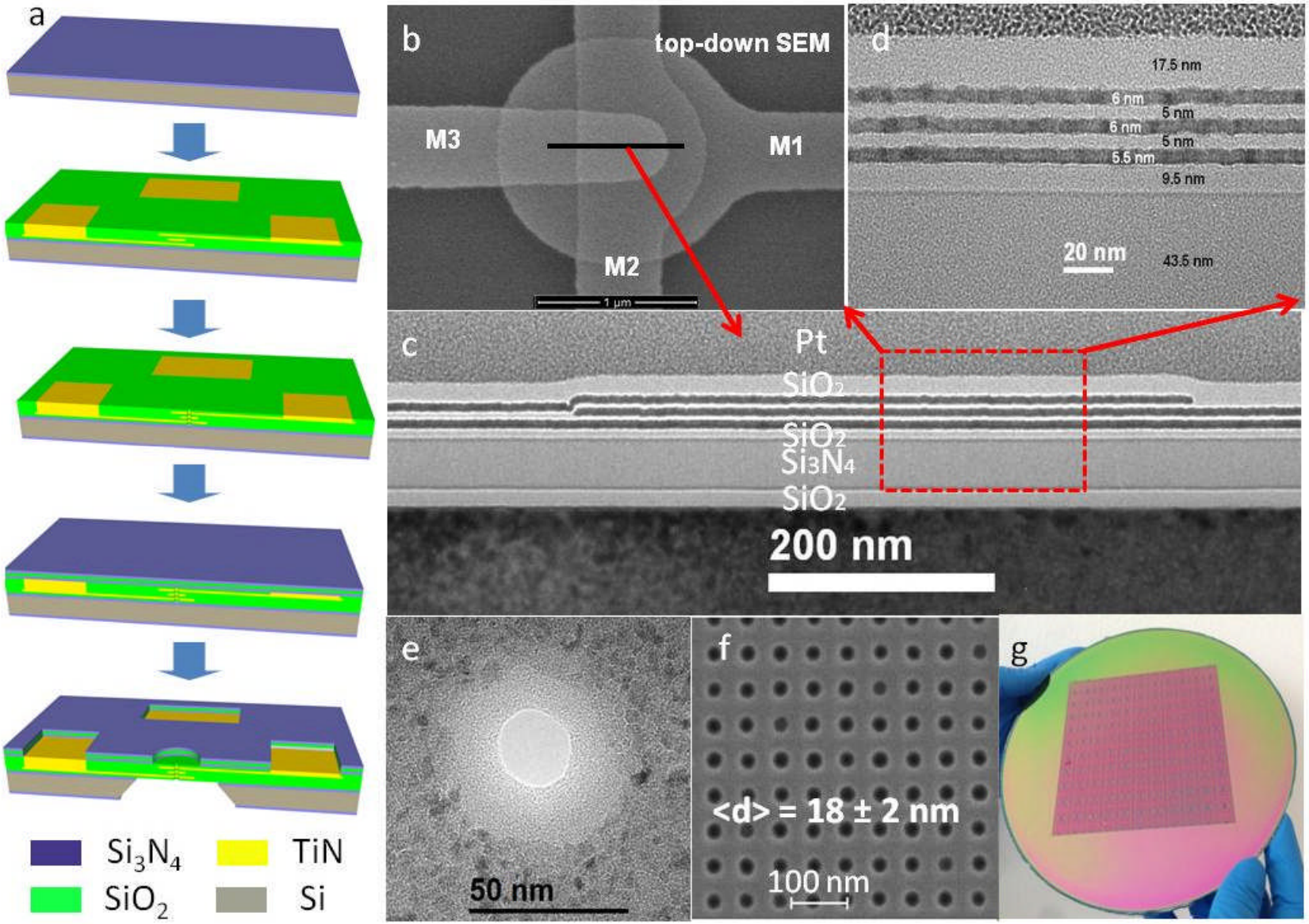

Figure 2

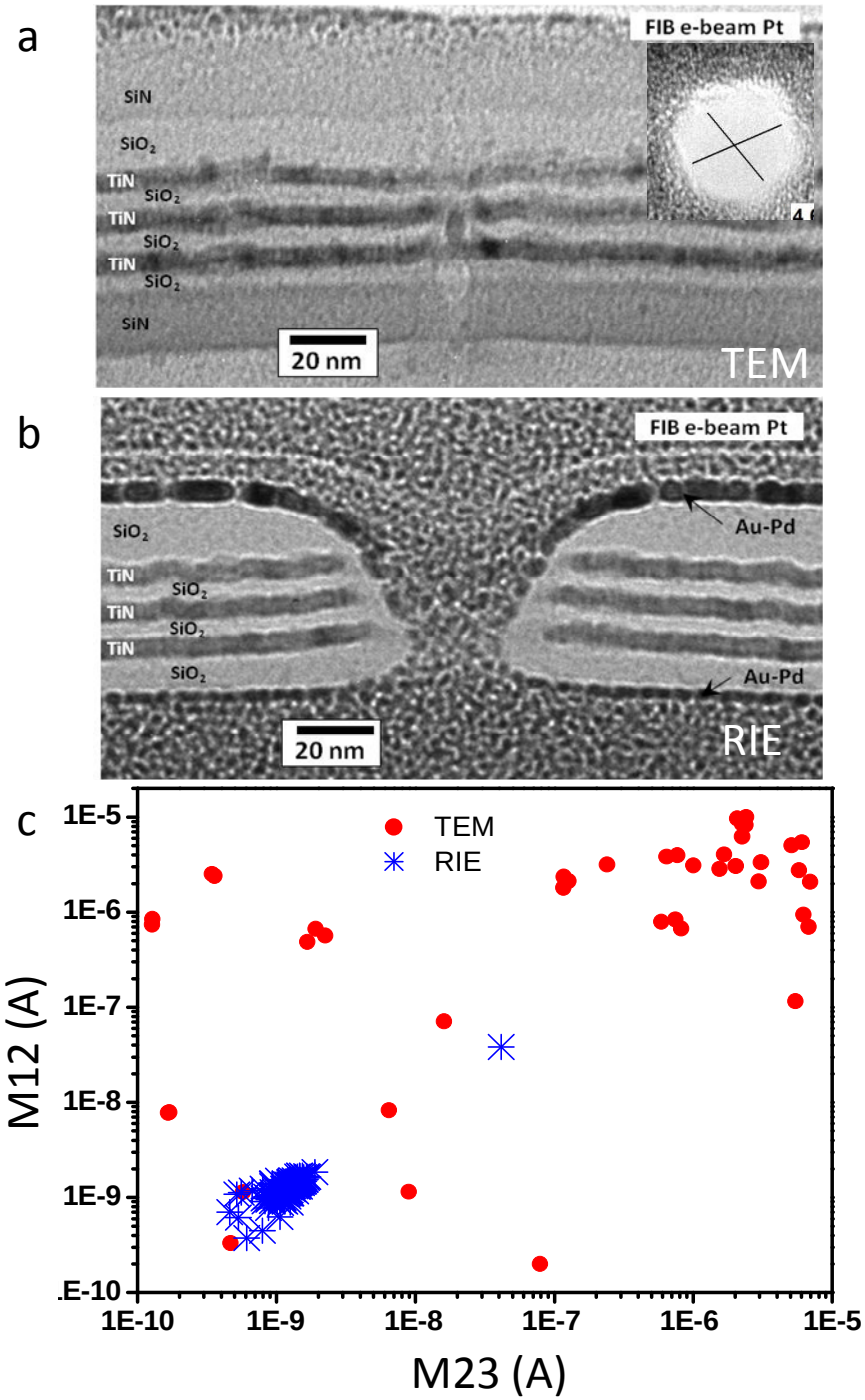

Figure 3

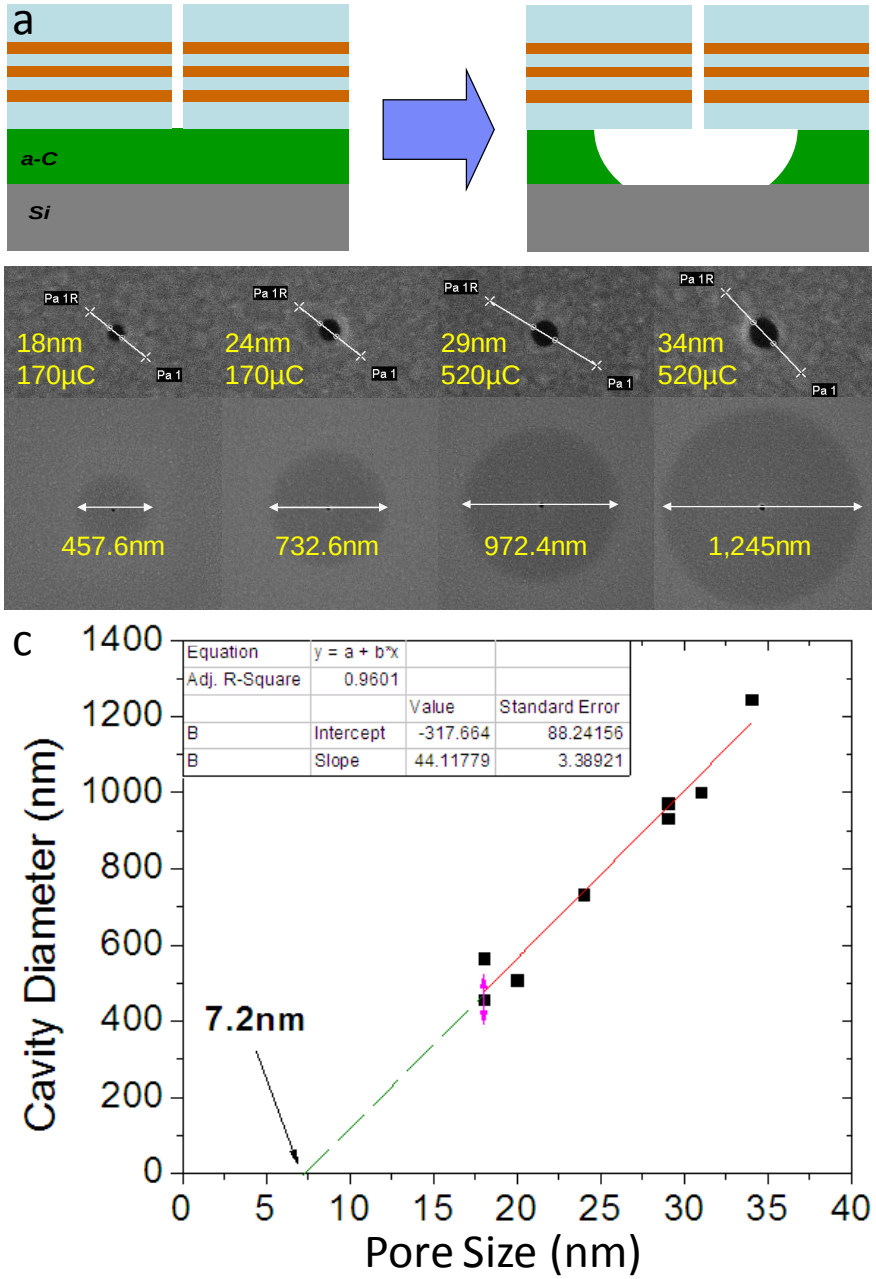

Figure 4

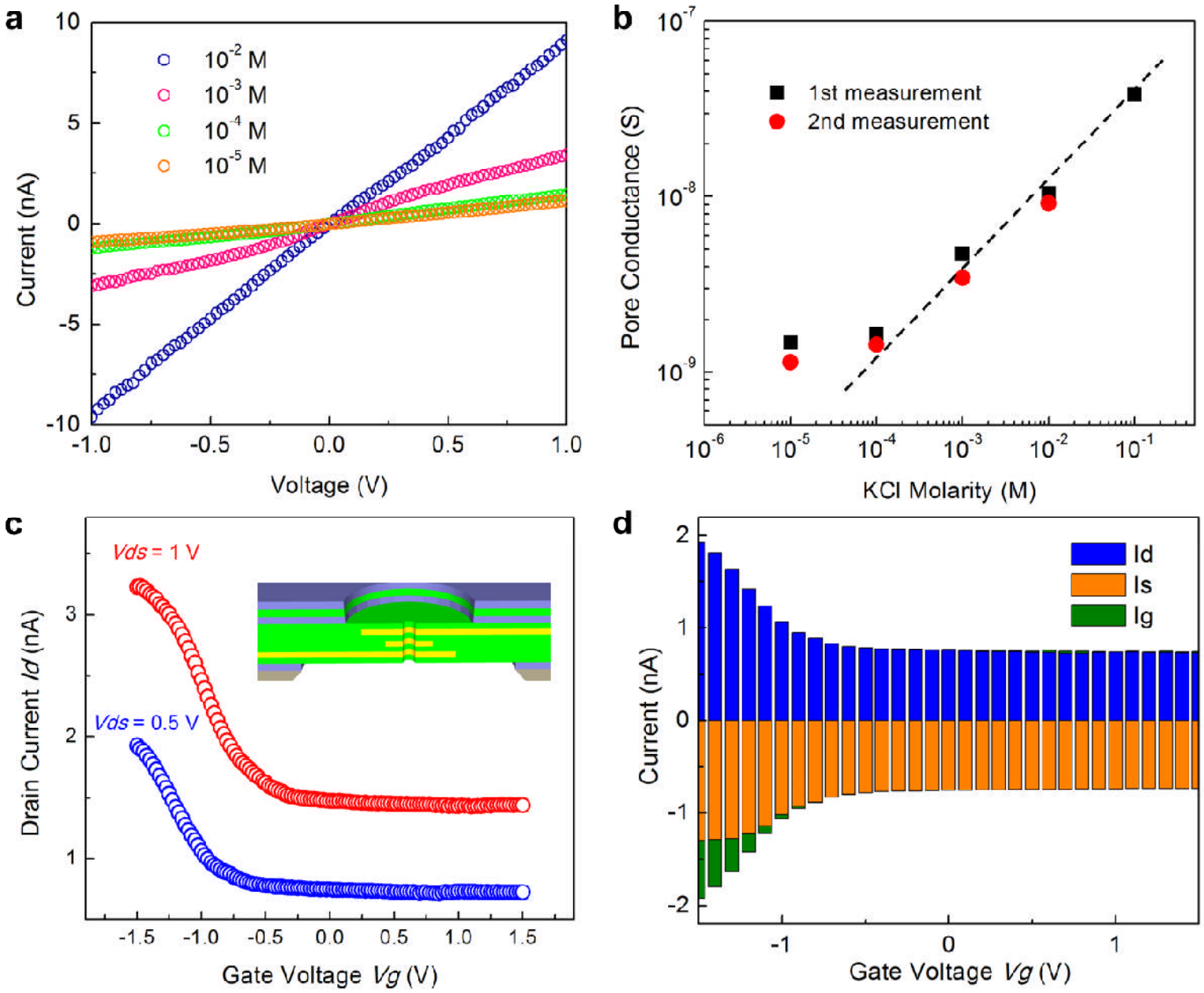

Figure 5