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Building a Fab on a Chip

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Abstract

Semiconductor fabs are large, complex industrial sites with costs for a single facility approaching $10B. In this paper we discuss the possibility of putting the entire functionality of such a fab onto a single silicon chip. We demonstrate a path forward where, for certain applications, especially at the nanometer scale, one can consider using a single chip approach for building devices with significant potential cost savings. In our approach, we build micro versions of the macro machines one typically finds in a fab, and integrating all the components together. We argue that the technology now exists to allow one to build a Fab on a Chip.

I. Introduction:

In this paper we discuss a novel approach to nano-manufacturing, using the so-called Fab on a Chip (FoC). As semiconductor technologies continue to shrink from the deep sub-micron regime into the nanometer regime[1], standard techniques to manufacture the devices are becoming increasingly challenging[2-5]. In spite of the fact that device physics is trending towards few or single atom devices, the conventional photo resist, liftoff, and optical/deep-UV/E-beam lithography techniques used in multi-billion dollar fabs show no potential for advancing into the single atom regime. Some approaches that address this concern are based on self-assembly[6]. In this paper we discuss a different approach by building a Fab on a Chip, a technique of directly depositing circuits and structures with atomic beams using small numbers of atoms or even single atoms under the control of a MEMS writing device[7]. We discuss re-creating all of the elements one finds in a VLSI fab on a single silicon chip and then using that system to directly fabricate nanoscale devices. In a very real sense, we are using macro-machines to build micro-machines and then using these micro-machines to produce nanostructures. Our approach advances manufacturing technology through the use of what is, in essence, a 3D printer at the atomic scale that allows us to assemble materials in a digitally programmable way. As we will show, this can be used for creating NEMS devices as well as electronic ones.

II. Background:

The basic and most fundamental idea of modern semiconductor processing is that of depositing or diffusing materials onto or into a silicon substrate with areas of the substrate masked off with various types of photoresists or other layers. While materials, deposition tools, lithography tools, etching tools, and lithography wavelengths keep changing, the basic fabrication technique remains the same; one deposits more material than is desired and then selectively removes the unwanted material. An extrapolation of Moore's Law[8] predicts that the industry is moving into the regime of single atom devices, where the standard manufacturing approach fundamentally breaks down. One answer to this technological challenge is a bottom up approach, inspired by biology, that relies on self-assembly and stochastic processes, as today's carbon nanotubes are grown[9]. Single molecule[10] and even single atom[1,11] transistors have already been manufactured and networks using carbon nanotubes to perform basic computational operations[12] have already been realized. For fabricating single atom devices there is no known method for depositing many atoms and then removing all but a single atom. If one wants only a single atom in a specific location on a silicon wafer, one will probably need a technique to be able to directly place the single atom. This paper discusses such an approach, the Fab on a Chip. It is illustrated how the

combination of MEMS devices can be leveraged to deposit as few as a single atom at a time within a well-defined area.

The technique is inspired by research done at Bell Laboratories in the mid 1980's by Bishop and Dolan[13]. Their work used static, nano-scale stencils and low temperature quench condensed evaporation. The advantages of directly evaporating at low temperatures (~77K or ~4.2K) are: a) higher purity due to a very good vacuum, b) excellent sticking of the deposited atoms, c) the ability to use a wide range of materials, including lithium and sodium, which are incompatible with conventional techniques and d) circumvention of thermal cycling from the fabrication process, which is known to cause creep, balling up, etc. in room temperature depositions. For *in situ* measurements this is particularly important as any change in temperature after deposition will result in a change of the material properties.

The approach we are proposing here is to combine low temperature, quench condensed evaporation with programmable dynamic MEMS stencils, *i.e*. the ability to directly write structures and patterns while evaporating in a controlled environment. Two technologies make our idea feasible: the extraordinary developments in MEMS technologies that enable aperture(s) to be moved with sub- nanometer precision and control[14] and the ability, using modern focused ion beam- and transmission electron- microscopes (FIBs and TEMs), to create nm-sized holes in silicon wafers[15]. Figure 1 shows an example of such a dynamic stencil controller. The basic idea is that one can write with a beam of atoms by using one or more sources to emit atoms while a MEMS plate follows a preprogrammed trajectory, tracing out a pattern. This approach has a number of advantages, including that it enables one to: a) turn the atom beam on and off quickly by using the fast thermal response time of the sources and/or an integrated shutter, b) create many devices in parallel by using arrays of apertures, c) deposit single or few atoms by using apertures on the order of tens of nanometers, d) control the size and shape of deposited structures by milling different size and shape apertures and by dynamically controlling the aperture location, e) deposit both insulating and conducting materials, allowing for the fabrication of complex interconnects and wire junctions, f) construct nano-mechanical devices, as well as electrical ones, and g) conduct the entire deposition in a cryostat, or other specialized environment. Finally, and most importantly, a single silicon chip that harbors all of the elements one needs for a Fab on a Chip can be created. By using a "system of systems" approach, one can construct complex evaporation setups with sources, writers, film thickness monitors, leads to the outside world, thermometers, heaters, and more, all on a silicon chip built inexpensively with high yield at an external foundry[16]. It is our belief that such FoC systems will be powerful basic research tools as well as foundational technologies for building a new class of nano-devices. As discussed in the supplementary materials, this process may even be

scaled beyond prototyping, and has the potential to allow one to build single or few atom devices in a semi-scalable way with high volumes, low costs and high yield.

For this work, the FoC devices are fabricated in a commercial foundry, using the MEMSCAP PolyMUMPS process[16]. Such an approach has many advantages. Commercial foundries allow for rapid cycle times (~2 months), high yields, and low development costs. Designing into a foundry also means that the high volume manufacturing issues are already solved. The same fab that built tens of devices can easily ramp up and manufacture thousands to millions, as needed. In principle, device designs can be used by different manufacturers and combined in unique ways. Starting from a set of well-characterized devices, complex systems can be created to complete a specific task very quickly. Though the results presented here are based on the PolyMUMPs process, there are, in addition to custom processes, other MEMS fabs that offer multi-user-runs[17] that can manufacture equivalent devices.

The PolyMUMPs process used in this work includes one static and two moveable silicon layers. For the system of systems described in the following section, three stacked layers are not sufficient for the complete integration of all components described. This could be overcome in multiple ways. For one, there is of course no fundamental reason that the fabrication is limited by three layers. For example the multi user SUMMiT V process offers a total of five device layers[17]. It should also be noted that although the PolyMUMPs multi user run only includes three layers, clever designs using hinges and springs can implemented to slide and fold layers resulting in larger stacks of mechanically active poly-silicon layers. One can also envision back-etching the writer dies to produce through-waver holes (as is already standard in SOI processes[18]). Subsequently, the writer dies would then be flip-chip-bonded onto a second die containing additional MEMS devices. This effectively turns the three layer process into a stacked six layer process. Although not yet implemented, we believe future dies, or die stacks, can incorporate all devices discussed, and more, on a single chip.

The capability of back-etching the writers and flip-chip bonding them onto a new die opens up the ability to place the writers on a large variety of substrates. Using this method one is no longer limited to writing on the nitride film intrinsic to the PolyMUMPs process, or restricted to using the poly-silicon layer for electrodes. In principle, flip-chip capabilities vastly expand where and how this lithographic tool can be implemented. Developing these capabilities is the focus of ongoing research.

III. FoC Sub-Systems:

A. A System of Systems

The idea behind our program is to use a "system of systems" approach where we take all of the elements of an evaporation system and ultimately integrate them onto a single silicon chip, the FoC. This allows for the design of complex systems using standard, reliable sub-systems that have already been optimized and whose performance is well understood. The use of a foundry to produce the various elements makes this an economical approach.

In essence, macro-machines are used to create micro-machines, which are then used to create nano-machines. The micro-machines we show here are created using a foundry process with minimum design rules of two microns. However, these machines can give us precision and control at the nano-meter level and using the techniques outlined here, allow us to build nm-sized devices and systems. As we will show, we have successfully built all of the elements of a FoC system including a lithography tool, micro-cells as sources, film thickness monitors, thermometers, heaters and shutters/masks. We plan to design a complete system, with all of these devices fabricated simultaneously on a die at the foundry. That way, each element is aligned with each other with micron precision. We ultimately need nano-meter precision and control. This comes from two techniques. The first is using micron-scale devices that move with nanometer precision and control and the second is using a FIB to cut nm-sized apertures.

We are creating a design library of atomic calligraphy tools, akin to modular electronics. An end user will be able to take our design files of robust devices with known and well-characterized properties and arrange them as desired on a die to be fabricated at a foundry. Using a FIB for post processing, users can conduct custom single or few atom experiments with great complexity and have the devices built in a foundry with high yield and at low costs.

B. MEMS Plates, Apertures, and Shutters as Writing Tools

B.1 Plates

The heart of our system is the writing plate that controls the beam of atoms as they are being deposited, acting like a dynamic stencil. The plate is attached by tethers to comb drives and folded flexural springs. It typically has a small aperture in its center ranging from ~10 nm to a few microns. The use of such plates as the lithography tool means that the evaporation is the last step in producing a nano-device and makes single atom devices possible. This technology can be contrasted to static[19, 20], dynamic[21], and AFM-based[22-24] stencil fabrication methods which also allow for resist free patterning of metals. It is the integration of multiple systems and ease of use in multiple settings that sets the purely

MEMS-based writers apart. AFM based Dip pen nanolithography[25] and oxidation nanolithography[26-28] are also related nanofabrication methods, but the applicability in terms of types of materials deposited as well as operational temperatures and pressures are very different.

Figures 1, 2 and 3 show the writing chip layout, including the aperture in the plate and the cantilever shutter. The MEMS die includes pre-positioned leads that electrically connect the written structures to the outside world; these are discussed in more detail below. The surface that our structures are written on is an insulating layer of silicon nitride. The plates containing the apertures are roughly 100x100 μm^2 and 1.5 or 2 μm thick. The plates are attached by long tethers to comb drives, allowing them to be moved in the plane of the silicon wafer. Typical displacements are up to 15 μm in each quadrant of the Cartesian plane. Actuator combs, springs, tethers and pre-deposited electrodes must be shielded from the atomic flux to prevent electrical shorting of the device. When placed in a macro thermal evaporator protection is ensured by adding a cover to the ceramic DIP package with a ~100 μm diameter aperture centered over the plate. When using the micro-sources the material deposited is not sufficient to impact the electro-mechanics of the writers.

To operate the linear actuator, a voltage is applied to the capacitor of the comb drive. The outer combs are attached to the substrate and do not move. The inner combs are held at ground potential, and are suspended by folded flexure springs, allowing them to move when a voltage is applied between the combs. As capacitor plates can only exert attractive forces, one needs matched sets of comb drives to move the plate in positive and negative *x* and *y* directions. Each of the four comb drives provides the actuation force, balanced by the spring constant of two folded flexure springs and orthogonal tethers. The electromechanical transfer function is given by

$$x_i = \frac{1}{2k_i}\frac{dC}{dx_i}V^2, \qquad (1)$$

where x_i is the displacement, k_i the spring constant, and $\frac{dC}{dx_i}$ is the differential capacitance of the actuating comb along the i^{th} axis. For comb drives the differential capacitance is a constant ($\frac{dC}{dx_i} = \epsilon_0 \eta N \frac{t}{g}$, where N is the number of combs, ε_0 is the permittivity of free space, t and g is the thickness and gap separation of the comb fingers respectively, and η is a numeric factor of order one accounting for the fringe fields), resulting in a linear displacement versus voltage squared relationship. The electromechanical response can be calibrated using optical techniques based on digital image correlation (see electronic supplementary information (ESI) for a full description of the method used). By fitting data to equation (1) one obtains electromechanical coefficients that define the response. A typical result is $\frac{1}{2k_i}\frac{dC}{dx_i} = 1.41 \pm 0.01$ nm/V^2, which means that for an actuation voltage of 10 V with 1 mV of voltage noise the plate is moved by 141 nm

with a voltage induced error of ~0.03 nm. With an actuation of 100 V and 1 mV of voltage noise the plate moves 14.1 μm with an accuracy of ~0.3 nm. The high frequency and quality factor of the MEMS device suppresses mechanical noise from the environment which falls off as $1/f$ [29]; we estimate that even without vibration damping the mechanical jitter is on the order of tens of nm[7]. Future experiments in temperature and vibration controlled environments will further improve these results.

The plate position in the *z*-axis can also be controlled, both by using the levitation effect observed in comb drives[30] and by snapping it down by applying a voltage to the degenerately doped substrate just below the insulating silicon nitride. As we have shown[7], such *z*-control modifies the geometry, allowing for significant amount of adjustment in the diameter of the spot size.

B.2 Creating Apertures using a FIB

The writing is done with one or more apertures in the center of the plate, allowing for the deposition of single devices or arrays of identical devices with a single die. Figure 2 depicts examples of different types of apertures, customized for the fabrication of a specific design. Examples of written structures are shown in Figures 4 and 5.

The MEMS foundry process used to create the writing structures has minimum design rules of two microns. The apertures define the pixel size of the writer, and thus to obtain deep submicron structures, the apertures must be correspondingly small. This is achieved using two complementary approaches.

As depicted in Figure 2, we use a FIB to create a two-step aperture. In the first step, a roughly 4x4 μm^2 region of the 1.5 μm thick plate is thinned to <400 nm. The FIB is then adjusted to lower currents (and smaller beam sizes), and the ion beam is used to poke through the remaining silicon and form the aperture. The stacked approach reduces the aspect ratio of the final aperture, which improves the resolution and reduced fabrication time. At this point, the MEMS is still embedded in silicon-oxide, preventing both unwanted drift or vibration as well as protecting the nitride canvas (see ESI for the PolyMUMPs fabrication outline). A close-up image of a ~100 nm aperture is shown in Figure 2 a), demonstrating the control provided by the FIB. Figure 2 also includes examples of b) arrays, c) aperture shutter systems, and d)-f) more complex patterning for custom applications.

As a result of atom surface mobility[19], after the holes have been milled they can be partially filled in by depositing gold onto the MEMS plate. Using this effect, we have previously demonstrated how to controllably narrow a nominally 204 nm diameter hole to down to 59 nm [7]. We believe it will ultimately be possible to create holes roughly 10-30 nm in diameter. During operation, we do not expect the filling up of the apertures to be a limiting factor because many different apertures, with a wide range of sizes and shutters

can be arranged, so that only one aperture is used at a time. The integrated approach allows one to uncover a clean aperture as needed. Aperture cleaning methods, based on local heating, have been demonstrated in stencil lithography systems[31]. While currently untested, the writer geometry used allows for heating of the central plate, and may be leveraged to extend the aperture life. It is expected that the ability to clean the apertures becomes particularly important for the smallest apertures. The method is expected to work best with low temperature evaporation sources such as indium, lead or lithium.

For holes smaller than 10 nm a TEM could be used. More complex plates with low stress nitride thin-film windows can be manufactured, through which the aperture is drilled post release[32]. Feedback control of this process can result in nano-pores in the few nanometer diameter range[33]. For this to be realized, two additional fabrication steps need to be implemented. First, the PolyMUMPs process described here needs to be expanded to include nitride deposition. Placing such a layer on top of the plate creates the opportunity for manufacturing apertures in much thinner windows, with thicknesses on the order of 40-100 nm. Second, a Deep Reactive Ion etch step can be added to back-etch the wafer. After the standard release step, this results in a free standing nitride membrane typically used for TEM nano-pore drilling. The writers would then be used in a flip-chip configuration.

B.3 MEMS Shutters for high Speed Aperture Selection

Simple devices can be written using one plate with one aperture. Devices with an integrated shutter, such as shown in Figure 3, can also be manufactured. This cantilever style shutter functions as an "on-off" switch for the atom flux. Other MEMS shutters, based on similar stacking of device layers, can be implemented. Alternatively, SOI based shutters or irises[34] could be integrated with the writer by flip chip binding. In its simplest implementation the shutter response time is on the order of the transient time of the resonant mode, given by $\tau = \frac{Q}{2\pi f_0}$. Quality factors are on the range of 10^2-10^4 and the shutter resonance frequency is on the order of 5 kHz, resulting in transient times of $\tau = 2 - 200$ ms. By including active feedback mechanisms, the shutter response time can be reduced considerably below the transient time[35]. Opening or closing an aperture can occur much faster by simply placing the shutter close to the aperture edge, for which case the transition can occur on the order of 10 μs [7]. Stacked plate designs function as a more complex shutter that can move in the same plane as the writer plate to select from multiple apertures. The size and speed of the shutter allows for the deposition of single atoms. For example, given a 100 nm-sized hole and evaporation rates of one monolayer per second, roughly 10^5 atoms per second are transmitted on average through the aperture. The 10 μs response time of the shutter is fast enough to stochastically allow only one or a few atoms to pass. It should be noted that the number of atoms can be of order one, but the placement

accuracy is defined by the area of the aperture and the position control of the writers. The MEMS plates themselves can typically be moved at speeds of ~1 m/s, hence when travelling in opposite directions the shutter-aperture system can be open for roughly as little as 100 ns, through which only 0.01 atoms would pass on average. In addition to enabling single atom placement, two plates with apertures also allow for the velocity selection of the atoms in a particular range of speeds. This may be achieved by timing the overlap of the apertures in each plate and using the time of flight of the atoms between plates as a velocity filter (see ESI for details).

B.4 Examples of Structures Fabricated

Examples of structures we have written are shown in Figures 4 and 5. Figure 4 shows a roughly 200 nm nano-bridge as well as three "3D" lines written with the MEMS writer. This demonstrates the ability to produce NEMS devices.

The NEMS bridges were manufactured in a two deposition process. Initially a gold sacrificial layer was deposited through a shadow mask depicted in Figure 2 f). During this evaporation the shutter protected the second, perpendicularly oriented apertures. Subsequently, the chromium device layer was evaporated through the unobstructed apertures, now positioned above the gold traces. The release was accomplished using a gold wet-etch, removing the sacrificial layer. Since the gold must be etched away, in this example deposition is not the last step of the fabrication process.

In Figure 5, an experiment is shown where an array of gold "BU"s are printed. For this deposition the writer was swept line by line, akin to a typical printer. This demonstrates the high level of positional control that we have using our writing plates. Other modes of operation follow a continuous line or, when using a predefined stencil the writer is moved to set points and then held steady while the metal is deposited (examples are illustrated in Figure 4). Further examples, including a demonstration of the functionality of the shutter is given by Imboden *et al.*[7].

C. Atomic Micro Sources

So far we discussed a method for resist free patterning by controlling the location of an atom flux. Here we present a possible MEMS-based source of such a flux. The micro-source is able to controllably provide the materials needed for nanofabrication. Examples include MEMS spray source[36] and picoliter dispensers for inkjet printing[37] and wet nano-fabrication[38]. The PVD approach presented here is based on thermal evaporation from a silicon micro-hotplate.

MEMS micro-plates can be uniformly heated in milliseconds to the temperatures needed

to evaporate a large range of metals and compounds. Such sources are shown in Figures 6 and 7. The center filaments range from 50x50 to 150x150 μm² in area and are suspended off the substrate. Narrow attachments provide the necessary mechanical stability and electrical properties. When a current is applied, the attachment points act like heaters. As shown in the simulation depicted in Figures 6 b) and c), the symmetry of the tethers and thermal isolation of the plate results in temperature uniformity at 1000 K of ~8 K while typically consuming only 50 mW. Blackbody radiative cooling make the plates more uniform in temperature because the T^4 dependence of the emitted power means a higher power density radiates from the hotter regions than the cooler ones. With radiation effects, the plates are expected to be isothermal to within ~4 K across their area.

Figure 6 d) depicts a measurement of the thermal response time of two plates. The voltage across the plate is recorded as the heating power is turned off. The exponential decay in voltage is a result of the temperature-dependent resistance. The time constants τ = 5.23 ms for the 150 μm plate and τ = 0.70 ms for the 50 μm plate are extracted from the plots. The thermal response time dictates the rate at which we can modulate the temperature of the plate and hence the on-off speed of the atomic flux.

Knowing the thermal characteristics of the micro source, we can calculate the atomic flux using the Hertz-Knudsen equation[39]:

$$J(T) = \frac{\alpha\,|P(T)-P_0|}{\sqrt{2\,\pi\,m\,k_B T}}. \qquad (2)$$

J(T) is the number of atoms per unit area per unit time entering the vapor phase, α is the sticking coefficient, P_0 is the partial pressure, and *P(T)* is the vapor pressure at temperature *T*. The vapor pressure is calculated using the Clausius-Clapeyron equation and empirically determined constants[40, 41] and making the common assumption that the sticking coefficient is one. Figure 6 c) depicts the predicted gold flux evaporating off a MEMS plate that is heated to 1000 K. The ESI Figure (S5) shows the atomic flux as a function of temperature for zinc, lead, indium, gold, iron, and silicon for partial pressures ranging from 0 to 10^{-5} Torr. All these metals can be used to generate fluxes on the order of monolayers per second at temperatures well below 1683 K, the melting temperature of the polysilicon plate. For example, gold at a nominal temperature of 1400 K generates a flux of ~4×10^7 atoms/s-μm². Accounting for geometric effects, a 150 × 150 μm² source would produce a flux of ~10^7 atoms/s-μm², or one monolayer per second, at a distance of 150 μm from the source. The high temperature sensitivity of the flux makes it difficult to predict evaporation/deposition rates unless a high accuracy temperature measurement can be made. Furthermore, as seen in the Figure (S5) of the ESI, the partial pressure imposes a cutoff to the lowest flux that can be obtained. For gold at a partial pressure of $P_0 = 10^{-6}$ Torr, this corresponds to a flux rate of $J(T = 1300\ \text{K}) \approx 4\times10^6$ atoms/s-μm². Not surprisingly, ultra-high vacuum as is typically found in a cryostat, is needed when working with a low number of atoms.

For most metals the vapor pressure is sufficiently high that the partial pressure can be set to zero; this approximation is especially valid in a cryostat.

The low numbers of atoms desired make it possible to thermally evaporate materials typically not possible in macroscopic systems. If we consider the list of elements that can be evaporated at rates of at least 1000 atoms/s-μm^2 at temperatures below 1683 K the elements included are Zn, Mg, Li, Sr, Ca, Tl, Ba, Pb, In, Mn, Ag, Ga, Be, Al, Cr, Rh, V, La, Ti, Co, Pd, Ni, Fe, Au, Nd, Cu and Sn. One does not normally think of many of these elements as being able to be evaporated using resistive-heating, but if one is only interested in tens to thousands of atoms, the phase space of useable elements opens up considerably. It must be noted that, in addition to the vapor pressure, the reactivity of the materials sourced must be taken into consideration. For example, gold forms a eutectic with silicon at 643 K [42]. The silicon may be chemically incompatible with a number of desirable materials. Further studies are underway to determine surface passivation techniques, such as growing a thin layer of silicon-oxide on the plate. Alternatively, adding a barrier layer made of an inert metal like tungsten to form tungsten disilicide[43] should enable a wide range of materials to be compatible with this setup.

For operation, films of the materials to be evaporated are pre-deposited onto the square structures. This can be achieved using a shadow mask, lithography, or, due to the overhang from the MEMS fabrication technique used, an entire wafer can be coated without shorting out the devices. As the resistivity increases with temperature (see section E) the devices are voltage biased, applying powers in the range of 5-25 milliwatts to obtain temperatures beyond 1000 K. Unlike a serpentine structure, the plates, heated by two symmetric point contact sources, show a uniform temperature over a large surface area, and are hence ideally suited as a controlled atomic flux source.

Figure 7 shows our micro-sources in operation. The source was placed in an SEM and the images shown were taken as indium was melting and subsequently evaporating off the hot silicon filament. In Figure 7 a), corresponding to time t = 0 s and T = 293 K, the polysilicon plate is loaded with a uniform layer of indium, approximately 315 nm thick. When the plate is resistively heated, b) the indium melts and balls up (t = 150 s, $T \approx$ 430 K) and c) evaporates until d) the indium is exhausted (t = 1253 s). Between b) and c) the power is ramped from $P \approx$ 11 mW to $P \approx$ 27.5 mW. A time sequence video of the evaporation is included in the ESI, and Figure (S6) depicts the power applied over time. Based on the surface area of the plate and the time taken for the indium to evaporate , it is estimated that the flux is on the order of $J \sim 10^9$ atoms/s-μm^2, corresponding to a MEMS source temperature of $T \approx$ 1100 K. Once the applied power exceeds 32 mW the heaters fail. There is evidence that the failure occurs at temperatures below the upper limit of 1683 K, thought to be the result of cracking due to thermal stresses. It is worth noting that only the source gets hot; the indium on the cold substrate does not ball up or evaporate. This makes

'loading' the source easier and minimizes the power requirements.

Since only the square plate gets hot, the micro-sources are a well-defined, almost point source of atoms. This is quite compatible with integration in a FoC. One could imagine tilling areas of a chip with many such sources, loaded with a variety of materials on them, creating a programmable atom generator. The data shown in Figure 6 d) indicates that their response time is such that one can turn these sources on/off in milliseconds, enabling another method for controlling the atomic deposition in addition to the integrated MEMS shutter. Multiple sources evaporating simultaneously allow for alloys and phase spreads to be created.

Low atomic flux numbers, yet high vapor pressures for enhanced flux control can be obtained by reducing the area of the metalized source. For example, the flux of gold atoms at a temperature of 1300 K and a partial pressure of $P_0 = 10^{-6}$ Torr is $J(T = 1300\ \mathrm{K}) \approx 4 \times 10^6$ atoms/s-μm^2. If only a 6 × 6 μm^2 area of the source is metalized with gold, the flux rate is 1.4×10^8 atoms/sec. Assuming that the source would uniformly coat the surface of a sphere above it, as in a Knudsen cell, the geometry factor reduces the flux to ~ 2000 atoms/s-μm^2 at a distance of 150 μm above the source. Placing one of our shutters with a 100nm aperture at a distance of 150 μm from the source would allow only one atom to pass through every 60 ms. As this time scale exceeds the thermal time constant of the source (~5 ms) by over an order of magnitude, one can modulate the applied power and use it as an on/off switch for the evaporation of single atoms.

Combining the small evaporation rates, narrow apertures, fast shutters and modest distances will enable the use of micro-sources and shutters to manipulate single or a few atoms at a time. A critical development component is a method to directly measure and control the temperature, corresponding to an atom flux, with high precision. One approach is to use the resistivity of the plate as a thermometer; this is considered in section E. Alternatively, the flux generated can be monitored using MEMS mass sensors such as those discussed in the following section.

D. Mass Sensor - Film Thickness Monitoring

D.1 MEMS Oscillators as Mass Sensors

A crucial element for any evaporation or deposition system is a film thickness monitor/mass sensor. So far, the MEMS discussed in this work are actuators and sources, devices that can manipulate the environment to produce a desired outcome. However, MEMS technology is most often used for sensing. Examples include magnetometers[44], chemical sensors[29, 45], inertial sensors, and pressure sensors[46]. Here we demonstrate using MEMS for mass sensing and, in the following section, we present MEMS thermometers. The

speed, sensitivity, and ability to be integrated on chip makes this an attractive approach. MEMS mass sensors have already been realized; examples include arrays of CMOS integrated sensors with femtogram resolution[47] as well as functionalized resonators for biological sensing with pg/fg resolution[48, 49]. We demonstrate resonators with an estimated 3 fg mass sensitivity, manufactured by the same fabrication process as the writers and sources. The sensitivity levels are ideally suited for the FoC applications considered and the sensor can be integrated on chip with micron alignment accuracy.

An example of a mass sensor we have built based on MEMS principles is shown in Figure 8 a). Figure 8 b) includes a finite element simulation of the fundamental mode occurring just below 40 kHz. The mass is dominated by the octagonal plate in the center. Eight springs are arranged around the edges and covered by the tan structure around the perimeter. The print-through from the manufacturing process makes the underlying springs visible. Similar square plate designs with four springs and resonance frequencies ranging from 40 kHz to 200 kHz have been tested. The cover is needed to protect the springs from the atom flux. This ensures that the deposited atoms only add mass to the resonator and do not affect the restoring force. As a result the change in the resonance frequency is purely due to the added mass and not dependent on other properties, such as elasticity, of the deposited material. The frequency can be monitored in a closed loop setup with an accuracy of < 1 part in 10^8. The shift corresponds to the mass loading according to

$$\frac{\Delta f}{f} = -\frac{1}{2}\frac{\Delta m_{eff}}{m_{eff}}, \qquad (3)$$

where f is the resonance frequency and m_{eff} the effective mass of the resonator, described in the ESI.

The resonator is driven and detected capacitively and can be modeled as a damped driven harmonic resonator[50]. The resonator plate forms one capacitive plate and an underlying electrode separated by 2 μm forms the second capacitive plate. Open loop frequency sweeps are used to characterize the Lorentzian response of the resonators and measure the quality factor, typically found in the range of 10^4-10^5 in high vacuum environments. When operating as a mass sensor, a lock-in amplifier is used in a closed loop setup. This allows the frequency to continuously adjust to the added mass while the resonator is driven in phase. A frequency counter keeps track of the resonance (a circuit diagram is included in the ESI). The added material does not contribute to the spring constant of the device. This assumption holds as: 1) typical deposition materials like gold have a much higher density and lower Young's modulus than silicon, hence the mass effect is much larger than the mechanical stiffness effect; 2) the spring constant is mostly determined by the folded springs, which are unaffected by the mass added to the center plate; 3) for typical thicknesses deposited, the film is not continuous due to the rough

surface of the polysilicon resonator. A measure of the frequency stability of an oscillator, and hence mass sensor accuracy, is given by the Allan deviation[51]

$$\sigma_f(\tau) = \sqrt{\frac{1}{2N}\sum_{n=1}^{N\to\infty}\left(\bar{f}_{n+1} - \bar{f}_n\right)^2}. \quad (4)$$

τ is the averaging time for each measurement; $\bar{f}_n$ is the average value of the n-th measurement. We find $\sigma_f(\tau = 0.5\ s) = 5.1$ mHz, as discussed in the next paragraph, this corresponding to a mass change of 25.4 fg, or order 10^{-4} monolayers of gold atoms per second. The lowest Allan deviation measured was $\sigma_f(\tau = 10\ s) = 0.5$ mHz, corresponding to a mass sensitivity of 2.5 fg. (see ESI for details.) This is better than the required sensitivity of order one monolayer per second, needed for single atom experiments.

The mass sensor is calibrated in a standard thermal evaporator. Using an Inficon thickness monitor the deposition is recorded independently of the frequency shift. The results are plotted in Figure 9. For the mass loading, it is found that $\Delta f/\Delta m$ = 201.1 ± 0.1 Hz/ng. The metal deposition will also change the temperature of the MEMS device and introduce a frequency shift due to the change in the Young's modulus[52]. To take this effect into account, the temperature is cycled without adding mass. The temperature dependence of 1.8Hz/K, plotted in Figure 9 c), is used to subtract out thermal effects by measuring changes in temperature during evaporations. This function can also be accomplished using on-chip silicon thermometers as discussed below. While the relative change in mass can be determined with high precision, the absolute mass sensitivity is limited by the calibration accuracy, which is on the order of 1% using the Inficon crystal.

State of the art NEMS devices have reached single atom mass sensitivity[53]. While this level may not be achievable using MEMS structures it is believed that there is still room for orders of magnitude improvements resulting in sensitivities on the order of 10^4-10^5 gold atoms. Given that we are targeting evaporation rates of a monolayer/sec for our experiments, we currently have ample sensitivity for our experiments. In operation, this device will be used to measure both the evaporation rate and the total number of evaporated atoms emitted by the micro-source cells. By using the mass sensors in high flux areas and considering geometric factors such as aperture size and distance from the source to the aperture, it will be possible to generate flux and monitor rates of a few atoms per second per aperture, and hence to fabricate structures comprised of single or few atoms.

D.2 Film Thickness Monitoring

The MEMS mass sensor can be used to monitor the flux generated from the micro-sources. It should be noted that the sensitivity of conventional, macroscopic thickness monitors is not sufficient to detect the small amount of mass coming off the micro-source.

However, the MEMS based mass sensor is ideally suited to operate in this parameter space. Figure 10 depicts the power applied to a micro-source, loaded with indium that is facing a MEMS mass sensor with a 1 mm gap between them. The changing frequency is recorded, corrected for heating effects, and the corresponding mass is determined. The results clearly demonstrate the mass transfer from the source to the sensor and provide a proof of concept for both devices. The derivative of the mass plot can be used to estimate the temperature of the hot plate. The rates measured are consistent with plate temperatures of 928 - 1009 K (see ESI for details). Further studies of the sources are needed to fine-tune the process and improve control.

In an actual setup, the mass sensor can be placed on the same die as the writer, thereby allowing measured change in mass to be directly converted into a corresponding deposition thickness on the writer. This would be the most common setup when using macro sources. Alternatively, the mass sensor can be placed on a different plane compared to the writer. This may be desired when using the micro sources. To increase the sensitivity, the sensors can be placed in close proximity to the sources. Geometric effects must be taken into account to determine the resulting flux. Such calibration is analogous to the empirical determination of the tooling factor typically needed in macroscopic evaporators.

E. On-Chip Thermometers/Heaters

Controlling the substrate temperature is crucial for manufacturing purposes as well as in experiments conducted using the fabricated nano-structures. Therefore both heaters and thermometers are needed, an example of which is depicted in Figure 11.

A material's temperature coefficient of resistance, ξ, characterizes the relative resistance (or resistivity) change with respect to changes in temperature and is expressed as

$$\xi = \frac{\Delta R}{R}\frac{1}{\Delta T}, \quad (5)$$

where ΔR is the change in resistance due to a change in temperature of ΔT and R is the resistance at the reference temperature. High levels of doping, as in the polysilicon used here, results in a positive coefficient[54], and a linear relation is measured for temperatures ranging up to 900 K[55]. The increase in resistivity with increasing temperature is a result of the phonon scattering of the charge carriers that occupy the conduction band. It has been reported that the resistivity of *n*-type doped polysilicon tends to drift at temperatures above 500 K as the dopants diffuse into the grain boundaries[56]. For high temperature applications this may be a concern, and a process using *p*-type dopants such as boron should be considered.

Figure 11 depicts resistance–temperature measurements of the device illustrated in the inset. A four terminal measurement setup enables resistance measurements accurate to four significant figures with standard multimeters. From the linear fit the relation $\Delta R/R = 1.1500\text{x}10^{-3} \pm 0.0002\ \text{K}^{-1} \times \Delta T$ is found. This is smaller than the temperature coefficient of resistance of many metals, including platinum, which is used as a standard[57]. The structures presented here can be used as both thermometers and heaters (one device for each function). Where the thermometers use the resistivity as a measure of temperature, the same structure can be used as a resistive heater. Typical room temperature resistances are on the order of 300 Ohm. Consequently for 1 Watt of power, the devices must be biased at a potential of 17.3 V.

One of the many advantages of these devices is that the strong thermal coupling between the thermometer/heater and the substrate allows for accurate measurements, as well as rapid response times. The dopant mobility may be a limiting factor when using the resistivity for thermometry of the MEMS evaporators. The die as a whole is not significantly heated above room temperature during device fabrication, and the experiments envisioned tend to be at cryogenic temperatures. As the calibration data shows, the thermometer performs linearly down to 100 K. Depending on the measurement setup, temperature sensitivities of 10 mK should be readily attainable. Other on chip methods to precisely measure the temperature can be implemented. For example, the known temperature dependence of the frequency shift[58] (and as discussed above) or quality factor[59] of a micro resonator can be used for millikelvin sensitive measurements, albeit requiring a considerably more complex measurement setup than for straight forward resistance measurements.

F. Connecting to the Outside World

To make the fabricated nano-devices electrically accessible, polysilicon leads are integrated on the die. The ends of these leads are close to the center of the canvas and within reach of the writer's apertures. Conductive metal traces can be traced from the poly leads to the nano-structures. In practice, one may first write the nano-structure and then use larger apertures to electrically connect the device to the poly leads. This would all occur during the same deposition session without breaking the vacuum or cycling the temperature.

Platinum pads are added to the end of the electrodes to improve the electrical contact. These "access points" are manufactured using the FIB, during the same fabrication step during which the apertures are milled. The FIB first mills the surface of the silicon to remove any silicon oxide contamination and is subsequently used to deposit the platinum pads. The platinum pads are important in three aspects: 1) to seal the polysilicon from

being oxidized[60]; 2) to provide better electrical contact between metal lines and polysilicon leads[61]; and 3) to create a smooth transition from the 500 nm thick leads to the nitride canvas. Removing the surface contamination and sealing the poly leads with the platinum are all accomplished in a single processing step.

Figure 12 shows two examples of such sets of leads. In one case (Figure 12 a)), a static stencil mask is used to deposit a four probe structure over the leads. Figure 12 b) shows a structure fabricated with a moving aperture that connects two sets of poly leads with FIB deposited T-shaped platinum pads. For both depositions the die is cooled to 84 K, which suppresses surface diffusion[62], resulting in smoother traces. The polysilicon electrodes each have a resistance of ~ 1.6 kOhm. The contacts are sensitive to the deposition parameters[63] as well as temperature, resulting in a diode-like behavior. Two probe measurements indicate a total circuit resistance on the order of 5 kOhm. Details, including *I-V* curves, are included in the ESI Figure (S12).

These experiments demonstrate that the writer can be used to make nano-structures and the prefabricated electrodes can be used to actuate as well as probe the fabricated devices. This enables experiments to be conducted with the deposition as the final fabrication step, followed by *in situ* measurements. Work still needs to be done to improve the contacts, where low impedance ohmic properties are desired. One may also imagine non-contact coupling to the fabricated structures using magnets, capacitively, or even optically, enabling multiple experiment methodologies. As mentioned previously, through-hole backside etching and flip-c hip bonding methods can be used to place the writers above electrodes and pre-existing circuits of far greater complexity than allowed by the PolyMUMPs process alone. Integrating this technology will greatly expand the capabilities of this technology.

IV. Conclusions and Outlook

In this paper we have presented a methodology for creating a fully integrated “Fab on a Chip”. We demonstrated all of the functioning elements needed to allow us to create micro-scale factories for producing single or arrays of nano-scale devices. The heart of the approach is based on a dynamic stencil with FIB apertures for resist-free patterning of deep sub-micron structures. In addition to the writers, MEMS based shutters, atom flux sources, mass sensors, and, thermometers are presented. The results presented here demonstrate the precision and control with which FoC systems can produce nano-scale devices. It is argued, how combining multiple micro-machines will enable patterning with individual atoms. This deterministic, top-down fabrication method is proposed as an economical method to create custom nano-devices.

This technology will enable the device fabrication made of quench condensed films at

cryogenic temperatures. It should be noted, that while the intrinsic nitride substrate may not be particularly clean, pre-depositing a buffer layer or using flip-chip methods described above may allow significant control of the target substrate upon which the nanoscale fabrication occurs. Furthermore, the low thermal-mechanical and -electrical noise provides an ideal setting for experiments, such as electron transport studies. Predefined polysilicon electrodes provide electrical access to the fabricated structure for *in situ* measurements. It is demonstrated how only three layers (one static two free) can be combined in practically limitless ways to actuate, sense, and probe with extraordinary sensitivity.

We believe that such Fabs on a Chip may be a viable technique for both prototyping and large scale, nano-manufacturing. Such novel approaches are required to ensure the continued validity of Moore's Law, and are hence both of scientific and economic interest.

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Notes

Electronic Supplementary Information (ESI) available: Experimental details and methods. See DOI: 10.1039/b000000x/

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Images

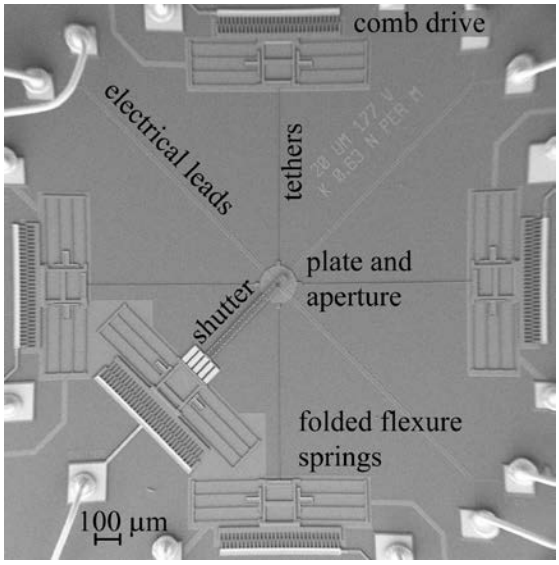

Figure 1. Top down SEM image of writer structure and shutter. The center plate can be actuated by four comb drives to cover an area of 30x30 μm^2.

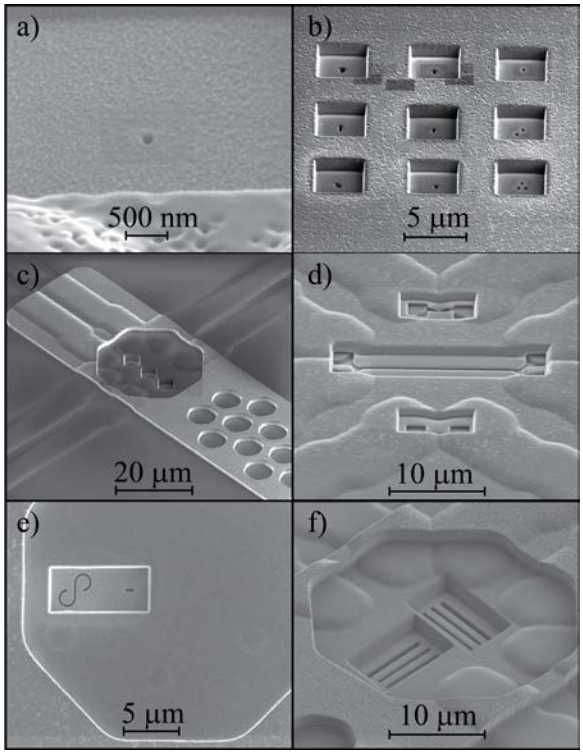

Figure 2. SEM images of apertures fabricated using a FIB.

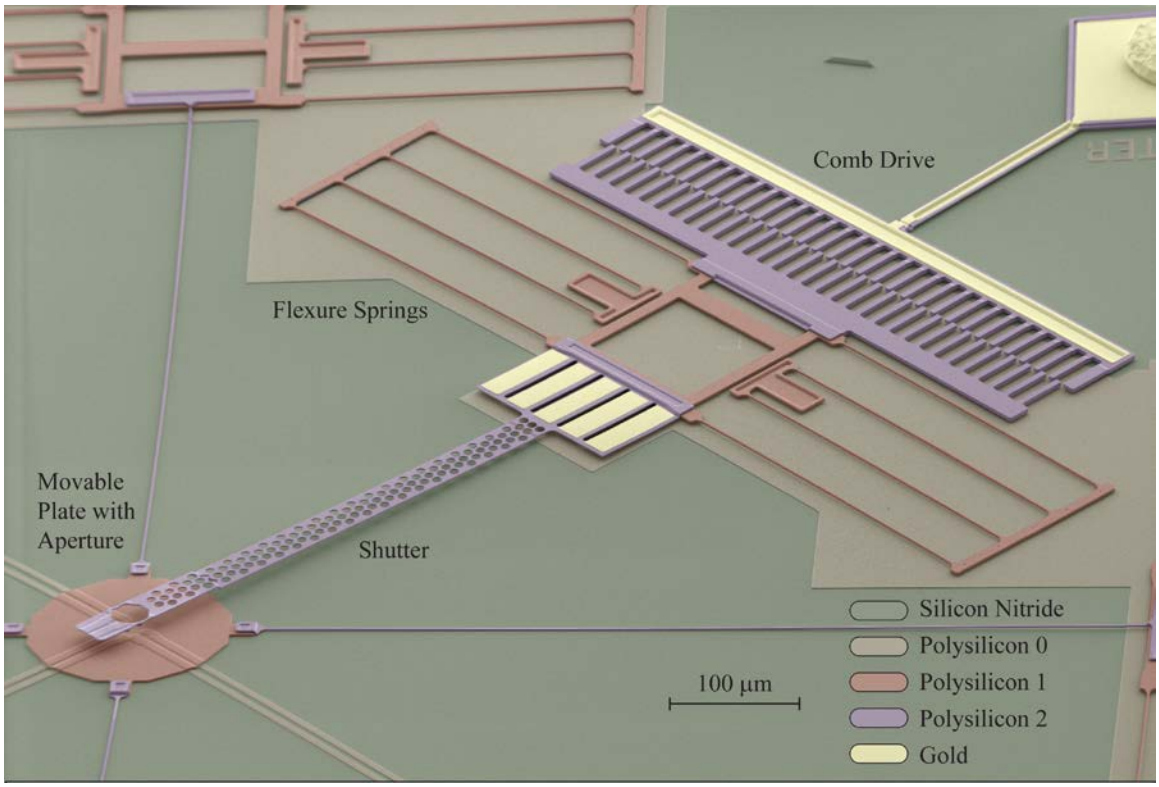

Figure 3. False color SEM micrograph of a writing plate and overhead shutter (lower left hand corner), the comb-drives that move them and the pre-positioned doped polysilicon leads for making contact to the fabricated structures are also visible. (Reprinted and adapted with permission from Imboden *et al*[7].)

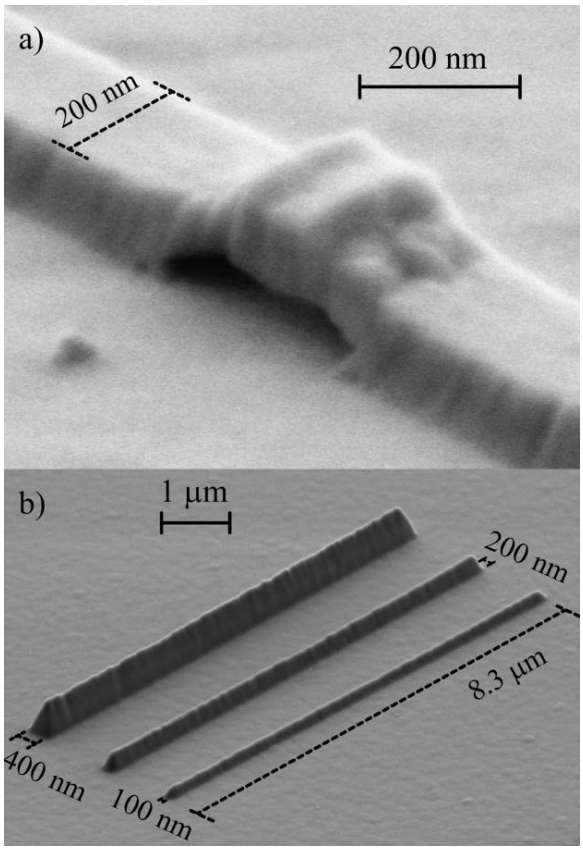

Figure 4. NEMS structures fabricated using the MEMS writers. a) ~200nm nano-bridge. b) Set of 3D lines. All structures are made of chromium.

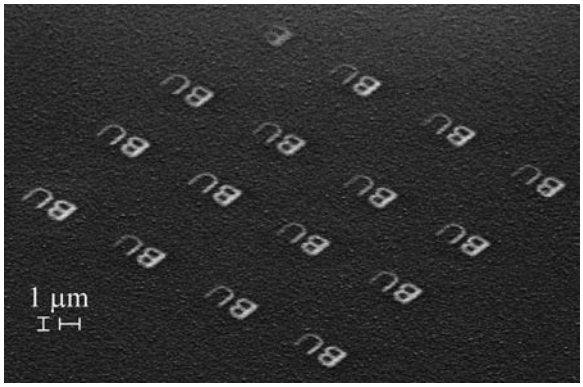

Figure 5. Array of patterns deposited using the writers. The structures are made of gold, the image is taken with the SEM stage at 50 degrees tilt.

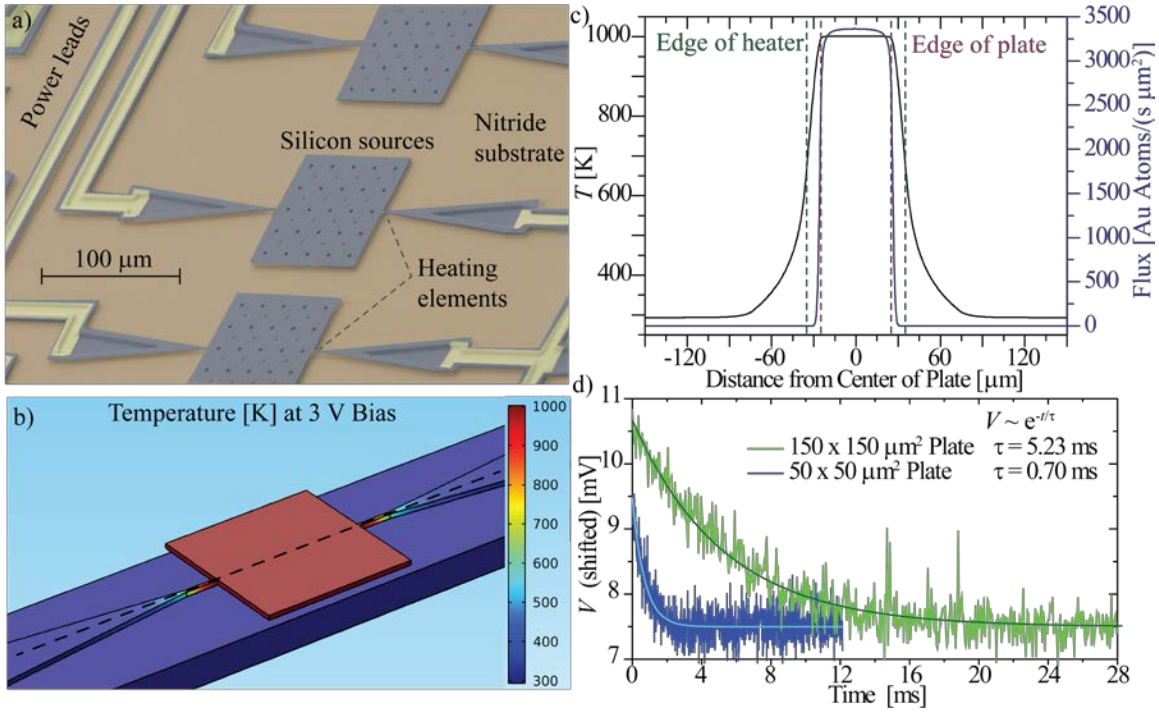

Figure 6. MEMS PVD a) False color SEM image of micro-evaporation sources. b) Finite element simulation of the temperature profile across the source and heaters. c) Temperature and calculated atomic flux of gold along the dotted trace of b). d) Measurements of the thermal time constants for two plate sizes.

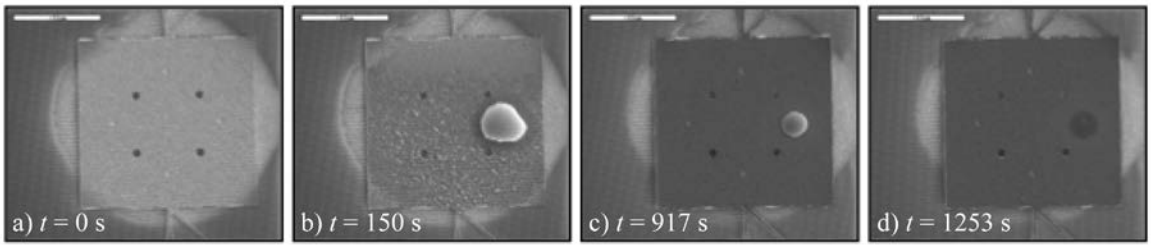

Figure 7. Micro-sources observed in an SEM as indium is evaporated from its surface. In panel a) the plate is at room temperature, fully loaded with indium. b) The indium melts and c) evaporates until d) the metal is exhausted. The scale bar in each figure is 50 μm.

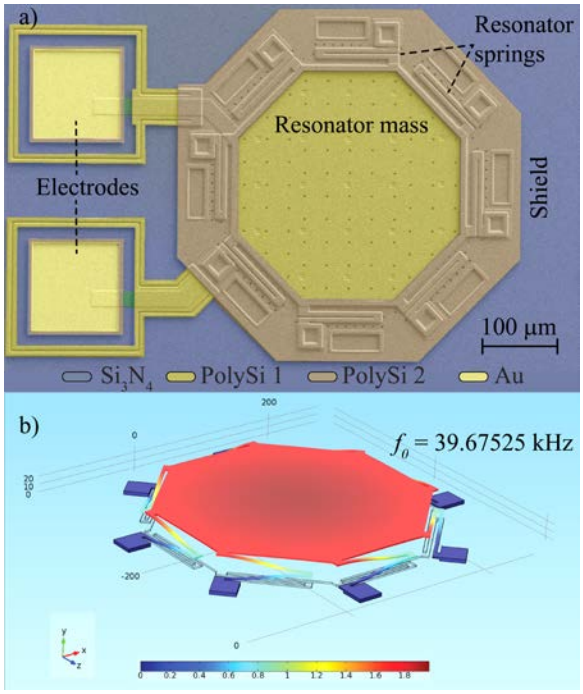

Figure 8. a) Colored SEM image of the integrated mass sensor. b) Finite element simulation showing the amplitude of vibration of the fundamental resonance mode.

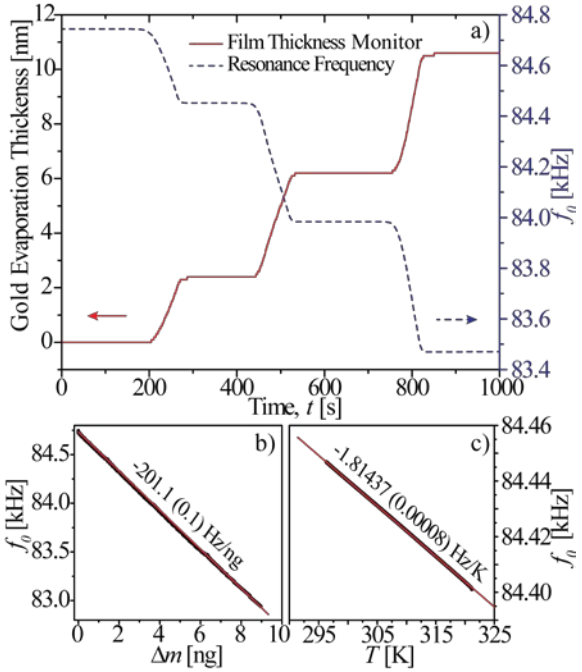

Figure 9. a) Calibration of the MEMS mass sensor using a conventional evaporator and film thickness monitor. b) From the slope it is found that a change of 1 mHz in resonance frequency corresponds to 5 fg added mass. c) Temperature calibration reveals a -1.81437 Hz/K linear temperature dependence. Parentheses indicate the standard fitting error.

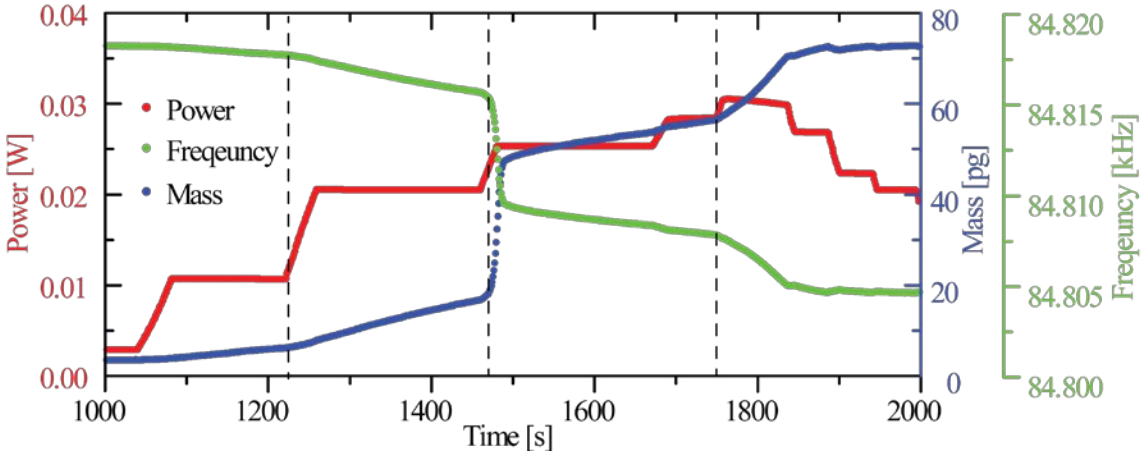

Figure 10. Experimental results of measuring the mass transfer from a MEMS evaporator plate onto the mass sensor. The data is for the evaporation of indium, the frequency is corrected for temperature drift.

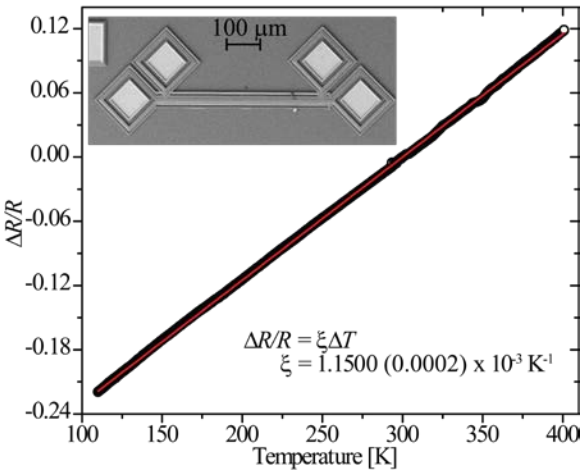

Figure 11. Integrated thermometer/heater and the calibration curve, characterizing the temperature dependence of the resistance.

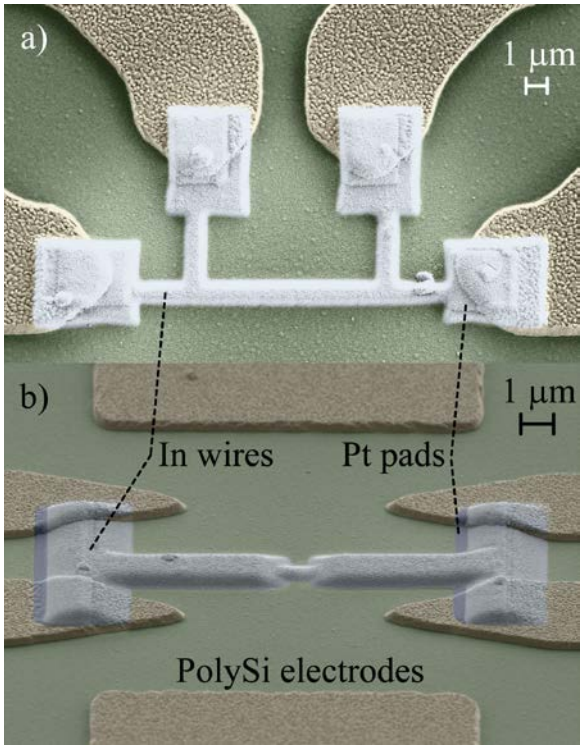

Figure 12. SEM image of FIB deposited platinum pads and indium connections deposited through a) a static stencil and b) a moving aperture onto the pre-positioned polysilicon leads.