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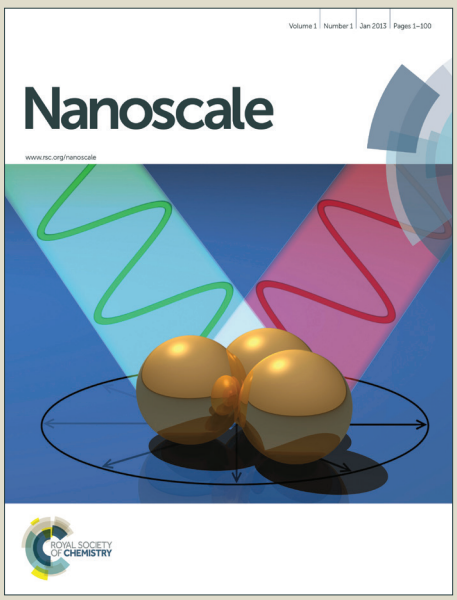

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COMMUNICATION

Inorganic Proton Conducting Electrolyte Coupled Oxide-Based Dendritic Transistors for Synaptic Electronics

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Ionic/electronic hybrid devices with synaptic functions are considered to be the essential building blocks for neuromorphic systems and brain-inspired computing. Here, artificial synapses based on indium-zinc-oxide (IZO) transistors gated by nanogranular SiO_2 proton-conducting electrolyte films are fabricated on glass substrates. Spike-timing dependent plasticity and paired-pulse facilitation are successfully mimicked in an individual bottom-gate transistor. Most importantly, dynamic logic and dendritic integration established by spatiotemporally correlated spikes are also mimicked in dendritic transistor with two in-plane gates as the presynaptic input terminals.

Introduction

Learning, dynamic logic and information integration are the fundamental functions established in human brain by modulating ionic fluxes in synapses and neurons.[1] Neurons are often considered to be the computational engines of the brain.[2] At the same time, synapses act far more than connection of neurons. They are also responsible for massive parallelism, structural plasticity, fault-tolerant and robustness of the brain.[1, 2] Mimicking the functions of synapses and neurons by non-biological substitution is of great significance for building neuromorphic learning and brain-inspired computing systems. Neuromorphic systems are electronic implementations of neural systems, and two approaches are available: software-based and hardware-based. [3] In software-based approaches, large amounts of computational resources are need, because the algorithm is essentially run by conventional sequential machines with limited parallelism. For example, to perform a cortical simulation at the complexity of the human brain, the IBM's Blue Gene supercomputer demands heavy computation resources, requiring clusters of 1,572,864 microprocessors, 1.5 PB (1.5 million GB) of memories, and 6,291,456 threads.[4] Thus, creating cognitive intelligent and energy-efficient system based on hardware is receiving increased interests especially due to the advent of new promising nanotechnologies.

Recently, artificial synapses based on single ionic/electronic hybrid devices with essential synaptic functions have aroused worldwide interests.[5-12] A broad spectrum of materials and devices, such as resistive change memory, phase change memory, conductive bridge type memory, ferroelectric switches, and three-terminal field-effect transistors have been investigated. Usually, ion migration and electrochemical process are regarded as the key points in programming device conductance. For example, WO_3-based memistor was fabricated by Thakoor et al. in 1990, and it was proposed as an analog synaptic memory connection for electronic neural networks. [13] Recently, oxide-based memistors with nanoscale size were also fabricated, and these devices are promising for nonvolatile random-access memory and artificial synapse applications.[14, 15] In electrolyte-gated transistors, ion penetration can induce charge carriers in semiconducting channel, which is known as electrochemical doping.[16-18] Such process can lead to a memory effect in channel conductance and is of significance for realizing synaptic plasticity. For example, K. Kim et al. demonstrated a carbon nanotube synaptic transistor gated by hydrogen-doped PEG electrolyte, and elementary dynamic logic and learning functions were mimicked.[10] The dynamic interaction between CNTs and hydrogen ions in such electrochemical device was found to be the intrinsic reason for synaptic behaviour emulation.

In neural systems, dendrites are the branched projections of a neuron, which conduct the electrochemical stimulation received from other neural cells.[1] Dendrites play a critical role in integrating the synaptic inputs and in determining the extent to which action potentials are produced by the neuron. In pursuing artificial synapses with dendritic functions, the interconnected channel or electrode can work as the dendrite. For example, two presynaptic inputs can jointly trigger postsynaptic currents by an interconnected CNT channel.[11] Here oxide-based electric-double-layer transistor arrays intercoupled by nanogranular phosphorus-doped SiO_2-based electrolyte were fabricated on glass substrates and used for dendritic synapse emulation. Synaptic behaviors, such as spike-timing-dependent plasticity (STDP) and paired-pulse-facilitation (PPF) were mimicked in an individual dendritic transistor. Most importantly, dynamic logic and dendritic integration established by spatiotemporal correlated spikes were also mimicked when multiple in-plane gates were used as the presynaptic input terminals.

Experimental detail

Oxide-based dendritic transistors were fabricated on conducting ITO glass substrates at room temperature. First, phosphorus (P)-

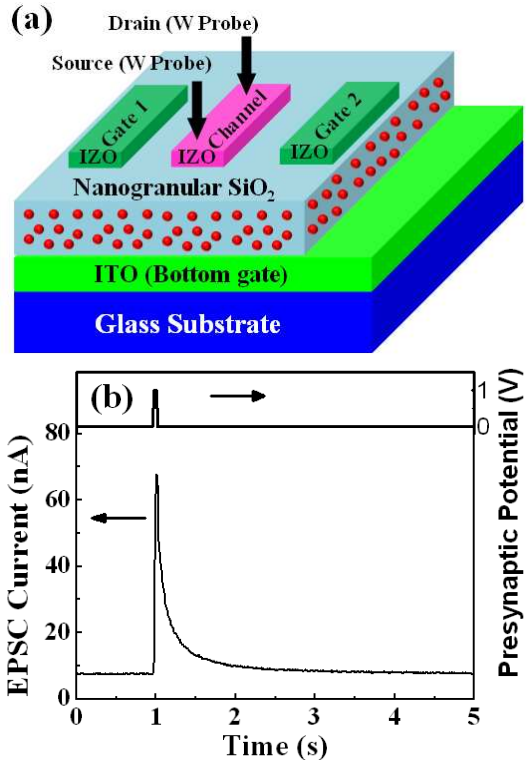

Fig. 1. (a) The schematic image of the oxide-based dendritic transistor gated by nanogranular P-doped SiO_2-based electrolyte film with bottom gate and in-plane gates. (b) The excitatory postsynaptic current (EPSC) plotted versus time. A presynaptic spike was applied on the bottom ITO gate electrode, and the postsynaptic current was measured by applying 0.2 V reading voltage between two W probes with a distance of 300 μm connected to top IZO channel layer.

doped SiO_2 nanogranular electrolyte films with the thickness of ~500 nm were deposited on ITO glass and Si (100) substrates by plasma enhanced chemical vapour deposition (PECVD) using SiH_4/PH_3 mixture and O_2 as reactive gases. Then, patterned indium-zinc-oxide (IZO) films with the size of 150 μm ×300 μm were deposited on the P-doped SiO_2-based electrolyte films by radio-frequency (RF) magnetron sputtering with a nickel shadow mask. IZO film deposition was performed using an IZO ceramic target (In_2O_3: ZnO = 90:10wt %) with a RF power of 100 W and a working pressure of 0.5 Pa. First, a 30-nm-thick bottom IZO layer was sputtered in an Ar/O_2 mixed ambient with a flow rate of 14 sccm and 0.5 sccm for Ar and O_2, respectively. Then the oxygen gas was turned off, and a 10-nm-thick highly conducting top IZO layer was deposited in ambient with gradually reduced oxygen. An ITO/P-doped SiO_2/ITO sandwich structure was prepared for measuring proton conductivities.

Scanning electron microscopy (SEM) was employed to characterize the micro-structure of P-doped SiO_2 nanogranular films. The proton conductivity of the P-doped SiO_2 nanogranular film was determined by Solartron 1260 impedance analyzer. A Cole-Cole plot was measured and the proton conductivity was obtained. Hall measurements were performed with a Hall measurement (Nanometrics HL5500PC). Electrical measurements of the dendritic transistors were performed with a semiconductor parameter analyzer (Keithley 4200). For taking transistor transfer curve, two tungsten (W) probes with a distance of 300 μm are connected to a patterned IZO channel layer and used as the source and drain electrodes. One W probe (source electrode) is grounded, and another W probe is biased at 0.2V (V_{DS}=0.2V) for measuring drain current. All the measurements were performed at room temperature with an air relative humidity of ~50%.

Result

Indium-zinc-oxide (IZO)-based dendritic transistors were fabricated on conducting ITO glass substrates at room temperature. As shown in Fig. 1(a), the channel conductance of the dendritic transistors can be tuned by both bottom gate (bottom ITO film) and in-plane gates (e. g Gate 1 and Gate 2).[19-21] Phosphorus-doped SiO_2 nanogranular proton-conducting films are used as gate dielectrics. Detailed proton conductivity characterization can be found in our previous publication. [22] When the bottom ITO film is used as the gate electrode, a junctionless transistor with bottom-gate structure is obtained (Fig. S1 (b)). While when the in-plane patterned IZO film is used as the gate electrode, gate voltage applied on patterned IZO film can be coupled to the IZO channel by two capacitors in series (Fig. S1 (c)). For electrical measurement, two tungsten probes (source and drain electrodes) with a distance of 300 μm were contacted to the same patterned IZO channel layer. So the channel length is the distance between two W probes (300 μm). No additional source and drain electrodes deposition process is needed, and a good ohmic contacts can be obtained between the W probe and patterned IZO film because the deposited IZO film has a high carrier density in the order of $10^{19}/cm^3$ and a low resistivity of about $2\times10^{-3}\Omega$•cm (measured by Hall measurements). For emulating excitatory postsynaptic current (EPSC), spike-timing-dependent plasticity (STDP) and paired-pulse facilitation (PPF), presynaptic inputs were applied on the bottom ITO gate electrode. While for mimicking dynamic logic and dendritic integration established by spatiotemporal correlated spikes measurements, two presynaptic inputs are needed. Therefore, two inputs are applied on two in-plane gates (Gate 1 and Gate 2). In both cases, the drain electrode is defined as postsynaptic terminal with source grounded. Channel conductance is defined as synaptic weight and measured by a read voltage applied on the drain electrode.

A typical EPSC of the dendritic transistor triggered by a presynaptic spike (1.0 V, 50ms) applied on the bottom ITO gate electrode is shown in Fig. 1(b). The postsynaptic current was measured in the IZO channel with a constant bias of 0.2 V between two tungsten (W) probes. The presynaptic spike triggers an EPSC above the resting current (~7.5 nA), reaching a peak value (~68 nA) at the end of the spike, and gradually reduces to the resting current. When a positive presynaptic spike is applied on the bottom ITO gate electrode, protons in nanogranular P-doped SiO_2 electrolyte will migrate and accumulate at the IZO/P-doped SiO_2 electrolyte interface. At the end of the spike, the accumulated protons will diffuse back to their equilibrium position due to concentration gradient. The migration of protons in the P-doped SiO_2 electrolyte will in turn induce an EPSC in the IZO channel due to the electrostatic couple effect.

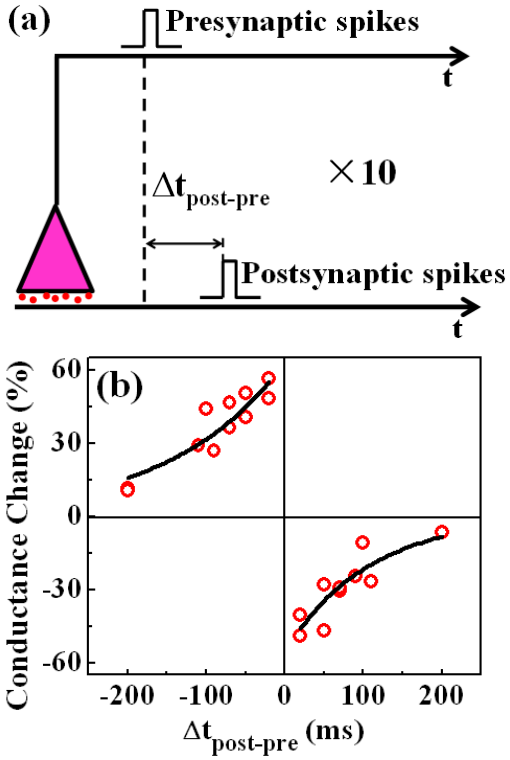

Fig. 2. (a) 10 pairs of presynaptic spike and postsynaptic spike are repeated applied to the bottom gate and drain electrodes, respectively, with a fixed inter-spike interval $\Delta t_{post\text{-}pre}$ for spike-timing dependent plasticity (STDP) stimulation. (b) STDP result of the oxide-based dendritic transistor. The points (red circle) are fitted with exponential decay functions (black line): $\Delta W = A_+ \exp(\Delta t_{post-pre}/\tau_+)$ for $\Delta t_{post\text{-}pre}<0$ and $\Delta W = A_- \exp(\Delta t_{post-pre}/\tau_-)$ for $\Delta t_{post\text{-}pre}>0$.

In biological system, spike-timing dependent plasticity (STDP) is essential to modify synapses in a neural network for learning and memory functions.[23-25] STDP is an elaboration of Hebbian learning applicable in spiking neural systems, in which the modulation of synaptic weight is based on the relative timing of spikes produced by the presynaptic and postsynaptic neurons. For STDP emulation, 10 pairs of presynaptic spikes (4.0 V, 20 ms) and postsynaptic spikes (5.0 V, 20 ms) with a fixed inter-spike interval ($\Delta t_{post\text{-}pre}$) were applied on the bottom ITO gate electrode and top source/drain electrodes (two W probes) connected to the top IZO channel film, respectively. The conductance of IZO channel is regarded as the synaptic weight. Before applying spike-pair, the channel conductance was tuned to the middle-state (~0.1 μS) with a relative deviation of 5% by applying programmed positive and/or negative gate pulses (detailed description see supporting information). Fig. 2(a) shows the schematic diagram for STDP emulation measurement. IZO channel conductance was measured by applying a read pulse (0.2 V, 50ms) between two W probes connected onto the IZO channel before (G_0) and 5 min after (G_t) the spike-pair application. The relative change of synaptic weight is defined as:

$$\Delta W=(G_t-G_0)/G_0$$

The changes in synaptic weight (ΔW) were measured under different $\Delta t_{post\text{-}pre}$ ranging from -200 ms to 200 ms as shown in Fig. 2(b). The data in Fig. 2(b) are statistically scattered, similar to that observed in biological synapse.[19] The changes in synaptic weight (ΔW) could be fitted by exponential functions: $\Delta W=A_+\exp(\Delta t_{post-pre}/\tau_+)$ for $\Delta t_{post\text{-}pre}<0$ and $\Delta W=A_-\exp(-\Delta t_{post-pre}/\tau_-)$ for $\Delta t_{post\text{-}pre}>0$. A_+ and τ_+ are fitted to be ~ 63% and145ms, respectively. And A_- and τ_- are fitted to be ~-56% and 106ms, respectively. The values of A and τ are comparable with those observed in biological synapses. [23, 24]

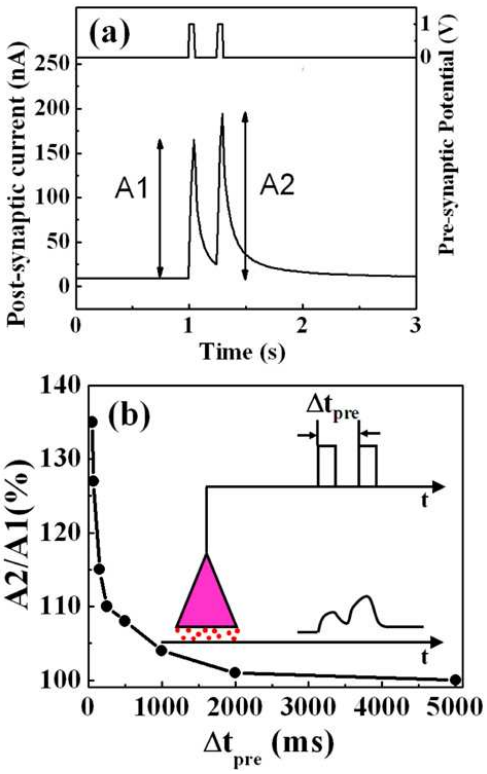

Fig. 3. (a) The EPSCs triggered by a pair of presynaptic spikes with a Δt_{pre}=250 ms and an IZO channel current reading voltage of 0.2 V (V_{DS}). The EPSC triggered by the second presynaptic spike is larger than the EPSC by the first spike. A_1 and A_2 were the amplitudes of the first and second EPSCs, respectively. (b) The ratio of the two EPSC amplitudes (A_2/A_1) is plotted versus interval-time between the two spikes (Δt_{pre}). The ratio decreases with the increasing Δt_{pre}. The inset is the Schematic diagram of the measurent of paired-pulse facilitation (PPF). Two successive pre-synaptic spikes (1.0 V, 50 ms) were applied on presynaptic neuron. The inter-spike interval (Δt_{pre}) ranges between 50 ms and 5000 ms.

According to STDP learning rule, plasticity or synaptic weight depends on the relative timing of pre- and post-synaptic spikes.22 In neocortical slices, hippocampal slice and cell cultures, long-term weakening of synapses occurs when presynaptic action potentials follow postsynaptic firing. While presynaptic action potentials that precede postsynaptic spikes produce long-term strengthening of synapses. The largest changes in synaptic efficacy occur when the time difference between pre- and post-synaptic action potentials is no smaller than a time-difference-window. It was reported that the P-doped SiO_2 electrolyte film is an inorganic proton conductor. [26, 27] When a positive pulse voltage is applied on the gate electrode (or IZO film), two

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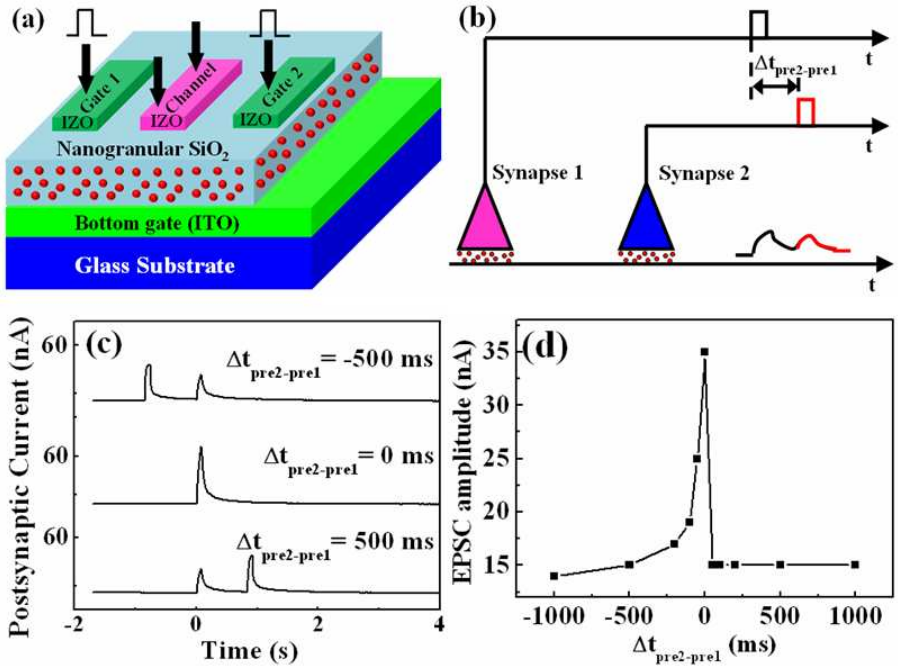

Fig. 4. (a) The schematic image of dynamic logic established by spatiotemporal spikes measurements with two in-plane gates as presynaptic terminals. (b) The schematic image of EPSCs triggered by a pair of spatiotemporally correlated spikes. The two presynaptic spikes with fixed time intervals $\Delta t_{pre2\text{-}pre1}$ were applied on Gate 1 and Gate 2, respectively, and EPSCs were measured in the IZO channel layer with a reading voltage of 0.2 V. (c) EPSCs plotted versus time with two spatiotemporally correlated spikes with $\Delta t_{pre2\text{-}pre1}$=-500 ms, 0 ms, 500 ms. (d) The amplitude of the EPSC at Δt=0 (as soon as the presynaptic spike applied on Gate 1) is plotted as a function of $\Delta t_{pre2\text{-}pre1}$.

processes can be observed: 1) hydrogen bond in SiO_2 electrolyte breaking, 2) ionized hydrogen hopping and migrating to the SiO_2 /ITO gate (or SiO_2/IZO channel) interface. If the two pulses are close enough, before the ionized hydrogen goes back its equilibrium state, the ionized hydrogen will migrate to the interface under the second pulse voltage. When a high positive (negative) bias is applied on gate, protons in the SiO_2 electrolyte can penetrate into (out) the IZO channel, which will result in a permanent increment (decrement) in channel conductance due to electrochemical doping.[28, 29] In fact, proton was reported to be the effective shallow donor in zinc oxide [30, 31] The ion relaxation process can be descirbed by a stretched-exponential function written as:

$$\Phi_t(t)=\Phi_o[-(t/\tau)^{\beta}]$$

where $\Phi_t(t)$, Φ_o, τ and β is the ion concentration, the initial ion concentration, the characteristic relaxation time, and the stretch index, respectively.[32,33] According to such equation, when two closer spikesare applied, the more residual ionized hydrogen can be obtained by the first spike. Then more remarkable proton penetration/extraction process can be observed in turn by the second applied spike. So, the net effect of the two processes eventually lead to the measured STDP behavior.

When a presynaptic neuron receives two stimuli in rapid succession, the postsynaptic response will commonly be larger for the second than that for the first—a phenomenon known as paired-pulse facilitation (PPF).[34] As a common form of short-term synaptic plasticity in biological synapses, PPF reflect responsivity for the second pulse when first pulse and the second pulse are close enough.[35] Such PPF is essential to decode temporal information in auditory or visual signals. In our case, oxide-based dendritic transistors can process temporally correlated spikes and generate the short-term plasticity, i.e., PPF. Fig. 3(a) show the EPSC triggered by a pair of presynaptic spikes with inter-spike interval Δt_{pre}=250 ms. Two successive presynaptic spikes (1.0 V, 50 ms) were applied on the bottom ITO gate electrode. The EPSC current was obtained with reading voltage (V_{DS}) of 0.2 V. The EPSC triggered by the second presynaptic spike is larger than the EPSC triggered by the first spike. The Δt_{pre} ranges from 50 ms to 5000 ms. The ratio of the amplitudes between the second EPSC (A_2) and the first EPSC (A_1) is plotted versus Δt_{pre} in Fig. 3(b). The ratio gradually decreases with increasing Δt_{pre}. A maximum value of ~137% is obtained with Δt_{pre}=50 ms. The inset in Fig. 3(b) illustrates the schematic diagram for measuring PPF. After the first spike, the protons in P-doped SiO_2 electrolyte would drift back to their equilibrium positions due to the concentration gradient. If the second spike is applied closely enough, the ionized hydrogen triggered by the first spike still partially resides near IZO channel. Thus, the worked protons triggered by the second spike near IZO are augmented with the residual protons. Bigger Δt_{pre} would

induce

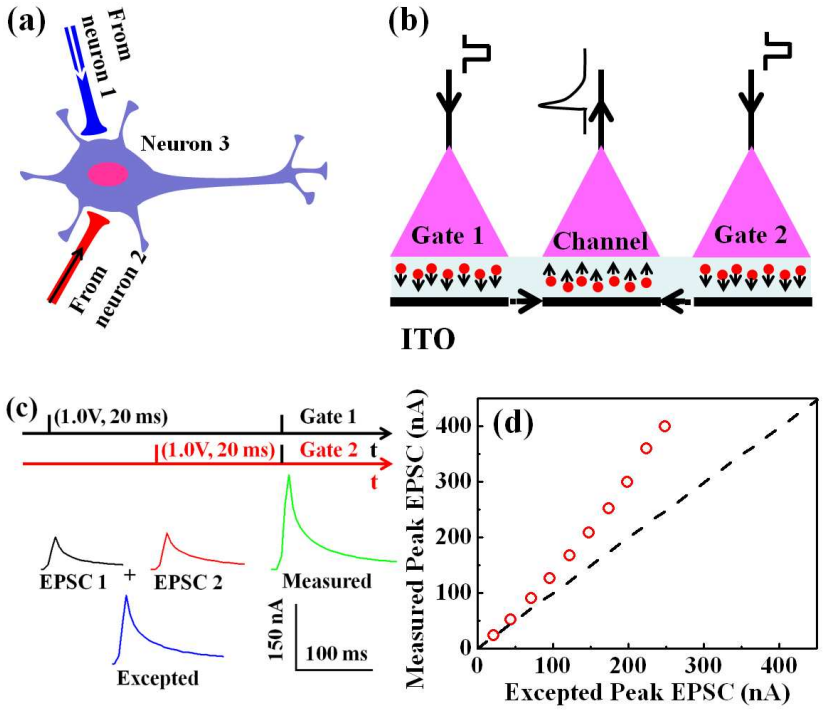

Fig. 5. (a) Schematic diagram of dendrite integration from two neurons. (b) Schematic diagram of the spatial summation mimicked in IZO-based dendritic transistor. Spatial signal from two in-plane gates can be integrated and coupled to the channel due to the electric field induced by mobile protons. (c) Protocol for testing spatial summation (dendritic integration). The two spikes (1.0 V, 20 ms) were first set separated (time interval=5 s) and then set simultaneously (at t=10 s). The combined event (green line) was compared with the expected (blue line)—linear sum of the two individual events (black line and red line). (d) Comparison of excepted sum and measured sum of two EPSC from two presynaptic neurons triggered by different presynaptic spikes(from 0.2 V to 2.0 V, 20 ms) with a channel reading voltage of 0.2 V.

less residual hydrogen ions near IZO channel and result in lower value of A2/A1.

Such dendritic transistors can also be implemented to establish a dynamic logic function when two in-plane gates are used as two presynaptic input terminals and drain electrode as postsynaptic output terminal (Fig. 4(a)). 10 Fig. 4(b) shows the schematic diagram for measuring the dynamic logic established by spatiotemporally correlated spikes (0.5 V, 50 ms) from two presynaptic neurons with an inter-spike interval ($\Delta t_{pre2\text{-}pre1}$). The zero time was defined as the presynaptic spike applied on Gate 1 (Pre1) just ended. Fig. 4(c) shows the EPSCs triggered by the spatiotemporally correlated spike pairs with $\Delta t_{pre2\text{-}pre1}$=-500 ms, 0 ms, and 500 ms. The results show the combination effect (EPSC amplitude at zero time) by the two spatiotemporally correlated spikes is dynamically dependent on $\Delta t_{pre2\text{-}pre1}$. Both the $\Delta t_{pre2\text{-}pre1}$=500 ms and $\Delta t_{pre2\text{-}pre1}$=-500 ms has no impact on the combination effect, while the $\Delta t_{pre2\text{-}pre1}$=0 case makes a remarkable increment on the EPSC amplitude at zero time. Fig. 4(d) shows the combination effect plotted as a function of time. If $\Delta t_{pre2\text{-}pre1} \leq 0$, the distribution of protons in dielectric at the beginning of Pre1 is largely dependent on the value of $\Delta t_{pre2\text{-}pre1}$. The closer the inter-spike interval would lead the more protons which are residual near the IZO channel. Therefore, the higher EPSC amplitude can be obtained at the zero time than solely applied the Pre1. While, if $\Delta t_{pre2\text{-}pre1} > 0$, there is no residual protons at the beginning of Pre1. In vivo, the highly parallel process in the neuron networks is mediated through a mass of synaptic interconnections. Presynaptic spikes from different neurons can trigger a postsynaptic current through synapses in a postsynaptic neuron to establish dynamic logic in a neural network. [36, 37] Therefore, such dendritic transistor is essential for spike-timing dependent logic and neural computation emulations.

Fig. 5(a) shows the schematic diagram of dendrite integration from two presynaptic inputs (known as spatial summation) from two different neurons. The information from two presynaptic neurons (neuron 1 and neuron 2) is summed in the dendrite of postsynaptic neuron. As shown in Fig. 5(b), presynaptic signals applied on in-plane gates (Gate 1 and Gate 2) can be integrated and coupled to IZO channel due to the electric field induced migration of protons. Fig. 5(c) shows the schematic diagram for measuring spatial summation of two presynaptic inputs. Firstly, input signals (1.0 V, 20 ms) from two presynaptic neurons (neuron 1 and neuron 2) are set separately with fixed pulse-to-pulse interval of 5000 ms. Then, they are set simultaneously and the triggered signals are summed in the postsynaptic terminal. Fig. 5(d) shows a comparison of excepted sum (arithmetic sum) and measured sum of two EPSC (EPSC1 and EPSC2) from these two presynaptic neurons triggered by different presynaptic spikes (from 0.2 V to 2.0 V, 20 ms). Such result illustrates that summation in such artificial synaptic network is linear for weak stimuli and superlinear for strong stimuli. Such results are similar to that observed in some biological experiments, [36-38] which

indicates a potential application in neuromorphic computing.

Discussion and Conclusion

In conclusion, oxide-based dendritic transistors intercoupled by nanogranular phosphorus-doped SiO_2 electrolytes were fabricated on glass substrates. Synaptic plasticity, such as STDP and PPF, are mimicked in individual oxide-based synaptic transistor. Most importantly, dynamic logic and spatial summation established by spatiotemporal correlated spikes from two different neurons were also mimicked in dendritic transistor with two in-plane gates. Moreover, the artificial synapse with synaptic plasticity and dendritic computation is not limited to two in-plane-gate presynaptic inputs. More complex function can also be realized with more presynaptic terminals and postsynaptic terminals. The energy consumption for an EPSC event is estimated of ~400pJ/spike from the data of Fig. 1(b). Energy consumption of our synaptic transistor can be further reduced by three approaches: 1) Using oxide channel layer with low electron concentration, such as IGZO layer; 2) Reducing the pulse operation voltage and the thickness of the P-doped SiO_2 electrolyte film; 3) Reducing the pulse width. At present, our synaptic transistors were fabricated by a low-cost and simple process based on one shadow mask. It is possible to scale the size of our device down to ~100 nm with the advanced photolithography process in the future because our device has a field-effect transistor configuration. Such artificial dendritic transistors could be potentially implemented as the building blocks for neuromorphic systems.

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† Electronic Supplementary Information (ESI) available: The structures and transfer characteristics of the IZO junctionless transistor worked at bottom-gate mode and in-plane gate mode. See DOI: 10.1039/b000000x/

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A table of contents entry

Artificial synapses based on oxide-based EDL transistors with two in-plane gates were fabricated and STDP, dynamic logic and dendritic integration were demonstrated.