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ARTICLE

Individual and synergetic charge transport properties at the solid and electrolyte interfaces of a single ultrathin single crystal of organic semiconductors

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Chemical structures and morphologies of organic semiconductors (OSCs) and gate dielectrics have been widely investigated to improve electrical performances of organic thin-film transistors (OTFTs) because the charge transport therein is a phenomenon at the semiconductor–dielectric interfaces. Here, solid and ionic gel gate dielectrics were adopted on the lower and upper surfaces, respectively, of a single, two molecules-thick single crystal of p-type OSCs to study the charge transport properties at individual interfaces between the morphologically compatible OSC surface and different gate dielectrics. By using the four-probe method, the solid and ionic gel interfaces exhibited hole mobilities of 9.3 and 2.2 $cm^2 V^{-1} s^{-1}$, respectively, which revealed the crucial impact of gate dielectric material on the interfacial charge transport. Interestingly, when gate biases are applied through both dielectrics, *i.e.*, under the solid/ionic gel dual-gate transistor operation, the hole mobility at the solid gate interface was improved up to 14.7 $cm^2 V^{-1} s^{-1}$, which is 1.5 times greater than that assessed without the ionic gel gate. This improvement can be attributed to the electric double layer forming at the ionic gel/uniform crystal surface, which provides a close-to-ideal charge transport interface through a dramatic trap-filling. Therefore, the present dual-gate transistor technique will be promising for investigating the intrinsic charge-transport capabilities of OSCs.

1. Introduction

Organic thin-film transistors (OTFTs) have been rapidly emerging owing to their potential applications to low-cost, printable and flexible devices, such as integrated circuit elements and sensors. In both fundamental and applied researches, single crystals of organic semiconductors (OSCs) play a significant role due to their long-range-ordering and grain-boundary-free structures[1] and potential solution processability[2] in OTFT applications. Along with the development of high-performance OSCs, the charge-carrier mobility (μ) of ≥10 $cm^2 V^{-1} s^{-1}$ has been demonstrated at room temperature by solution-processed single-crystal OTFTs.[3–8] Although such high μ have been typically demonstrated by conventional solid gate dielectrics, an electric double layer (EDL) formed by electrolytes or ionic liquids is of interest for high-density carrier accumulation at low voltages.[9] A recent work on the electric double-layer transistor (EDLT) architecture realized a two-dimensional hole gas in solution-grown ultrathin OSC single crystals.[10] As the OSC–gate dielectric interface is crucial for charge-transport properties,[11–14] it is important to understand the relationships between gate dielectric materials and OTFT properties. Accordingly, solid-gate OTFTs should show different characteristics from EDLTs. Although it is desirable to see the relationships by using a single OSC film, polycrystalline films show different morphologies at their upper and lower surfaces due to step formation and voids (Fig. 1a), which leads to non-straightforward interpretations even in dual-gate OTFTs with solid gate dielectrics at both surfaces. In this respect, OSC single crystals particularly in a few-molecules thickness should be the likeliest platform[16] to avoid such complications owing to

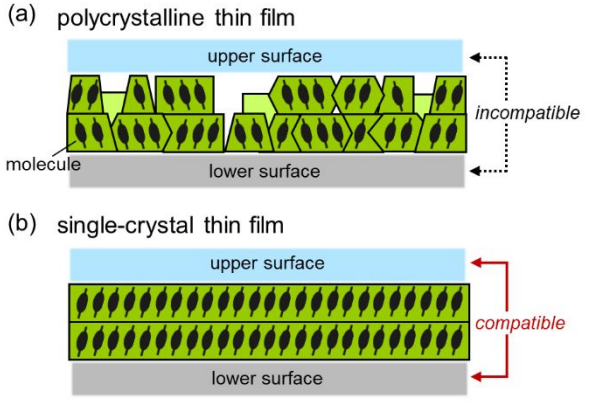

Fig. 1 Schematic illustration of (a) polycrystalline and (b) single crystal thin films composed of organic molecules.

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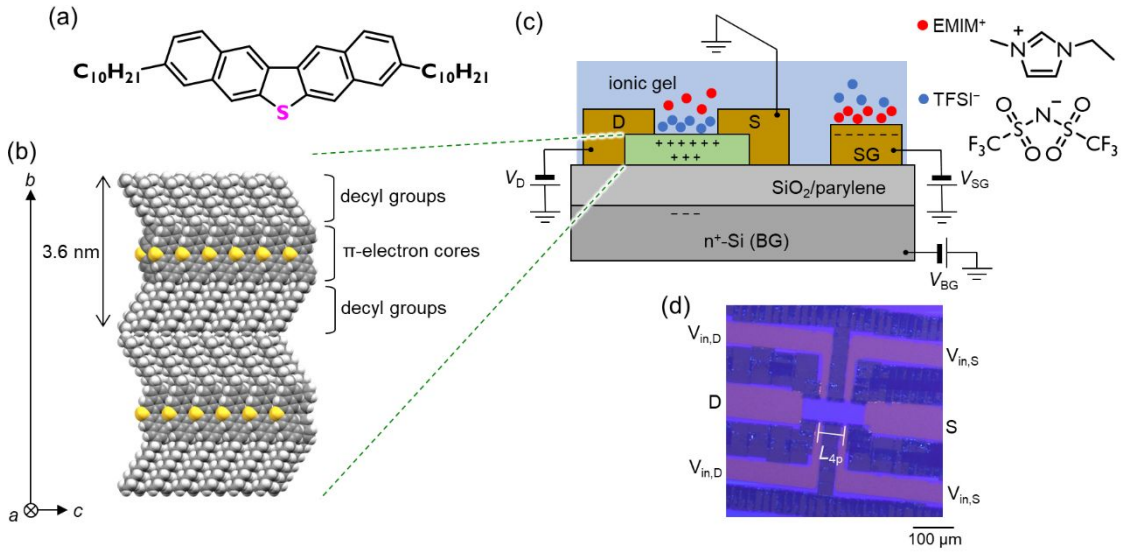

Fig. 2 (a) Chemical and (b) crystal structure (CCDC 2010721)[15] of C_{10}–DNT–VW. (c) Schematic device structure of solid/ionic gel dual-gate organic thin-film transistor. (d) The patterned C_{10}–DNT–VW transistor viewed under optical microscope with polarized light. S: source electrode; D: drain electrode; BG: bottom-gate electrode; SG: side-gate electrode; $V_{in,S}$ and $V_{in,D}$: in-channel potential probes at the source and drain electrode side, respectively; V_D: drain bias; V_{BG}: bottom-gate bias; V_{SG}: side-gate bias.

their highly uniform surfaces (Fig. 1b).

In this work, solid and ionic gel gate dielectrics were adopted to study individual transistor properties of solution-grown ultrathin single crystals of OSCs by using the four-probe transistor architecture which allows an assessment of the intrinsic μ values owing to an exclusion of contact resistance effects.[17] The μ values under the solid and ionic gel gating were differed by 4 times or more due to charge-trap densities at different gate dielectric interfaces. In addition, the solid/ionic gel dual-gate OTFT properties were investigated. Whereas dual-gate OTFTs are generally discussed in terms of threshold voltage controls,[18,19] the present four-probe architecture provides deeper insights into the charge transport properties. Interestingly, the maximum μ of 14.7 $cm^2\ V^{-1}\ s^{-1}$ was observed under an appropriate EDL strength, which mobility is 1.5 times greater than that without the ionic gel. This synergetic enhancement is most likely due to the close-to-ideal trap-free state. Therefore, this paper provides significant insights into the impact of gate dielectric materials on interfacial charge transport event, and demonstrates the solid/ionic gel dual-gate OTFT architecture as a tool to study potential charge-transport capabilities of OSCs.

2. Experimental

2.1. Materials

C_{10}–DNT–VW was prepared according to the literature.[15] Anisole (Kanto Chemical), acetonitrile (Tokyo Chemical Industry), 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (EMIM–TFSI) (Kanto Chemical) and poly(vinylidene fluoride-co-hexafluoropropylene) (P(VDF–HFP)) (Sigma-Aldrich) were purchased from the commercial sources and used without further purification.

2.2. Bottom-gate OTFT fabrication

To an n^+-Si wafer with thermally oxidized SiO_2 layer (100 nm) was deposited 85 nm-thick parylene (diX-SR, KISCO Ltd.) by chemical vapor deposition. Single-crystalline thin films of C_{10}–DNT–VW were solution-coated by from a 0.01 wt % anisole solution with maintaining the substrate temperature around 45 °C. After annealing at 45 °C for 10 hours under vacuum, 45 nm-thick Au electrodes were vacuum-deposited through a metal shadow mask. The four-probe architecture was patterned by laser ablation, followed by annealing at 110 °C for 1.5 hours under vacuum.

2.3. Side-gate EDLT (dual-gate OTFT) fabrication

To an n^+-Si wafer with thermally oxidized SiO_2 layer (100 nm) was deposited 85 nm-thick parylene (diX-SR, KISCO Ltd.) by chemical vapor deposition. Single-crystalline thin films of C_{10}–DNT–VW were solution-coated by from a 0.01 wt % anisole solution with maintaining the substrate temperature around 45 °C. After annealing at 45 °C for 10 hours under vacuum, 45 nm-thick Au electrodes were vacuum-deposited through a metal shadow mask. The four-probe architecture was patterned by laser ablation, followed by annealing at 110 °C for 1.5 hours under vacuum.

2.4. Electrical evaluations

Capacitance measurements were carried out by using a HIOKI IM3533 LCR meter. The capacitance of the bottom-gate dielectric layer was measured with an n^+-Si/SiO_2 (100 nm)/diX-SR (85 nm)/Au (45 nm) metal-insulator-metal structure, affording $C_{i,BG}$ = 18.1 nF cm^{-2} at 1 Hz. The capacitance of an ionic gel was measured with two bottom-contact Au electrodes

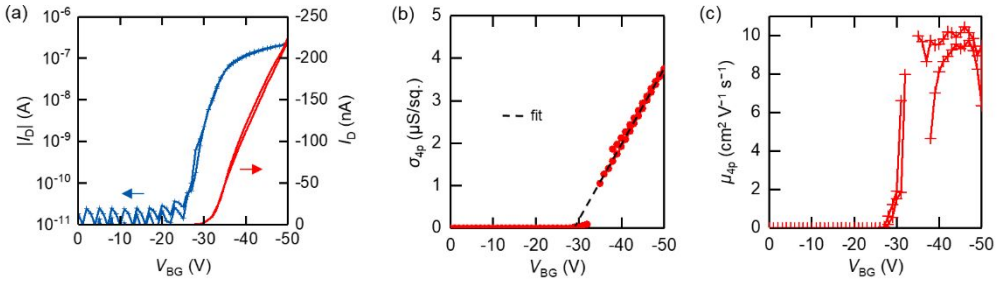

Fig. 3 Four-probe analysis of solid-gate OTFT properties. (a) Transfer curve, (b) sheet conductivity, and (c) field-effect hole mobility for the bottom-gate operation in air (V_D = −1 V). Noises due to the four-probe measurements are excluded for clarity.

bridged by an ionic gel sheet on a glass substrate. The specific area was 1.32 × 10^{-2} cm^2 (Fig. S1, ESI). Bottom-gate OTFT properties were measured on a Keithley 4200-SCS semiconductor parameter analyzer under ambient atmosphere and in the dark. EDLT and dual-gate OTFT measurements were carried out with Keithley 2634B and 2400 sourcemeters, and Keithley 2000 multimeters for transistor operation and in-channel potential measurement, respectively, in an argon-filled glovebox at room temperature to avoid undesired electrochemical reactions and device degradations by water adsorption. Further details of contact resistance measurements are described in Electronic Supplementary Information (Fig. S2, ESI).

3. Results and discussion

3.1. Bottom-gate OTFT properties

A p-type OSC, 3,9-didecyldinaphtho[2,3-*b*:2′,3′-*d*]thiophene (C_{10}–DNT–VW)[20] (Fig. 2a) was employed in this work. C_{10}–DNT–VW exhibits a lamellar, herringbone packing structure with the column direction suitable for hole transport capability along the *c*-axis direction (Fig. 2b).[15] It is noted that two molecules-thick single crystals were focused on. The schematic structure of a dual-gate OTFT is shown in Fig. 2c. The series capacitance of an SiO_2/parylene bottom-gate dielectric per unit area ($C_{i,BG}$) was measured to be 18.1 nF cm^{-2} at 1 Hz. Thin-films of C_{10}–DNT–VW were deposited by edge casting method[21] using anisole as a solvent, and top-contact Au electrodes were vacuum-evaporated through a metal shadow mask to adjust the channel parallel to the *c*-axis direction. Channel width and length are 48 and 150 μm, respectively, and the longitudinal inter-probe distance (L_{4p}) is 50 μm (Fig. 2d). A 2 mm by 3 mm side-gate electrode is placed approximately 1.5 mm away from the drain electrode.

The bottom-gate OTFT performance was investigated in air without an ionic gel layer. As shown in Fig. 3a, the best OTFT based on C_{10}–DNT–VW exhibited a typical p-channel operation despite no extra doping at the metal–semiconductor interfaces as conducted in the previous works.[15,20] Four-probe sheet conductivity (σ_{4p}) given by $(I_D/\Delta V_{in})(L_{4p}/W)$, where ΔV_{in} is the potential difference between $V_{in,D}$ and $V_{in,S}$, is shown in Fig. 3b as a function of bottom-gate voltage (V_{BG}). Four-probe hole mobility (μ_{4p}) was extracted according to the equation:

$$\sigma_{4p} = C_i \mu_{4p} (V_{BG} - V_{th,BG}) \quad (1)$$

where μ_{4p} is 9.3 cm^2 V^{-1} s^{-1}, and the threshold voltage for bottom-gate operation ($V_{th,BG}$) is −29 V (Fig. 3c). Here the $V_{th,BG}$ value is not negligible due to a high ionization potential of C_{10}–DNT–VW (−5.64 eV)[20] producing considerable interfacial trap states and contact resistance,[22,23] the latter of which also explains the lower two-probe mobility of 1.9 cm^2 V^{-1} s^{-1}. Note that the μ_{4p} is comparable with our previous work,[15] being indicative of the reproducible single-crystal qualities.

3.2. Side-gate EDLT properties and comparison with bottom-gate OTFT

Then, a free-standing ionic gel (IG)[24] sheet was prepared from 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (EMIM–TFSI) ionic liquid and poly(vinylidene fluoride-co-hexafluoropropylene) (P(VDF–HFP)) polymeric support at a 2:1 weight ratio.[10] The areal gate capacitance for the present IG ($C_{i,SG}$) was measured to be 4.64 μF cm^{-2} at 1 Hz (Fig. 4a). A side-gate (SG) configuration was fabricated by manually placing the IG sheet on top of the OTFT to yield the dual-gate OTFT. First, a transfer curve with SG modulation, namely, EDLT operation,

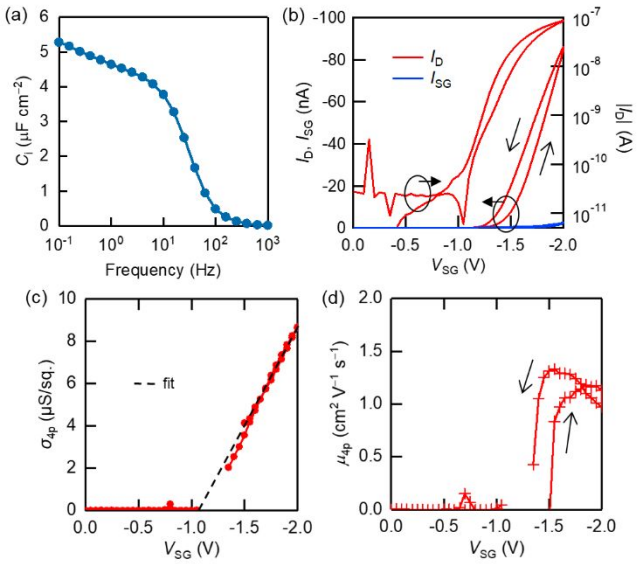

Fig. 4 Four-probe analysis of EDLT properties. (a) Frequency-dependent capacitance of the ionic gel. (b) Transfer curve, (c) sheet conductivity, and (d) field-effect hole mobility for the side-gate operation in an argon atmosphere (V_D = −0.05 V and V_{BG} = 0 V). Noises due to the four-probe measurements are excluded for clarity.

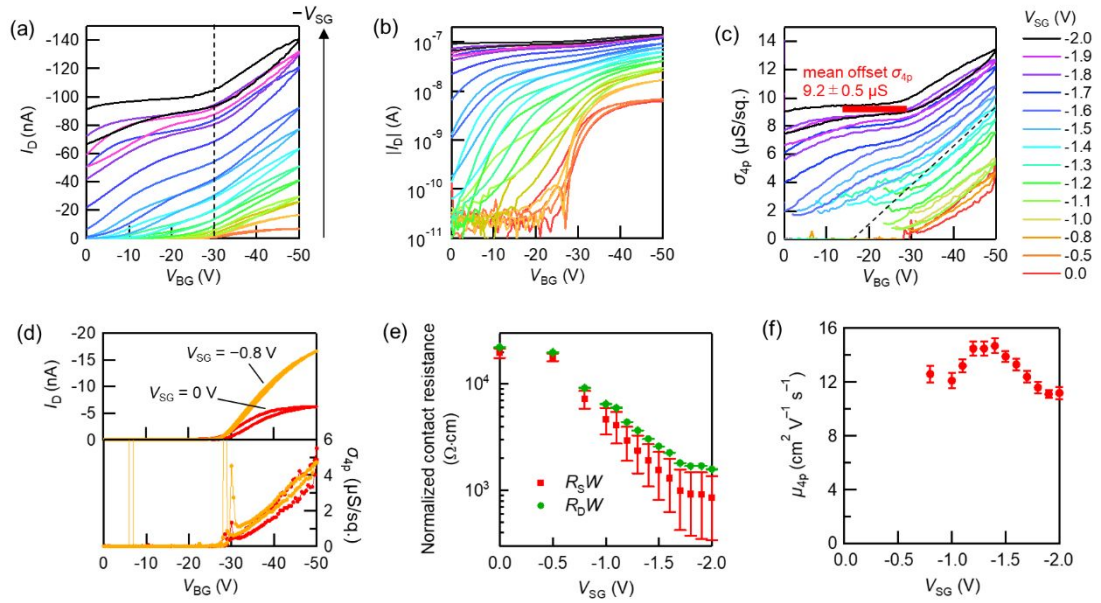

Fig. 5 Dual-gate OTFT properties. (a, b) Transfer curves under BG modulation at various V_{SG}. $-V_{SG}$ = 0, 0.5, 0.8 and 1.0–2.0 V with an increment of 0.1 V. V_D = −0.05 V. Black broken line in (a) shows the threshold of bottom-gate transistor. (c) σ_{4p}–V_{BG} characteristics. Dashed black line is the representative best-fit result by Equation 1 (V_{SG} = −1.4 V), and thick red line depicts the offset current at V_{SG} = −2.0 V. (d) Extracted I_D– and σ_{4p}–V_{BG} curves (upper and lower panel, respectively) at V_{SG} = 0 and −0.8 V. (e) Contact resistance normalized by channel width of dual-gate OTFT as a function of V_{SG}. (f) Bottom-gate μ_{4p} as a function of V_{SG}.

was characterized with the bottom-gate electrode grounded (V_{BG} = 0 V) (Fig. 4b). The p-channel transistor behavior was again observed with a counterclockwise hysteresis.[10,25] The maximum source–SG current (I_{SG}) was −2.7 nA at side-gate voltage (V_{SG}) of −2.0 V. Thus I_{SG} was maintained <4% source–drain current (I_D), revealing a proper EDLT operation. Fig. 4c shows σ_{4p} as a function of V_{SG}, where the maximum σ_{4p} is 8.6 μS/sq. at V_{SG} = −2.0 V. The hysteresis observed in the I_D–V_{SG} curve is likely suppressed in the depiction of σ_{4p}, which affords a threshold voltage ($V_{th,SG}$) of −1.1 V for the EDLT if Equation 1 is used. It is noted that, in contrast to EDLTs based on rubrene single crystals,[26–30] peak structures were not observed in the transfer curves, which is consistent with EDLTs based on single crystalline OSCs bearing alkyl or fluoroalkyl substituents.[10,31] This suggests the importance of the insulating substituents encapsulating charge-transport layers, despite the limited V_{SG} to avoid dissolution of the C_{10}–DNT–VW thin-film single crystal.[25] μ_{4p} under the EDLT operation is estimated to be 2.2 cm^2 V^{-1} s^{-1} by using the capacitance of EDL ($C_{i,SG}$ = 4.64 μF cm^{-2}) (Fig. 4d). The lower EDLT mobility than that of the solid-gate OTFT is typically attributed to carrier scattering[27] and/or charge trapping[28,30] granted by charged (ionic) components. This is confirmed by calculating the maximum density of interfacial trap states (D_{it}^{max}) following the equation[32]:

$$D_{it}^{max} = \frac{C_i}{q^2}\left(\frac{qS}{k_BT\ln(10)} - 1\right) \quad (2)$$

where q is the elementary charge, S the subthreshold swing, k_B the Boltzmann's constant, and T the absolute temperature. Inthe C_{10}–DNT–VW device, S is estimated to be 1.95 and 0.17 V dec^{-1} for solid and IG gating, respectively (Figs. 3a and 4b). Hence, D_{it}^{max} for the OSC–parylene/SiO_2 and OSC–IG interfaces are calculated to be 3.7 × 10^{12} and 5.6 × 10^{13} eV^{-1} cm^{-2}, respectively. Thus, the OSC–IG interface clearly produces a larger density of interfacial traps by an order of magnitude.

3.3. Behavior and contact resistance in solid/ionic gel dual-gate OTFT properties

Furthermore, dual-gate OTFT performances were studied by measuring transfer curves by sweeping V_{BG} while fixing V_{SG} to respective values (Figs. 5a-5c). Fig. 5a indicates an increase in $-I_D$ that was observed following an increase in $-V_{SG}$, while apparent changes were not observed below −0.8 V. At V_{SG} = −0.8 V, the slope of the I_D–V_{BG} curve increased relative to that with smaller $-V_{SG}$, which led to nearly triple $-I_D$ at V_{BG} = −50 V, as represented in the upper panel of Fig. 5d. Note that σ_{4p} did not increase from V_{SG} = 0 to −0.8 V (the lower panel of Fig. 5d). This suggests reduced contact resistances of the bottom-gate OTFT without $V_{th,BG}$ shift owing to enriched carrier concentrations near source and drain electrodes as reported on split-gate[33,34] and solid/solid dual-gate OTFTs[35] by the strong electric field of EDL at the upper surface. From the experimental results, normalized contact resistances at V_{BG} = −50 V and V_{SG} = 0 V are calculated to be 19.7 and 22.2 kΩ cm for the source (R_SW) and drain (R_DW) contacts, respectively. By applying V_{SG}, R_SW and R_DW are slightly decreased to 18.0 and 19.8 kΩ cm, respectively at V_{SG} = −0.5 V, and further to 7.3 and 9.2 kΩ cm, respectively, at V_{SG} = −0.8 V (Fig. 5e). Larger V_{SG} further reduces the contact resistance, where R_SW and R_DW become 0.86 and 1.6 kΩ cm, respectively, at V_{SG} = −2.0 V. On the other hand, in Figs. 5a and 5b, there are apparent positive shifts of $V_{th,BG}$ by applying V_{SG}, in similar vain to dual-gate OTFTs so far reported.[19,36] As $-V_{SG}$ is increased, the apparent $V_{th,BG}$ is followed by remarkable increases in the offset (*i.e.* the off-state) current in the low V_{BG} region, which has been observed in dual-solid gate rubrene single crystal[37] and solid/ionic liquid dual-gate transistors based

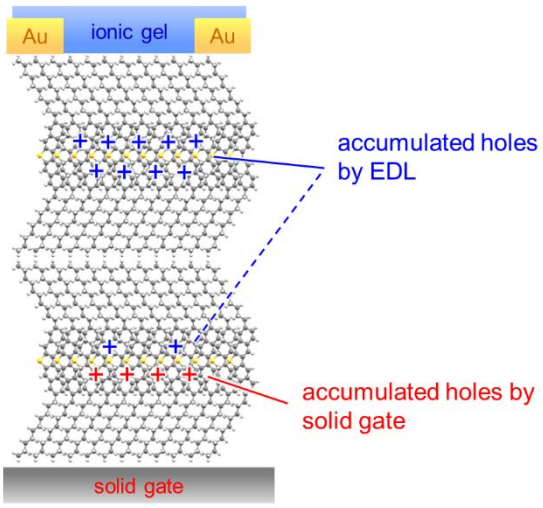

Fig. 6 Schematic illustration of the effect of EDL on dual-gate OTFT properties.

on polycrystalline octathio[8]circulene thin film.[38] In the present study, the increase in the offset current is much remarkable than that in the previous works, revealing the contributions of both single-crystal OSC and EDLT architecture to the dual-gate OTFT properties.

3.4. Synergetic mobility enhancement under solid/ionic gel dual-gate OTFT operation

One can also see that the transfer curves are likely composed of two regions: proportionally V_{BG}-dependent and offset regions in high and low V_{BG} regimes, respectively. As denoted in Fig. 5a (dashed black line), the threshold between those regimes is located at about −30 V, which is comparable to the abovementioned $V_{th,BG}$. Hence, the apparent $V_{th,BG}$ shift is associated with the upper shift of the proportionally V_{BG}-dependent I_D curve due to the emergence of offset current. As the representative, the mean offset σ_{4p} at V_{SG} = −2.0 V is 9.2±0.5 μS/sq. (thick red line in Fig. 5c), which is close to the σ_{4p} of 8.6 μS/sq. measured in the EDLT operation (Fig. 4c). That is, the offset current is principally attributed to the formation of a conductive upper surface due to the EDLT mechanism, which is almost independent of the bottom-gate OTFT. Thus, the measured σ_{4p} could be expressed as follows, following the literature[37]:

$$\sigma_{4p}(V_{BG},V_{SG}) = C_{i,BG}(V_{BG} - V_{th,BG})\mu_{4p,BG} + C_{i,SG}(V_{SG} - V_{th,SG})\mu_{4p,SG} \quad (3)$$

where $\mu_{4p,BG}$ and $\mu_{4p,SG}$ are the four-probe mobilities for bottom- and side-gate modulations, respectively.

$\mu_{4p,BG}$ from dual-gate operations could then be estimated from the high V_{BG} ranges, where σ_{4p} is mostly proportional to V_{BG}, at each fixed V_{SG}. The $\mu_{4p,BG}$ values within small hysteresis loops were extracted by fitting to Fig. 5c by using Equation 1 (an example is shown in Fig. 5c by a black broken line), which are plotted with standard deviations as a function of V_{SG} in Fig. 5f. Although $\mu_{4p,BG}$ at small V_{SG} could not be properly determined due to a measurement issue, high $\mu_{4p,BG}$ values of >10 cm^2 V^{-1} s^{-1} were estimated in $-V_{SG} \geq 0.8$ V. Interestingly, in response to charge accumulation at the upper surface by EDL, $\mu_{4p,BG}$ exhibited an increase to 14.7 cm^2 V^{-1} s^{-1} at V_{SG} = −1.4 V, followed by a decrease with an increase of $-V_{SG}$. Interestingly, the maximum $\mu_{4p,BG}$ of 14.7 cm^2 V^{-1} s^{-1} is 1.5 times greater than that from the conventional OTFT operation. According to the multiple trap-and-release transport model,[39,40] this could be attributed to a close-to-ideal, disorder-free charge transport layer produced by filling both shallow and deep traps by strong electric field *via* EDL. Since the decrease in $\mu_{4p,BG}$ at larger $-V_{SG}$ is attributable to carrier scattering and/or charge trapping caused by ionic components as mentioned above, a competition between these positive and negative effects granted the peak structure in Fig. 5f. Note that this transport layer not only encompasses the channel regions, but also the source/drain contact regimes by EDL-derived trap filling through a separating layer of long alkyl chains.[10,25] Therefore, in the present dual-gate system, the upper and lower surfaces of the two-molecules-thick single crystal primarily contribute to individual operations as an EDLT and a bottom-gate OTFT, respectively. In addition, some favorable interactions could be granted from the EDL to bottom-gate OTFT properties depending on the strength of EDL, such as reduced contact resistances and trap-filling effects (Fig. 6).

Conclusions

In conclusion, we reported individual and dual-gate OTFT properties based on solid and ionic gel gate dielectrics and a single, ultrathin single crystal of C_{10}–DNT–VW in conjunction with the four-probe architecture. Individual OTFT measurements showed the hole mobilities of 9.3 and 2.2 cm^2 V^{-1} s^{-1} with the solid and ionic gel gating, respectively. The lower EDLT mobility is attributed to carrier scattering and/or trapping due to the ionic gate dielectric components. Under the dual-gate operation, the hole mobility was effectively and synergistically enhanced up to 14.7 cm^2 V^{-1} s^{-1}, which is 1.5 times greater than that of the individual OTFT at room temperature maybe due to the close-to-ideal trap-filling effects by the strong EDL. Hence, the present dual-gate OTFT geometry can be used to study the intrinsic charge-carrier mobility of a variety of OSCs which have a high ionization potential (possibly, a low electron affinity for n-type OSCs as well) and a large threshold voltage in their OTFTs.

Author contributions

J. T. conceived the project. T. W. performed device fabrication and measurements. S. K. and N. K. supervised experiments and analyses. Y. Y. and S. W. gave suggestions of analyses. T. O. designed and supplied semiconducting material. S. K. wrote the first draft. All the authors discussed and reviewed the manuscript.

Conflicts of interest

There are no conflicts to declare.

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