Nanoscale

Optical Control of Ferroelectric Switching and Multifunctional Devices Based on van der Waals Ferroelectric Semiconductors

Journal:	*Nanoscale*
Manuscript ID	NR-COM-09-2020-006872.R1
Article Type:	Communication
Date Submitted by the Author:	12-Nov-2020
Complete List of Authors:	Xu, Kai; University of Illinois at Urbana-Champaign, Jiang, Wei; University of Minnesota Gao, Xueshi; University of Illinois at Urbana-Champaign Zhao, Zijing; University of Illinois at Urbana-Champaign, Electrical and Computer Engineering Low, Tony; University of Minnesota Zhu, Wenjuan; University of Illinois at Urbana-Champaign, Electrical and Computer Engineering

SCHOLARONE™
Manuscripts

Optical Control of Ferroelectric Switching and Multifunctional Devices Based on van der Waals Ferroelectric Semiconductors

Kai Xu[1], Wei Jiang[2], Xueshi Gao[1], Zijing Zhao[1], Tony Low[2] and Wenjuan Zhu[1]*

[1]Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801, USA

[2]Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, Minnesota 55455, USA

ABSTRACT: Indium Selenide (In_2Se_3) is a newly emerged van der Waals (vdW) ferroelectric material, which unlike traditional insulating ferroelectric materials, is a semiconductor with a bandgap of about 1.36 eV. Ferroelectric diodes and transistors based on In_2Se_3 have been demonstrated. However, the interplay between light and electric polarization in In_2Se_3 has not been explored. In this paper, we found that the polarization in In_2Se_3 can be programmed by optical stimuli, due to its semiconducting nature, where the photo generated carriers in In_2Se_3 can alter the screening field and lead to polarization reversal. Utilizing these unique properties of In_2Se_3, we demonstrated a new type of multifunctional device based on 2D heterostructures, which can concurrently serve as a logic gate, photodetector, electronic memory and photonic memory. This dual electrical and optical operation of the memories can simplify the device architecture and offer additional functionalities, such as ultrafast optical erase of large memory arrays. In addition, we show that dual-gate structure can address the partial switching problem commonly observed in In_2Se_3 ferroelectric transistors, as the two gates can enhance the vertical electric field and facilitate the polarization switching in the semiconducting In_2Se_3. These discovered effects are of general nature and should be observable in any ferroelectric semiconductors. These findings deepen the understanding of polarization switching and light-polarization interaction in semiconducting ferroelectric materials and open up their applications in multifunctional electronic and photonic devices.

Van der Waals (vdW) ferroelectric materials emerged in recent years as a new class of ferroelectric materials.[1-3] Contrary to traditional ferroelectric materials such as perovskite compounds, vdW ferroelectric materials are free from dangling bonds and offer additional merits such as bandgap tunability, mechanical flexibility, and high carrier mobility.[1, 4-5] More importantly, they can be synthesized on common substrates and allow for easy integration with general semiconducting materials. Therefore, these new vdW ferroelectrics are not only scientifically intriguing but also promising for applications, including nanosensors, actuators, non-volatile memories, and multifunctional devices.

In_2Se_3 is a recently discovered vdW ferroelectric material.[6-11] Unlike SnTe which has narrow bandgap (0.18 eV in bulk)[12] and CIPS which has wide bandgap (2.9 eV),[13] In_2Se_3 has a semiconducting gap (1.36 eV α-phase).[14] Ferroelectric diodes and memristive devices based on In_2Se_3 and graphene were demonstrated.[9, 15-16] Back-gate ferroelectric field-effect transistors (FETs) with In_2Se_3 as the channel have been realized. [17] However, the In_2Se_3 FETs with thick gate oxides show clockwise hysteresis loops (opposite direction to the ferroelectric hysteresis), due to partial polarization switching in In_2Se_3.[17] In this paper, we show that sandwiching In_2Se_3 between two sets of gates can address this problem. By enhancing the vertical electric field across In_2Se_3, full control of polarization switching in In_2Se_3 can be achieved. More importantly, the interplay between light and polarization in In_2Se_3 has not been explored so far. In this work, we discovered that light can induce polarization reversal in In_2Se_3. The mechanism of the photo-induced polarization reversal is proposed. Furthermore, we demonstrated for the first time multifunctional devices based on In_2Se_3 heterostructures, which can concurrently serve as a logic gate, photodetector, electronic memory and photonic memory.

Electrical control of polarization switching

The electrical control of polarization switching in In_2Se_3 was investigated using metal/In_2Se_3/metal and graphene/In_2Se_3/metal structures. α-In_2Se_3 nanosheets are mechanically exfoliated on the highly doped silicon substrate. The crystal phase of the In_2Se_3 flake was confirmed by Raman and photoluminescence (PL) measurements, as shown in Fig. S1 in supplementary information. The local piezoelectric loops of In_2Se_3 were measured by switching spectroscopy piezoresponse force microscopy (SS-PFM), as shown in Fig. 1a. The phase shows sharp change up to 180° and the amplitude shows butterfly-like voltage dependence, which are

typical characteristics for ferroelectric materials. The domain switching in In_2Se_3 was further investigated by PFM mapping. A box-in-box pattern was written using conductive atomic force microscopy (CAFM) with opposite sample voltages (−7 and +7 V). Fig. 1b and 1c show the topography and PFM phase images of an In_2Se_3 flake after the write operation. In the ±7 V region, the out-of-plane phases of the In_2Se_3 are about ±90º respectively, corresponding to the polarization up and down states respectively. The resistive switching in metal/In_2Se_3/metal structures was investigated by CAFM. Figure 1d shows the IV curves taken in the regions programmed with −6 V and +6 V, which exhibit rectifying behavior. When the sample bias is positive, the current after +6 V programming is significantly higher than that after −6 V programming. The current mapping also manifests two distinct current states, as shown in the inset of Fig. 1d. More importantly, the on/off ratio for the ferroelectric diodes at 2 V is more than 10^2. Furthermore, vertical ferroelectric Schottky diodes based on In_2Se_3/graphene vdW heterostructure were also fabricated as shown in Fig. 1e. After a 5 V write pulse, the DC IV of the vertical diode exhibits forward rectifying behavior, while after a −5 V write pulse, it shows reverse rectifying behavior. Both the write and read voltages were applied on the metal electrode (drain terminal). These results indicate that the polarization in In_2Se_3 can affect the Schottky barrier height and switch the diode polarity. The energy band diagrams are shown in Fig. 1f and 1g to explain the reversible rectifying current behavior. When a 5 V write voltage is applied on the metal electrode, the ferroelectric polarization points from metal to graphene, which will raise the Fermi level and induce n-doping in graphene. Subsequent application of positive read bias at the metal would then induce the required band bending in the In_2Se_3, allowing for electrons injection from graphene. When a negative pulse is applied, the polarization of In_2Se_3 switches direction, thus barrier height on the graphene side increases while that on the metal side decreases. As a result, electrons are easier to inject from the metal side, changing the forward to reverse rectifying behavior. The calculated band structures of In_2Se_3-graphene heterostructures under two different polarization directions are shown in Fig. S2 in supplementary information.

Utilizing the electrical controlled polarization and the semiconducting nature of In_2Se_3, we can fabricate ferroelectric In_2Se_3 transistors. Different from traditional ferroelectric transistors where the ferroelectric layer serves as the insulator, here the ferroelectric semiconducting In_2Se_3 serve as the channel. The polarization in In_2Se_3 can induce mobile screening carriers, which can participate the current transport in the transistor. By modulating the direction and amplitude of the

polarization in In_2Se_3, we can control the carrier type/concentration and thus the drain current of the transistor. Recently, back-gated ferroelectric In_2Se_3 transistors were demonstrated, [17] however, trap-like hysteresis window was observed due to partial polarization switching in In_2Se_3 transistors, especially in the transistors with thick oxide. In the back-gate structure, only part of the In_2Se_3 channel is sandwiched between the source (or drain) electrode and back-gate, so there is not enough vertical electric field to completely switch the polarization in the In_2Se_3 channel, illustrated in Fig. 2a. To address this problem, we propose to use dual-gate structure, illustrated in Fig. 2b. The top and embedded gates will induce a vertical electrical field across the entire In_2Se_3 channel to ensure the sufficient polarization switching. Using this structure, we were able to observe large ferroelectric windows in the In_2Se_3 transistors. Fig. 2c shows the transfer characteristics of a double-gated In_2Se_3 transistor measured at 7 K after applying program pulses with various amplitudes. The program pulses were applied on the top gate with the back gate grounded. When the program pulse amplitude exceeds 20 V, the transfer curves shift toward opposite directions after positive and negative program pulses, which can be attributed to the ferroelectric polarization switching in In_2Se_3. The details of the measurement are shown in Fig. S3. Large memory window (~1 V) and high current ratio (~10^4) between the two ferroelectric polarization support their robust function as memory states. The threshold voltages (V_{th}) and drain currents (I_d) at back-gate voltage of 1 V were extracted and plotted as a function of program pulse amplitude (Fig. 2d). The threshold voltage decreases and the drain current increases with increasing program voltage, indicating excellent non-volatile tunability of the electrical characteristics of In_2Se_3 transistors, through ferroelectric domains switching. The transfer curves measured at various temperatures all exhibit large and stable ferroelectric memory window (Fig. S5).

The ferroelectric windows in the In_2Se_3 transistors were also analyzed using electrostatic model. The semiconducting nature of In_2Se_3 implies the presence of conducting free carriers, which can be induced by the polarization charges, and is responsible for the observed device current. Figure 2e and 2f show the energy diagrams of the device, depicting the charge densities at the metallic gates (Q_m), the polarization charges in the ferroelectric In_2Se_3 (Q_{FE}), as well as the free carriers within the semiconducting ferroelectric vdW layers denoted as (q_i). The latter requires proper electrostatic analysis, which differs from the analysis of traditional three-dimensional (3D) ferroelectric materials. Due to relatively weak vdW stacking, the bandgap of individual layers remains relatively unchanged in multilayers (Fig. S6). Therefore, the induced charges within the

ferroelectric semiconductor can be treated as discretely distributed charge layers q_i near the In_2Se_3 interfaces. Due to electrostatic screening, these q_i decrease away from the interface, where the out-of-plane electric field is the largest, as depicted in the Fig. 2e and 2f. The charge distribution within the ferroelectric In_2Se_3 can be obtained for a given potential profile by minimizing the total energy $U = U_{el} + U_b$, in which U_{el} and U_b represent the electrostatic interaction between layers and the band-filling energy, respectively. However, the solution for the discretely distributed charges q_i should be solved self-consistently with Poisson's equation, $\nabla^2 \phi = -\rho/\varepsilon$, with the boundary condition enforced by the work function difference between metal and ferroelectric materials. From this, we can get the complete charge distribution profile, electric field and potential profile of the dual gate device. For simplicity, we consider the case where the In_2Se_3 has no residual doping and the two metal contacts are the same.

Figure 2g shows the modeled charge components as a function of the program pulse voltages. The initial charge density on the metal without polarization Q_{m0} was solved using electrostatic model, while the change of the charge density on the metal due to polarization ΔQ_m was estimated from the threshold voltage shift after program pulses, which was measured experimentally, as depicted in Fig. 2c and 2d. With the total charge density on the metal ($Q_m = Q_{m0} + \Delta Q_m$), we solved for the polarization charge density Q_{FE} and free carrier density q_i self-consistently using the electrostatic model described above (details of the modeling are in Supplementary Information). The screening charges obtained are on the order of 10^{12} cm^{-2} when the magnitude of the pulse voltage is larger than 20 V, which constitutes the ON-state of the In_2Se_3 semiconductor channel.

In making the comparison with experiments, we reiterate the observation that the ferroelectric polarization for the +25 V pulse renders a negative shift in threshold voltage, which means more electron-doped, as compared to the −25 V case. These observations are consistent with the scenario that only the bottom channel is conducting. The asymmetry in the conduction can be explained by the different top/bottom gate and source/drain metals. The choice of Au for bottom gate, in conjunction to Ti as the source/drain contacts render it an Ohmic contact to electrons in In_2Se_3. The fact that the transistor transfer curves reveal only electron carrier conduction is due to the low work function Ti contact at source/drain, which provides low injection barrier for electrons. In addition, the drain voltage applied is 0.1 V, which is far below the coercive voltage for the in-plane ferroelectric polarization.[16]

Furthermore, we studied the pulse width and amplitude dependence of the memory window. Figure 3a shows the transfer curves of a dual-gate In_2Se_3 transistor after +25 V and −25 V program pulses. When the pulse width scales down from 200 ms to 40 ns, the memory window is nearly unchanged. These results ruled out the possibility of hysteresis effects arising from slow moving mobile ions. In addition, the memory window shows a step function of the program pulse amplitude and has a sharp transition at ~20 V (Fig. S3c), which corresponds to the coercive field of 0.12 V/nm in the ferroelectric In_2Se_3. This result indicates that the memory window is due to ferroelectric polarization instead of interface traps. We also systematically characterized the retention and endurance of the In_2Se_3 memory devices. The threshold voltages were plotted as a function of retention time, shown in Fig. 3c. At room temperature, over 90% of the memory window remains after extrapolation to 10 years. The endurance of the In_2Se_3 memory is shown in Fig. 3d. The memory window was nearly unchanged after 120 cycles. These results indicate that the ferroelectric devices based on In_2Se_3 have excellent reliability.

Optical control of polarization switching and multifunctional devices based on In_2Se_3

Most traditional ferroelectric materials are insulators with wide bandgaps, such as Pb $(Zr,Ti)O_3$, (PZT) with bandgap of 3.3~3.55 eV and $BiFeO_3$ with a bandgap of 2.7 eV. The absorption spectrum of these wide bandgap materials does not fully address the visible light range. In contrast, In_2Se_3 has a much smaller bandgap (1.36 eV in bulk), which is photoactive to the entire visible spectrum.[25,26] Combining the photoactive, ferroelectric and semiconducting properties of In_2Se_3, we can create multifunctional devices, which can detect light, and process these optical signals simultaneously. Here, dual-gate In_2Se_3 devices were fabricated with multi-layer graphene as the transparent top electrode to facilitate the light absorption. The device structure is shown in Fig. 4a. Electrical and optical pulses were applied on the device sequentially and the drain current was measured as a function of time, as shown in Fig. 4b. In addition, the transfer characteristics were tested after electrical pulse, during light illumination and after light removal (corresponding to the time points #1 to #6 marked in Fig. 4b). As shown in Fig. 4c, the polarization of the In_2Se_3 was programmed by the electrical pulses and a large memory window was observed after ±25 V pulses, which is consistent with the dual-gate In_2Se_3 devices with metal top electrodes discussed in the previous section. The threshold voltage after +25 V pulse is around −1 V, corresponding to the downward polarization (P_{down}) in In_2Se_3, while the threshold voltage after −25 V pulse is

around 0.2 V, corresponding to the upward polarization (P_{up}) in In_2Se_3. As a result, the drain current at zero gate voltage is high after a +25 V pulse and low after a -25 V pulse, as shown in Fig. 4b. Moreover, this device is very sensitive to light, exhibiting an excellent photoresponse, as shown in Fig. 4d. The drain current increased dramatically when the device was illuminated with mild lamp light (4400 $\mu W/cm^2$). More interestingly, after the light was removed, all the transfer curves exhibit a threshold voltage around −1 V, regardless of whether the device was programed with a +25 V or −25 V pulse previously, as shown in Fig. 4e. This means that light can erase the polarization of In_2Se_3 to P_{down} state and reset the threshold voltage of the dual-gate In_2Se_3 device. The time evolution of the drain current in Fig. 4b confirms that the device was set to an "On" state (high drain current) by the light illumination and remains at the "On" state even after the light removal. This photo-induced polarization reversal was also observed in MoS_2/PZT stacks previously.[18-19] Figure S7 shows the photo-induced polarization switching in other In_2Se_3 transistors. These results indicate that this effect is repeatable and reliable. The cyclic operation with electrical pulses and light illumination were conducted as shown in Fig. 4f. It clearly displays the excellent periodic modulation of the drain current induced by the electrical and light stimuli. Time evolution of the drain current with various light intensities was also tested as shown in Fig. S8. It took longer time for the light with low intensity to neutralize the screening charges and reset the polarization as compared to the light with high intensity.

In the following, we propose a physical mechanism for this photo-induced polarization reversal and threshold voltage reset in In_2Se_3 devices. In this dual-gate device, due to the work function difference between the top graphene electrode and the bottom gold electrode, a built-in electric field pointing toward the bottom electrode exists under equilibrium, as illustrated in Fig. 4g. This built-in electric field will induce an imprint in In_2Se_3 with P_{down} being the preferred polarization state. This polarization state can be reversed, however, under a high electric field. When a −25 V pulse is applied on the top gate, the polarization of the In_2Se_3 is switched to the upward direction (P_{up}) and the threshold voltage shifts to around 0.2 V, as shown in Fig. 4b. Since In_2Se_3 is a semiconductor, a P_{up} polarization will attract negative (positive) screening charges at the top (bottom) surface. These screening charges result in an electric field E_{sc} pointing upward, which will help to stabilize the polarization, as shown in Fig. 4h. When light is illuminated on the sample, the photo-generated carriers will neutralize the negative and positive screening charges at the surfaces and significantly reduce the electric field E_{sc}. Then the depolarization field from the

polarization charges and the built-in electric field will reverse the polarization from P_{up} to P_{down}, as illustrated in Fig. 4i. As a result, the transfer curve with the −25 V program pulse after light illumination shifts back to around −0.7 V, corresponding to a P_{down} polarization, as shown in Fig. 4d. The fact that the threshold voltages are all around −1 V after removing light regardless the program voltages further confirms that P_{down} polarization is the preferred polarization state.

Combining the electrical and optical control of the polarization, we demonstrate multifunctional devices based on vdW ferroelectric In_2Se_3, which can serve as a logic switch, photodetector, electronic memory, and photonic memory concurrently, as illustrated in Fig. 5. The ferroelectric semiconducting channel based on In_2Se_3 enables the device to response actively to both electrical and optical stimuli. The dual-gate structure ensures efficient electrical control of the polarization in the ferroelectric channel. Transparent graphene electrode facilitates light absorption of the ferroelectric channel, which can induce not only photocurrent but also polarization reversal in the In_2Se_3. For photonic memory, the memory array can be reset electrically to P_{up} state (ON state), then the data can be written optically by illuminating individual devices using a focused light source such as a laser to switch the polarization of the In_2Se_3 to P_{down} state (OFF state) (Fig. 5b). For electronic memory, the polarization of In_2Se_3 is programmed using electrical pulses. The erase operations can be carried out either electrically or optically (Fig. 5d). In the electrical erase operation, the polarization of In_2Se_3 is reset by applying pulses between the top and bottom gates. In the optical erase operation, the polarization of In_2Se_3 in the entire memory block can be reset to P_{down} state (OFF state) simultaneously by light illumination. As compared to electrical erase, which is carried out sequentially on individual device(s), optical erase is a parallel process and is much faster. In addition, these devices can also serve as electrical switches where the drain current is controlled by the gate voltage, and as optical switches/photodetectors where the drain current is modulated by the light illuminating the device. This dual electrical and optical operation of the memories can simplify the device architecture and offer additional functionalities, such as an ultrafast optical erase of large memory arrays. Traditionally, ferroelectric devices are used in memory blocks while non-ferroelectric transistors are used for logic blocks in central processing units (CPUs). The memory and logic blocks are physically separated. Here, due to the ferroelectric and semiconducting nature of In_2Se_3, an In_2Se_3-based transistor enables the realization of memory and logic functions in one device. These logic-in-memory devices can potentially reduce the data transportation between memory and logic blocks and thus reduce the energy

consumption and process latency. Moreover, traditional ferroelectric materials are insulators with large bandgaps (2-4 eV), while In_2Se_3 has a small bandgap of 1.36 eV, which is photoactive to the entire visible spectrum. This implies that In_2Se_3 devices can sense the light signal, process the signal in-situ, and store the information locally, which enables in-sensor computing. These devices will have broad applications in sensor networks and un-manned vehicles.

In summary, we found that the polarization states of the In_2Se_3 can be programmed by both electronic pulse and optical illumination. Through DFT calculations and electrostatic analysis, we revealed the underlying physical mechanisms that explain the experimental observation and could be generalized to other 2D ferroelectric semiconductors. Furthermore, we demonstrated multifunctional device based on In_2Se_3, which can serve as logic gate, electronic memory, photodetector, and photonic memory simultaneously for the first time, Large memory window (~2.3V) and a high current ratio (~10^4) between two memory states (±25 V) were realized. These electronic and photonic memories are non-volatile and energy efficient. A single device, which can detect light, store information and process electrical signals, will not only increase the packing density of the circuit, but also enable in-sensor and in-memory computing architecture, which can significantly reduce the latency and energy consumption related to the data movement. These results indicate that 2D ferroelectric In_2Se_3 and its heterostructures are an excellent platform for future multifunctional electronics and optoelectronics.

Methods

Material Characterization: In_2Se_3 ultrathin flakes were mechanically exfoliated from bulk In_2Se_3 (HQ graphene) using the typical Scotch tape method, and then transferred by gel film. The crystal structure and optical bandgap of In_2Se_3 were examined using a confocal Raman microscope (Renishaw, 532 nm excitation laser). The thickness, surface morphology, local ferroelectric properties and current mapping were obtained using an Asylum Research Cypher scanning probe microscope and MFP-3D systems.

Device Fabrication and Measurements: Electrical devices were fabricated by standard lithography and metal deposition. Electrical measurements were conducted in Lakeshore probe station (CPX-VF) connected to Keysight B1500 parameter analyzer. The photoelectric measurements were performed in our home-made optical systems.

DFT Calculation: The total-energy electronic-structure calculations were carried out using first-principles methods based DFT. The generalized gradient approximation exchange-correlation potentials plus the projector augmented wave method for the electron-ion interaction was used,[20] as implemented in Vienna *ab initio* simulation package (VASP) code.[21] The In_2Se_3 thin film slabs were cleaved from the bulk α-In_2Se_3 structure with a lattice constant of 4.106 Å. The heterostructures of In_2Se_3/graphene were constructed using a 3x3/5x5 supercell to have a relatively small lattice mismatch. To avoid interaction between slabs, a vacuum region of more than 15 Å was introduced for the slab systems. DFT-D3 method is applied to properly treat the Van der Waals interaction between layers.[22] An electric field is applied along the *z* direction with the dipole corrections performed to avoid interactions between the periodically repeated images due to the intrinsic ferroelectricity of the In_2Se_3.[23] All self-consistent calculations were performed with a plane-wave cutoff of 500 eV. The geometric optimizations were carried out without any constraint until the force on each atom is less than 0.01 eV/ Å and the change of total energy per cell is smaller than 10^{-5} eV. The Brillouin zone k-point sampling was set with a $12 \times 12 \times 1$ Γ-centered Monkhorst-Pack grids. Bader charge analysis was performed to study the charge transfer within and between In_2Se_3 layers.

ASSOCIATED CONTENT

Supporting Information. The more details of characterizations and simulation of devices.

AUTHOR INFORMATION

Corresponding Author

Wenjuan Zhu - Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801, USA; Email: wjzhu@illinois.edu
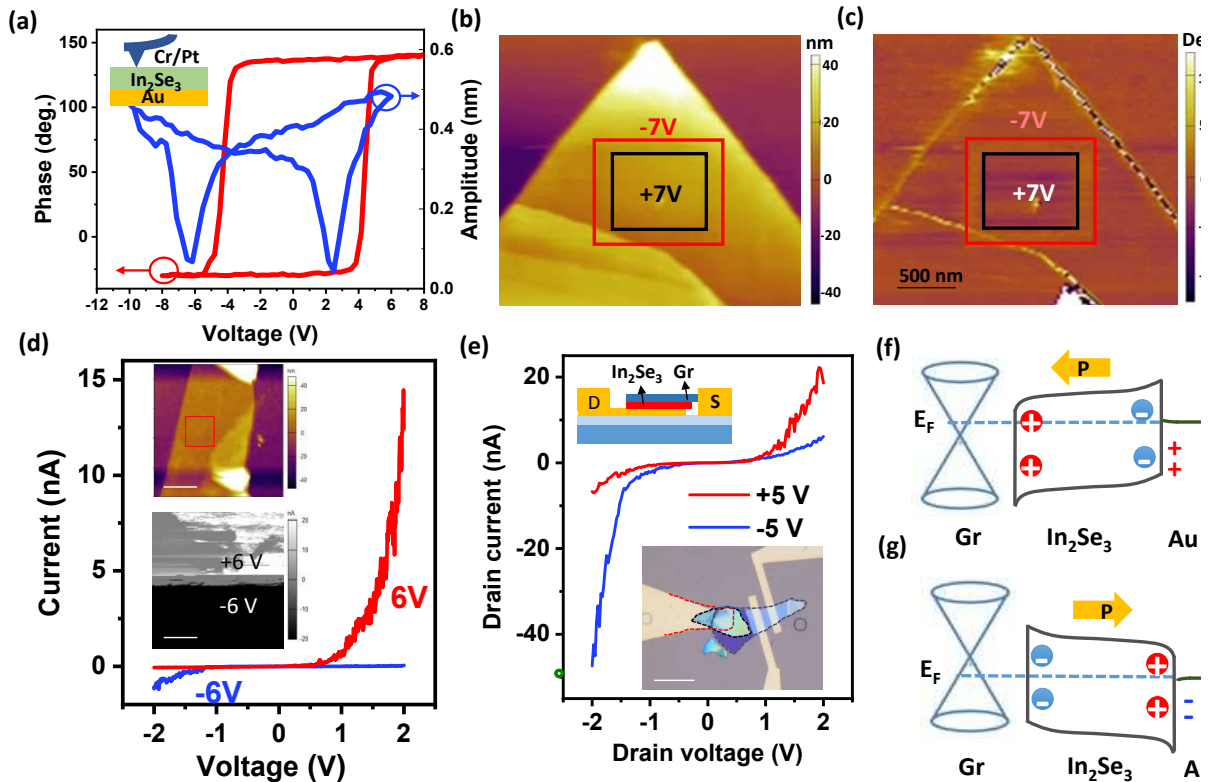
Figure 1. Electrical control of polarization switching in In$_2$Se$_3$. (a) Local hysteresis loop of 27 nm In$_2$Se$_3$ measured by SS-PFM. The 180° reversal for phase and "butterfly" curve for amplitude confirm the piezoelectricity of In$_2$Se$_3$. The sample structure is illustrated in the inset. (b) Topography and (c) PFM phase image of a 36 nm In$_2$Se$_3$ flake in a PFM measurement. In (b), an illustration of the box-in-box pattern is overlaid on the topography image. In (c), the phase contrast indicates the polarization direction is switched by external electric field. (d) IV curves measured by CAFM at regions programmed with −6 V and 6 V respectively. The inset shows the topography of the In$_2$Se$_3$ flake (top) and current mapping of the −6 V and +6 V programmed regions (bottom). The scale bars are 1 μm and 200 nm respectively. (e) The IV characteristics of a vertical ferroelectric Schottky diode based on In$_2$Se$_3$/graphene heterostructure. The schematic and optical image of the device are shown in the insets. By switching the polarization with +5 V and −5 V applied on the gold terminal, the IV curves manifest forward and reverse rectifying behavior respectively. The scale bars are 20 μm. (f)

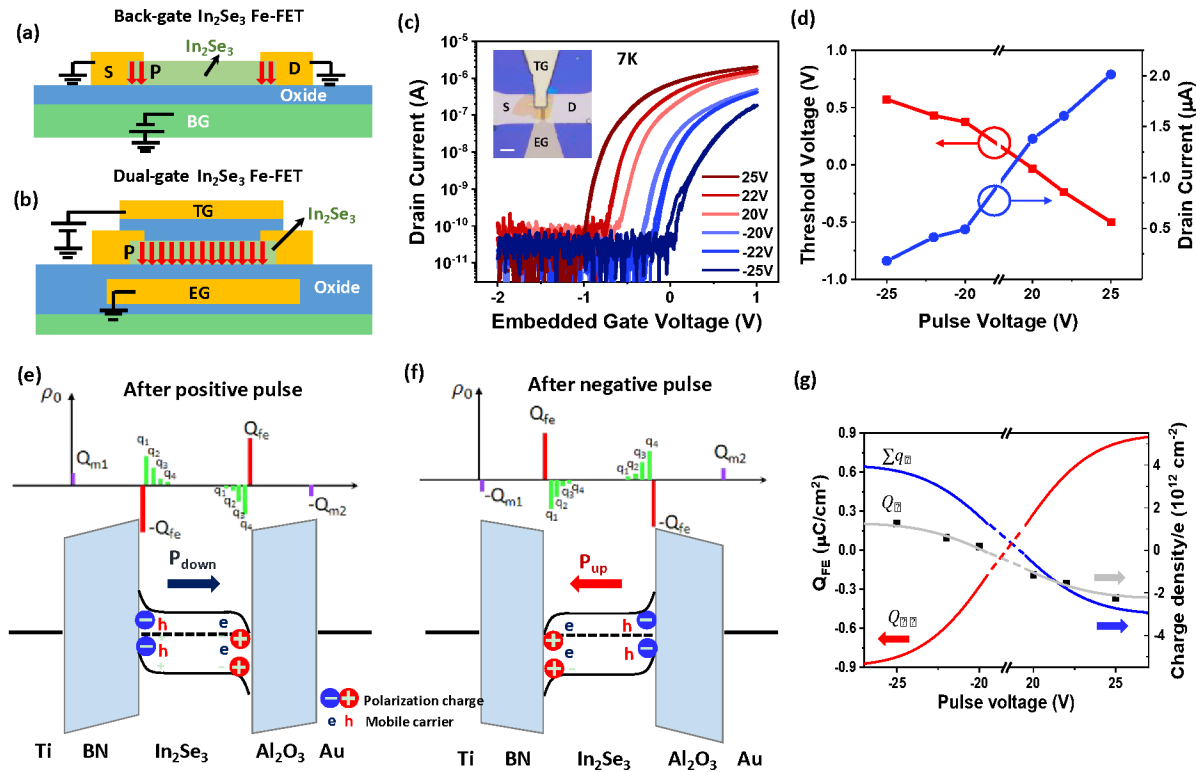**Figure 2.** Electrical memories based on ferroelectric In_2Se_3. (a) Illustration of a back-gate In_2Se_3 transistor. Applying a voltage between the back gate and the source/drain terminals leads to a partial switching of polarization in In_2Se_3. (b) Illustration of a dual-gate In_2Se_3 transistor, where the ferroelectric In_2Se_3 channel is sandwiched between the top and bottom gates with insulators in between. Applying a voltage between the top and bottom gates leads to a vertical electric field across the In_2Se_3 channel, which can effectively switch the polarization in In_2Se_3. (c) Transfer characteristics after various program pulses at 7 K shows large memory window (~1V) and high current ratio (~10^4) between two memory states (±25 V). The inset shows the optical image of the device and the scale bar is 10 μm. (d) The threshold voltage and drain current at back-gate voltage of 1 V are extracted and plotted as a function of program pulse voltages. The monotonic decrease of the threshold voltage and increase of the drain current as the pulse voltage increases indicate excellent ferroelectric tunability of the electrical properties of In_2Se_3 FETs. (e) and (f) The schematic band diagrams of the dual metal gate device with the polarization direction pointing to the right and left respectively. (g) Simulated polarization charge density (Q_{FE}, red) and free carrier density in In_2Se_3 (q_i, blue) as a function of program pulse voltage based on the estimated charge density near the metallic surface (Q_m, gray line and black dots).
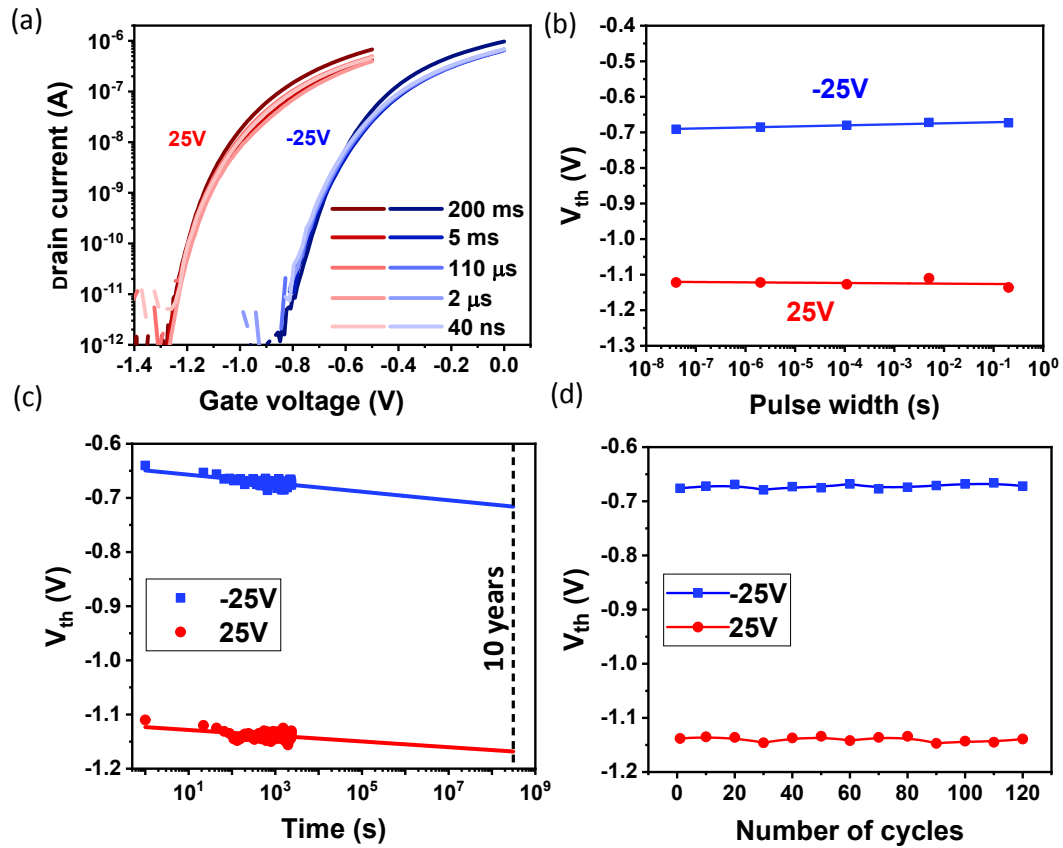
Figure 3. Memory window of a dual-gate In_2Se_3 transistor. (a) The transfer curves of the dual-gate In_2Se_3 transistor measured using various program pulse voltages and widths. (b) Threshold voltage of the dual-gate In_2Se_3 transistor as a function of program pulse width. When the pulse width scales down from 200 ms to 40ns, the memory window is nearly unchanged, indicating that the memory window is due to ferroelectric polarization instead of mobile ions. (c) The retention and (d) endurance of the In_2Se_3 transistor. The extrapolated retention time is over 10 years. The measurement temperature is 50 K for (a)-(d).
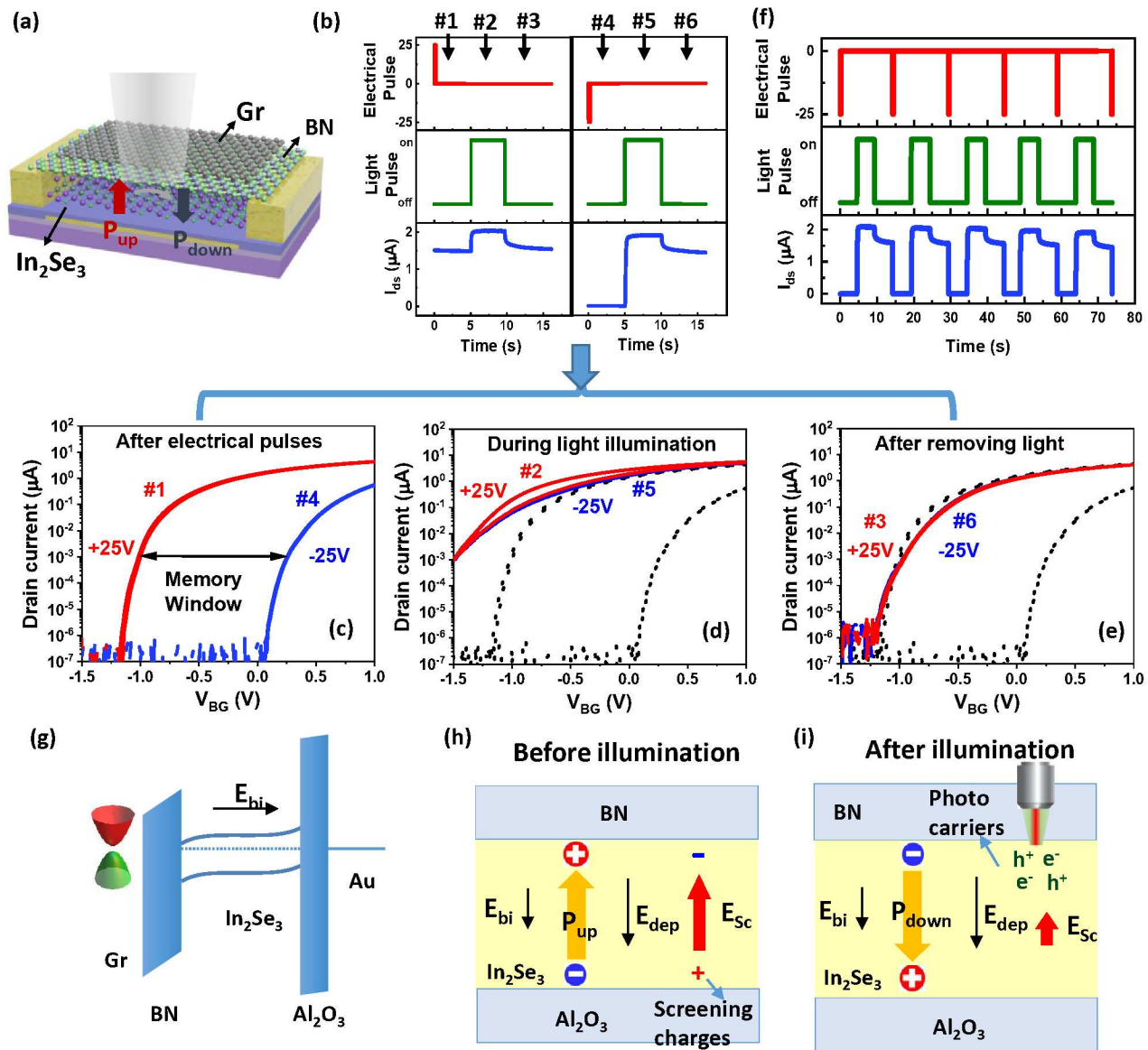
Figure 4. Optical control of polarization switching in In_2Se_3. (a) Illustration of the dual-gate In_2Se_3 device with graphene top electrode. (b) Programming and erasing the In_2Se_3 memory using electrical pulses (± 25 V) and light illumination. The width of the electrical pulse is 200 ms. The light intensity is 4400 $\mu W/cm^2$. (c) Transfer characteristics of the device after ± 25 V program pulses, showing clear memory window. (d) The transfer characteristics of the device during the light illumination. (e) Transfer curves of the device after removing the light. In (d) and (e), the red and blue lines correspond to the device previously programmed with $+25$ V and -25 V pulses respectively. For comparison, the transfer curves before the light illuminations are also included as the dashed black lines in (d) and (e). (f) The cyclic operations of the memory device with electrical pulses and light illumination show reproducible modulation of the drain current. (g) Energy diagram of the dual-gate In_2Se_3 device at equilibrium. The built-in electric field, E_{bi}, is pointing to the bottom electrode. (h) and (i) Illustrations of the polarization and electric field in In_2Se_3 after -25 V pulse before and after light illumination respectively. (h) Before light illumination, P_{up} develops after -25 V pulse is applied on the top gate. The depolarization field due to the polarization charge, E_{dep}, is balanced by the electric field due to the screening charges, E_{sc}, thus the polarization is stabilized. (i) After light illumination, photo-generated electrons and holes neutralize the screening charges at the surfaces and weaken the screening field E_{sc}. The built-in electric field, E_{bi}, and the depolarization field induced by the polarization charge, E_{dep}, reverse the polarization from P_{up} to P_{down} in In_2Se_3.
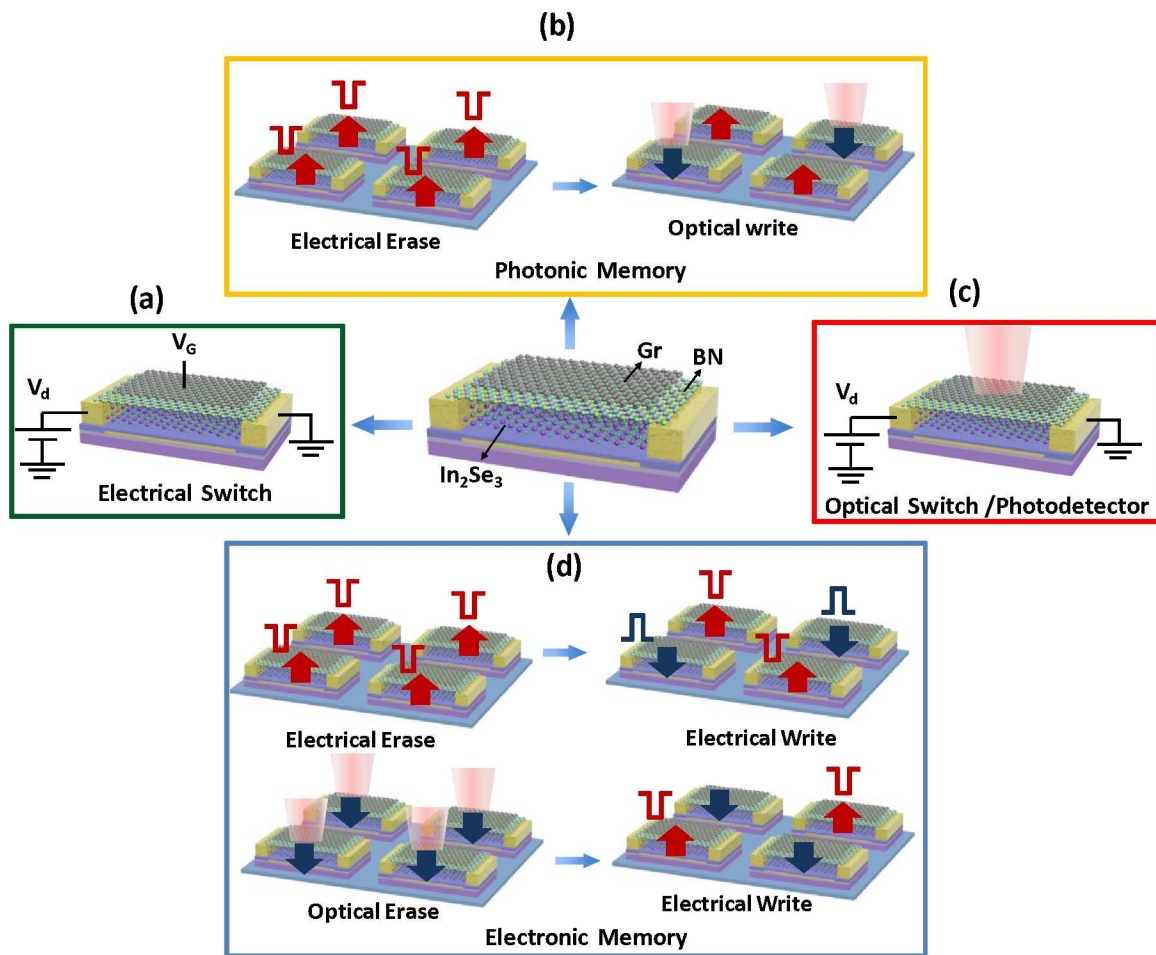
Figure 5. Illustration of the multifunctionality of the dual-gate In_2Se_3 transistor with transparent electrode. (a) Electrical logic switch, where the drain current is controlled by the gate voltage. (b) Optical memory, which can be erased electrically and programmed optically. The polarization direction of In_2Se_3 is indicated by the arrow (blue downward arrow: P_{down}; red upward arrow: P_{up}.) (c) Optical switch, where the drain current is modulated by the optical illumination. (d) Electrical memory, where the write operation is carried out by applying electrical pulses. The memory array can be erased either electrically or optically. In electrical erase operation, the devices are addressed individually and the polarization of In_2Se_3 can be reset by applying pulses on the top and bottom gates. In the optical erase operation, the polarization of In_2Se_3 in the entire memory block can be reset to P_{down} state simultaneously by light illumination.

REFERENCES

1.   Cui, C. J.; Xue, F.; Hu, W. J.; Li, L. J., Two-dimensional materials with piezoelectric and ferroelectric functionalities (vol 2, 18, 2018). *Npj 2d Materials and Applications* **2018,** *2*.

2.   Wu, M. H.; Jena, P., The rise of two-dimensional van der Waals ferroelectrics. *Wiley Interdisciplinary Reviews-Computational Molecular Science* **2018,** *8* (5).

3.   Chang, L.; You, L.; Wang, J. L., The path to flexible ferroelectrics: Approaches and progress. *Japanese Journal of Applied Physics* **2018,** *57* (9).

4.   Chang, K.; Liu, J. W.; Lin, H. C.; Wang, N.; Zhao, K.; Zhang, A. M.; Jin, F.; Zhong, Y.; Hu, X. P.; Duan, W. H.; Zhang, Q. M.; Fu, L.; Xue, Q. K.; Chen, X.; Ji, S. H., Discovery of robust in-plane ferroelectricity in atomic-thick SnTe. *Science* **2016,** *353* (6296), 274-278.

5.   Liu, F. C.; You, L.; Seyler, K. L.; Li, X. B.; Yu, P.; Lin, J. H.; Wang, X. W.; Zhou, J. D.; Wang, H.; He, H. Y.; Pantelides, S. T.; Zhou, W.; Sharma, P.; Xu, X. D.; Ajayan, P. M.; Wang, J. L.; Liu, Z., Room-temperature ferroelectricity in CuInP2S6 ultrathin flakes. *Nat Commun* **2016,** *7*.

6.   Cui, C. J.; Hu, W. J.; Yan, X. G.; Addiego, C.; Gao, W. P.; Wang, Y.; Wang, Z.; Li, L. Z.; Cheng, Y. C.; Li, P.; Zhang, X. X.; Alshareef, H. N.; Wu, T.; Zhu, W. G.; Pan, X. Q.; Li, L. J., Intercorrelated In-Plane and Out-of-Plane Ferroelectricity in Ultrathin Two-Dimensional Layered Semiconductor In2Se3. *Nano Lett* **2018,** *18* (2), 1253-1258.

7.   Zhou, Y.; Wu, D.; Zhu, Y. H.; Cho, Y. J.; He, Q.; Yang, X.; Herrera, K.; Chu, Z. D.; Han, Y.; Downer, M. C.; Peng, H. L.; Lai, K. J., Out-of-Plane Piezoelectricity and Ferroelectricity in Layered alpha-In2Se3 Nanoflakes. *Nano Lett* **2017,** *17* (9), 5508-5513.

8.   Zheng, C. X.; Yu, L.; Zhu, L.; Collins, J. L.; Kim, D.; Lou, Y. D.; Xu, C.; Li, M.; Wei, Z.; Zhang, Y. P.; Edmonds, M. T.; Li, S. Q.; Seidel, J.; Zhu, Y.; Liu, J. Z.; Tang, W. X.; Fuhrer, M. S., Room temperature in-plane ferroelectricity in van der Waals In2Se3. *Science Advances* **2018,** *4* (7).

9.   Wan, S. Y.; Li, Y.; Li, W.; Mao, X. Y.; Zhu, W. G.; Zeng, H. T., Room-temperature ferroelectricity and a switchable diode effect in two-dimensional alpha-In2Se3 thin layers. *Nanoscale* **2018,** *10* (31), 14885-14892.

10.   Poh, S. M.; Tan, S. J. R.; Wang, H.; Song, P.; Abidi, I. H.; Zhao, X.; Dan, J. D.; Chen, J. S.; Luo, Z. T.; Pennycook, S. J.; Neto, A. H. C.; Loh, K. P., Molecular-Beam Epitaxy of Two-Dimensional In2Se3 and Its Giant Electroresistance Switching in Ferroresistive Memory Junction. *Nano Letters* **2018,** *18* (10), 6340-6346.

11.   Si, M.; Saha, A. K.; Gao, S.; Qiu, G.; Qin, J.; Duan, Y.; Jian, J.; Niu, C.; Wang, H.; Wu, W.; Gupta, S. K.; Ye, P. D., A ferroelectric semiconductor field-effect transistor. *Nature Electronics* **2019,** *2* (12), 580-586.

12.   Belianinov, A.; He, Q.; Dziaugys, A.; Maksymovych, P.; Eliseev, E.; Borisevich, A.; Morozovska, A.; Banys, J.; Vysochanskii, Y.; Kalinin, S. V., CuInP(2)S(6) Room Temperature Layered Ferroelectric. *Nano Lett* **2015,** *15* (6), 3808-14.

13.   Studenyak, I. P.; Mitrovcij, V. V.; Kovacs, G. S.; Gurzan, M. I.; Mykajlo, O. A.; Vysochanskii, Y. M.; Cajipe, V. B., Disordering effect on optical absorption processes in CuInP2S6 layered ferrielectrics. *Physica Status Solidi B-Basic Research* **2003,** *236* (3), 678-686.

14.   Bacewicz, R.; Filipowicz, J.; Wolska, A., Optical properties of indium-rich phases in the Cu-In-Se system. *Ternary and Multinary Compounds* **1998,** *152*, 507-510.

15.   Wan, S. Y.; Li, Y.; Li, W.; Mao, X. Y.; Wang, C.; Chen, C.; Dong, J. Y.; Nie, A. M.; Xiang, J. Y.; Liu, Z. Y.; Zhu, W. G.; Zeng, H. L., Nonvolatile Ferroelectric Memory Effect in Ultrathin -In2Se3. *Adv Funct Mater* **2019,** *29* (20).

16.   Xue, F.; He, X.; Retamal, J. R. D.; Han, A. L.; Zhang, J. W.; Liu, Z. X.; Huang, J. K.; Hu, W. J.; Tung, V.; He, R. H.; Li, L. J.; Zhang, X. X., Gate-Tunable and Multidirection-Switchable Memristive Phenomena in a Van Der Waals Ferroelectric. *Adv Mater* **2019,** *31* (29).

17.   Si, M. W.; Saha, A. K.; Gao, S. J.; Qiu, G.; Qin, J. K.; Duan, Y. Q.; Jian, J.; Niu, C.; Wang, H. Y.; Wu, W. Z.; Gupta, S. K.; Ye, P. D. D., A ferroelectric semiconductor field-effect transistor. *Nat Electron* **2019,** *2* (12), 580-586.

18.   Lipatov, A.; Sharma, P.; Gruverman, A.; Sinitskii, A., Optoelectrical Molybdenum Disulfide (MoS2)—Ferroelectric Memories. *ACS Nano* **2015,** *9* (8), 8089-8098.
19.   Li, T.; Lipatov, A.; Lu, H.; Lee, H.; Lee, J.-W.; Torun, E.; Wirtz, L.; Eom, C.-B.; Íñiguez, J.; Sinitskii, A.; Gruverman, A., Optical control of polarization in ferroelectric heterostructures. *Nature Communications* **2018,** *9* (1), 3344.
20.   Kresse, G.; Joubert, D., From ultrasoft pseudopotentials to the projector augmented-wave method. *Physical Review B* **1999,** *59* (3), 1758-1775.
21.   Kresse, G.; Hafner, J., Ab initio molecular dynamics for liquid metals. *Physical Review B* **1993,** *47* (1), 558-561.
22.   Grimme, S.; Antony, J.; Ehrlich, S.; Krieg, H., A consistent and accurate ab initio parametrization of density functional dispersion correction (DFT-D) for the 94 elements H-Pu. *The Journal of Chemical Physics* **2010,** *132* (15), 154104.
23.   Makov, G.; Payne, M. C., Periodic boundary conditions in ab initio calculations. *Physical Review B* **1995,** *51* (7), 4014-4022.