

**Monocrystalline Perovskite Wafer/Thin Film for Photovoltaic and Transistors Applications**

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## Monocrystalline Perovskite Wafer/Thin Film for Photovoltaic and Transistors Applications

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### Abstract

High-purity monocrystalline silicon has a long history in development of photovoltaics and so far has dominated the modern computers with its profound implementations in transistors and chips. The success of silicon has shown that monocrystalline wafers/thin films of semiconducting materials which have superior electronic properties are good platform for these optoelectronic and electronic applications. Recently, the newly emerging semiconducting materials of halide perovskites (*HPs*) have attracted much attention owing to their continuing success in high-efficiency solar cells. Demonstrated optoelectronic properties of *HPs* indicate that it could be a promising alternative to the silicon-based semiconducting industry. While the prerequisite of high-efficiency device is the material accessibility of monocrystalline *HPs* (*mono-HP*), as can be learned from the lessons of monocrystalline silicon. Current *HPs* based technologies, in terms of research areas like solar cells, photodetectors, light-emitting diodes (LEDs), lasers and transistors, are bottlenecked in manufacturing the *mono-HP* wafer/thin film materials, hence lacking exciting results of *mono-HP* devices. The state-of-the-art optoelectronic *HP* based devices are exclusively built using polycrystalline thin films, which are limited in their performance due to issues such as grain boundary defects, large trap-density and inhomogeneous charge transport. However, these issues can be resolved by utilizing *mono-HPs*. In this review, we will manifest in-depth analyses and discussions on the potential of *mono-HPs* in photovoltaics and transistor applications, and present the remaining challenges as well as promising research strategies to provide direction for future programs.

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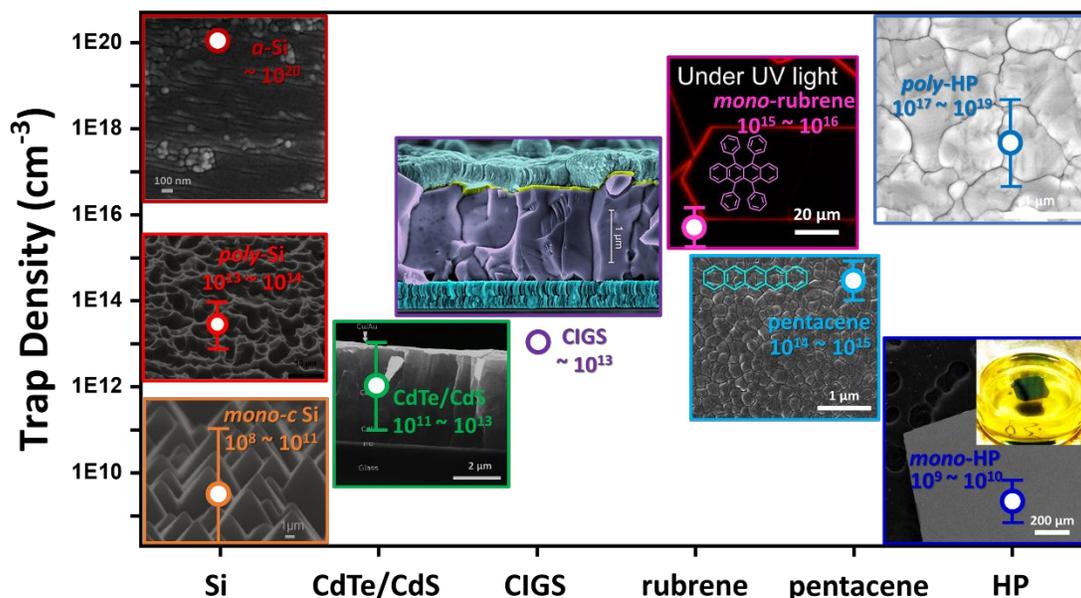
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## 1. Introduction

Owing to its great abundance and mature infrastructure, silicon based solar panels/modules have dominated the photovoltaic technology with over 90% market share.<sup>1,2</sup> High purity monocrystalline silicon is the foundation for the transistors,<sup>3</sup> the basic building blocks of modern computers. Today, silicon-based semiconductor technology is at the heart of the \$1 trillion global electronics industry and is vital in many other areas representing \$33 trillion global economy.<sup>4</sup> However, silicon is reaching saturation in many application areas and this is more obvious in photovoltaics and transistors. Exploring novel semiconductors with superior optoelectronic properties for these platforms is essential for continuing progress. Recent progress on halide perovskites (*HPs*) has provided a new dimension for exploring novel semiconductors. The implementation of *HPs* in photovoltaics has demonstrated solar power-conversion efficiency (PCE) on the order of 25%.<sup>5</sup> This PCE magnitude surpasses that of the polycrystalline silicon (*poly-Si*) photovoltaics (22.3%). *HPs* provide pathway to reach closer towards the Shockley-Queisser limit for single-junction solar cell with a theoretical maximum efficiency of 33.7%.<sup>6</sup>

Currently polycrystalline thin films of *HP* (*poly-HP*) are utilized in demonstrating various applications including photovoltaics and transistors. However, the presence of grain boundaries (GBs), large trap-density ( $n_{trap}$ ), and small grain sizes can compromise the electronic properties. In comparison, GB-free *mono-HPs* possess ultra-long carrier diffusion length up to  $\sim 3$  mm,<sup>7</sup> four orders of magnitude higher than their polycrystalline counterparts (*e.g.*, 90 nm in typical *poly-HP* thin film<sup>8</sup>). The trap-density in *mono-HPs* is on the level of  $10^{10}$  cm<sup>-3</sup>, significantly lower than that of  $10^{17} \sim 10^{19}$  cm<sup>-3</sup> in *poly-HP*,<sup>9,10</sup> and even lower than typical semiconductor materials such as *poly-Si*, CdTe/CdS, copper indium gallium selenide (CIGS) and organics (**Figure 1**). The existence of these trap-states results in scattering and trapping of the charge carrier thereby reducing the charge transport through the Shockley-Read-Hall (SRH) recombination (or so called the “trap-assisted recombination”). Even in the state-of-the-art perovskite photovoltaic devices, the SRH recombination contributes towards the major energy loss.<sup>6</sup> Another problem of heat generation caused by hot-carrier thermalization and energy dissipation from SRH recombination is often neglected in literature. This becomes significant issue in real

application. For example, certain *HP* materials (*e.g.*, methylammonium lead perovskites) exhibit high thermal expansion coefficient ( $\alpha_v = 1.57 \times 10^{-4} \text{ K}^{-1}$ ).<sup>11</sup> Thus, the temperature-induced phase transition during day-night cycle could deteriorate the device performance.<sup>12,13</sup> Heat generated from SRH recombination can be reduced through the use of monocrystalline hybrid perovskites (*mono-HPs*) which consist of much lower trap density. In transistor applications, heat generation has also become prominent issue that degrades the performance and lifetime. In electronics industry, where the heat generated from hundreds of millions of transistors integrated on a single chip could cause reduced power density and degrade the computing power. Thermal cooling has become one of the important factors in maintaining Moore's Law.<sup>14,15</sup> Therefore, qualification of potential applications in transistor or even in chips, monocrystalline material is of great importance compared to their polycrystalline counterparts. *Mono-HP* wafer/thin film with ultralow trap density and its free GB nature, coupled by its super opto-electronic properties such as direct bandgap, excellent charge transport properties, easy material engineering including large doping space and various compositional modifications, and convenient solution processability, *etc.*, makes it a great platform for constructing next-generation ultra-high-performance devices.



**Figure 1** Comparison of trap-density between typical semiconductors, including amorphous silicon (*a-Si*),<sup>16</sup> polycrystalline silicon (*poly-Si*),<sup>17</sup> monocrystalline silicon (*mono-Si*),<sup>18</sup> CdTe/CdS,<sup>19</sup> copper indium gallium selenide (CIGS),<sup>20</sup> mono-rubrene,<sup>21</sup> pentacene,<sup>22</sup> poly-HP,<sup>9</sup> mono-HP,<sup>23</sup> with their microscopic images. Credits are given to various sources.<sup>6,24–30</sup> Copyright © 2018 Elsevier Inc. Copyright © 2002 Elsevier Inc. Copyright © 2018 Elsevier Ltd. John Wiley & Sons, 2017, © Copyright 2019 IEEE, ©2007 American Physical Society, © 2002 American Institute of Physics. Copyright © 1999-2019 John Wiley & Sons, Inc. © The Royal Society of Chemistry 2019. Copyright © 2018, Springer Nature. © 2019 Zentrum für Sonnenenergie- und Wasserstoff-Forschung Baden-Württemberg. Copyright © 2017 American Chemical Society. TRANS TECH PUBLICATIONS, LTD. Copyright © 2018, Springer Nature.

## 2. Fundamental merits of *mono-HP*

### 2.1 *HP* vs. typical organic and/or inorganic semiconductors

The ‘*perovskite*’ structure is named in honor of a Russian mineralogist Lev Perovski who reported calcium titanium oxide ( $\text{CaTiO}_3$ ,  $\text{XII A}^{2+\text{VI}}\text{B}^{4+}\text{X}^{2-}_3$ ) mineral and its unique crystal structure. In the early 1890s, Wells introduced the halide perovskite family of lead and tin-based alkali-metal halides synthesized by Campbell, Walden and Wheeler.<sup>31</sup> Later in 1978, Weber synthesized the organic-inorganic hybrid perovskite,  $\text{CH}_3\text{NH}_3\text{PbI}_3$  ( $\text{MAPbI}_3$ ), by substitutional doping of the alkali-metal by an organic cation, methylammonium ( $\text{CH}_3\text{NH}_3^+$ ), at the crystallographic A-site of the perovskite.<sup>32</sup> In these earlier years, the research focus was on transistor and light emitting applications but there was limitation in material synthesis and characterization.<sup>33,34</sup> In 2009, Miyasaka’s team implemented the *HP* into the dye-sensitized solar cell<sup>35</sup> (DSSC, or ‘*Grätzel cell*’). After that within a decade, the *HP* based solar cells have exhibited a phenomenal rise in device efficiency from 3% to over 24%.<sup>36</sup> The efficiency of *HP* based solar cells is higher than that reported for organic photovoltaics (OPV) (16.6%) and inorganics comprising of CdTe (22.1%) and CIGS (22.9%).<sup>36</sup> This high efficiency can be ascribed to the superior opto-electronic properties of *HP*. The direct band structure provides a high light extinction coefficient ( $\eta = 10^5 \text{ cm}^{-1}$  vs.  $10^3 \text{ cm}^{-1}$  of silicon) and small effective mass of electron and hole (originating from the strong *s-p* anti-bonding in the crystal corresponding to a  $m_h^* = 0.07$  vs. 0.29 of silicon). This enables super electrical and bipolar transport (high mobility,  $\mu$ , up to  $10^2 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  vs.  $10^{-4} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  of organics). Further, *HP* exhibit high flexibility in material engineering that allows tuning the bandgap (by substitutional doping) to be near the ideal bandgap of 1.34

eV in accordance with the Shockley-Queisser theory. Detailed discussions on the materials' physics can be found elsewhere.<sup>37</sup> *HP* is a highly crystalline material which enables the engineering of GBs, trap density, crystal orientation, phase purity, crystal grain size, *etc.* in order to tune the combination of electronic parameters.

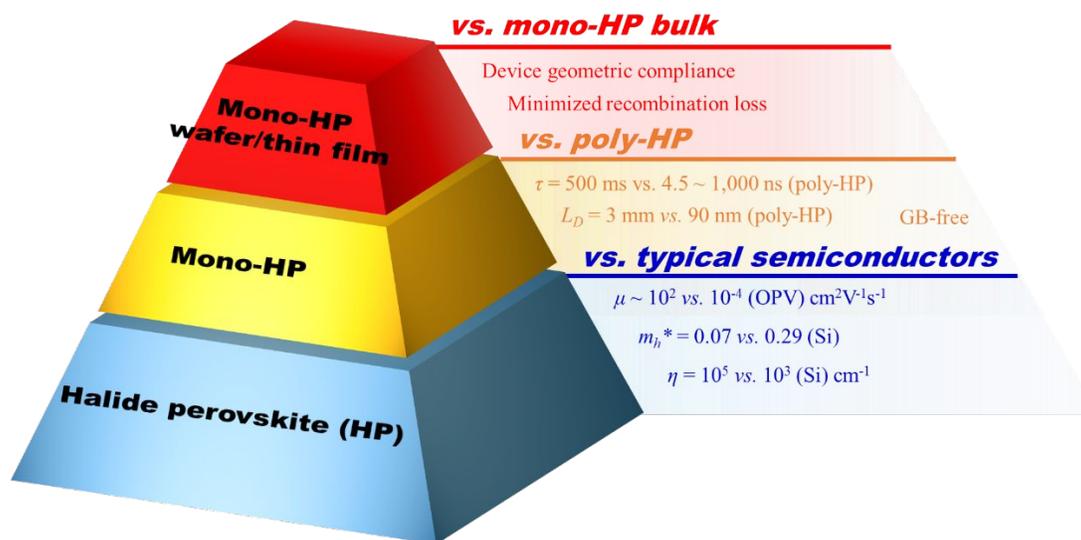
## 2.2 *Mono-HP vs. poly-HP*

The record solar cell efficiency (25.2%, KRICT/MIT) of *HP* PVs is based on *poly-HP* thin films. It is widely agreed that monocrystalline semiconductors have advantage over the polycrystalline semiconductors due to lower disordered energetic states. Taking *mono-HP* as an example, due to the elimination of GBs there is minimized trap density down to  $n_{trap} = 10^9 \text{ cm}^{-3}$  (*vs.*  $10^{17} \text{ cm}^{-3}$  in *poly-HP*, as shown in **Figure 1**),<sup>9,23</sup> high carrier mobility of  $\mu = 200 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  (*vs.*  $0.4 \sim 40 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  in *poly-HP*),<sup>38,39</sup> longer carrier lifetime of  $\tau = 500 \text{ ms}$  (*vs.*  $4.5 \sim 1,000 \text{ ns}$  in *poly-HP*),<sup>40</sup> larger carrier diffusion length of  $L_D = 3 \text{ mm}$  (*vs.*  $90 \text{ nm}$  in *poly-HP*)<sup>7,8</sup>. These features mitigate parasitic issues in the solar cell devices, such as photocurrent hysteresis, ion migration, as well as degradation present in typical polycrystalline devices. Overall, these features have raised the question that would a *mono-HP* PV exhibit better device performance than that of its polycrystalline counterparts? A positive answer in *mono-Si* PV gives us the hint of optimism, as the *mono-Si* PV displays the record 26.7% PCE in contrast to 22.3% of *poly-Si* PVs.<sup>6</sup> Taking the learnings from *mono-Si* PVs and building upon the achievements of *poly-HP*, we expect that *mono-HP* PV will create opportunities to further enhance efficiency. Recent discoveries on ferroelectric electron/hole channels,<sup>41,42</sup> highly conductive layer-edge states,<sup>43</sup> slower hot-carrier cooling,<sup>44</sup> and photon recycling process<sup>45</sup> have inspired the proof-of-concept *mono-HP* devices for improving the PCEs. To exemplify, the slow hot-carrier cooling in *mono-HPs* has been predicted to result in a potential PCE of 66%,<sup>44</sup> which is far higher than the Shockley-Queisser limit of 33.7% for typical single-junction PV devices.

## 2.3 *Mono-HPM membrane (mono-HP wafer/thin film) vs. mono-HP bulk*

During the past few years, *mono-HP* bulk materials with millimeter to several inch dimension have been grown and applied in optoelectronic applications including PVs,<sup>46</sup>

detectors,<sup>47</sup> and light emitters.<sup>48</sup> However, typical bulk single-crystal has a larger geometric dimension than its maximum charge diffusion length. For example, for sample handling and real implementation, a bulk *mono-HP* needs to have a dimension on the order of centimeters, which is significantly larger than its maximum carrier diffusion length (e.g., 175  $\mu\text{m}$  for  $\text{MAPbI}_3$ <sup>49</sup>). In most cases, the depletion width also needs to be taken into consideration to secure a high charge collection efficiency.<sup>50</sup> Hence, in case of bulk *mono-HP* based PV, photogenerated charge carriers traveling beyond the maximum diffusion length and/or the depletion width typically contribute to energy loss by a recombination process. To minimize these recombination losses, shrinking the thickness of *mono-HP* to comply with the diffusion and/or the depletion limit is of great relevance. Consequently, the *mono-HP* wafer/thin film with suitable thickness provides the solution for efficiency losses. As shown in **Figure 2**, the *mono-HP* wafer/thin film is expected to deliver a better performance in photovoltaics and transistors.



**Figure 2** A 'Mesoamerican pyramid' showing the relationship between *mono-HP* wafer/thin film, *mono-HP*, and *HP*, as well as their comparison with *mono-HP* bulk, *poly-HP* and other typical semiconductors, respectively.

### 3. Techniques for growing *mono-HP* wafer/thin film

Although the advantages of *mono-HP* wafer/thin film have been recognized, the realization of product-oriented *mono-HP* wafer/thin film that meets device requirements remains to

be achieved. These requirements include large aspect ratio (*i.e.*, large basal area but small thickness), smooth surface, low-surface trap density, controllable crystal facet orientation, and good compatibility with target substrate. In terms of device construction, both wafer and thin film could be utilized, as solar cells and transistors can be either built from free-standing *mono-HP* wafer by coating functional layers on both sides analogous to the manufacturing of *mono-Si* PVs, or from the *mono-HP* thin film that has been grown on FTO and/or ITO electrodes followed by metal electrode deposition. Several methods have been proposed in literature to provide *mono-HP* wafer/thin film. These include: (i) *floating method*, (ii) *space-limited growth method*, (iii) *vapor phase epitaxy (VPE)* and (iv) *bulk-crystal dicing*. In this section, we will discuss these techniques for growing *mono-HP* wafer/thin film emphasizing crystallization mechanisms and growth processes.

### 3.1 Floating method

The driving force for the precipitation of a solid phase from a *supersaturated* solution is quantified as the chemical potential difference ( $\Delta\mu$ ) of a molecule between solution and bulk crystal phase:

$$\Delta\mu = \mu_s - \mu_c \quad (3.1)$$

where  $\mu_s$  and  $\mu_c$  are the chemical potential of a molecule in solution and in the bulk crystal, respectively. **Equation 3.1** can also be thermodynamically expressed as:

$$\Delta\mu = kT \ln S \quad (3.2)$$

where  $k$ ,  $T$ ,  $S$  are the Boltzmann constant, absolute temperature, and the supersaturation ratio, respectively. Initiation of *supersaturation* can be achieved through temperature adjustment (cooling), concentration changes (concentrating), or by altering solution activity coefficients as in the solvent/antisolvent method (denoted by purple dash arrow in **Figure 3a**) according to the temperature-composition-phase behavior in **Figure 3a**. As it can be seen from **Figure 3a**, the solubility curve represents thermodynamic equilibrium between the phases. For most perovskite systems with composition and temperature below the solubility curve, a stable '*unsaturated zone*' (blue region in **Figure 3a**) exists. Typical systems have a positive correlation between solubility and temperature, hence, reducing the temperature of a saturated solution can trigger the crystallization. However, some *HP*

solutions have an ‘inverse’ dependence of solubility on temperature. For example, the solubility of MAPbI<sub>3</sub> in GBL solution increases with the temperature.<sup>51</sup> This requires a higher temperature to induce the *supersaturation*. In any case, beyond this solubility limit the liquid might not be in the thermodynamic equilibrium with respect to the formation of its solid phase, which is termed as the ‘*metastable zone*’ (green region in **Figure 3a**). In this region, spontaneous nucleation is difficult to occur, but crystal-growth is easy, implying the perfect region for growing a larger crystal from a small one. Typically, in order to initiate the formation of a solid phase, heterogeneous nucleation sites are introduced. Beyond the boundary of ‘*metastable zone*’, these nucleation seeds are no longer required, and the region becomes the ‘*supersaturated zone*’ (red region in **Figure 3a**), which is neither stable nor in equilibrium, and is thus subject to a spontaneous nucleation and rapid crystal growth.

Initiating nucleation requires the work for overcoming the free energy barrier ( $\Delta G_T$ ), which is set by the free energy difference between the system in its final and initial states ( $\Delta\mu$ ) plus a surface tension related term ( $4\pi \cdot r^2\sigma$ ):<sup>52</sup>

$$\Delta G_T = -\frac{4}{3}\pi \cdot \frac{r^3}{V}\Delta\mu + 4\pi \cdot r^2\sigma \quad (3.3)$$

where  $r$ ,  $\sigma$ , and  $V$  are the radius of the nucleus, surface free energy and volume of each molecule. **Figure 3b** shows the  $\Delta G_T$  as a function of  $r$ . It can be seen from this relation how the function reaches a maximum, representing the energy barrier ( $\Delta G^*$ ), that should be overcome to initiate the nucleation. The magnitude of  $\Delta G_T$  depends heavily on the surface free energy ( $\sigma$ ), so any process that could change this value would have a significant effect on the nucleation. A classic example is the introduction of foreign seeds, which has been utilized in the ‘*Czochralski method*’.<sup>53</sup> In the case of halide perovskite, the nucleation can first occur at the ‘*solution/substrate*’ interface as the presence of the foreign substrate can decrease the surface energy  $\sigma$ , reducing the  $\Delta G_T$  by a factor of  $f(\theta)$  according to the equation:<sup>52</sup>

$$\Delta G_{\text{solution/substrate}} = \Delta G_{\text{hetero}} = \Delta G_{\text{homo}} \cdot f(\theta) \quad (3.4)$$

$$f(\theta) = \frac{2 - 3\cos\theta + \cos^3\theta}{4} \in [0, 1] \quad (3.5)$$

where  $\theta$  is contact angle of the solution on the alien substrate surface. A wetting substrate has higher probability of inducing the nucleation as it has a smaller contact angle and the resultant smaller  $f(\theta)$  is close to  $\theta$ , which renders a lower energy barrier ( $\Delta G^*$ ). The ‘*solution/air*’ interface is often neglected, where the existence of the surface tension can reduce the energy barrier. In our recent study,<sup>54</sup> we have developed a simplified model to illustrate the surface energy contribution to facilitate the nucleation at the water-air interface. The analysis considered one type of precursor molecules ( $A$ ), which can exist in form of (i) free precursor molecules “ $A$ ”, (ii) “ $A$ -cluster” nucleus, and (iii) solvated complex “ $A$ - $jS$ ” where one  $A$  is intermolecularly bonded with  $j$  solvent molecules ( $S$ ) having a complex binding energy  $E_C$ . We derived the free energy difference expressions for nucleation in either bulk solution or at the ‘*solution/air*’ interface. In contrast to the bulk solution, the molecules at the ‘*solution/air*’ interface experience extra tensile elastic stress (surface energy contribution) that increases the energy of precursor molecules by  $\chi$  ( $> 0$ ) and results in a reduced energy barrier by contributing  $\chi$  to the denominator, as can be seen from the equation:

$$\Delta G_{\text{solution/air}} = \frac{16}{3} \pi \sigma^3 \left( \xi - E_C - \xi_A + \chi + k_B T \ln \frac{1}{\frac{M_S^j}{M_A} - j^2 \cdot M_S^{j-1}} \right)^{-2} \quad (3.6)$$

where  $\xi$  ( $> 0$ ) is the cohesive energy of precursor molecules in the cluster,  $\xi_A$  ( $> 0$ ) is the energy of precursor molecules,  $\sigma$  is the surface tension coefficient,  $k_B$  is the Boltzmann constant,  $T$  is temperature, and  $M_S$  and  $M_A$  are the total molar concentrations of solvent and precursor molecules, respectively. **Figure 3b** compares the free energy differences with and without tensile elastic stress. Clearly, at the ‘*solution/air*’ interface, there is a contribution from surface energy/tensile elastic stress towards reducing the energy barrier ( $\Delta G^*$ ), which enhances the probability of nucleation (blue line in **Figure 3b**).

In terms of crystal growth, particularly for growing a large single-crystal, the crystal growth needs to be controlled in the ‘*metastable zone*’ (**Figure 3a**) to eliminate other nuclei seeds and hence only one nucleus grows into a larger single-crystal. In the solution, the crystal can grow in any direction to achieve larger dimensions. In order to confine the resultant crystal into a wafer/thin film geometry, a strategy relying on the surface energy

has been developed.<sup>54,55</sup> Fundamentally, the crystal growth rate ( $\Psi$ ) can be determined by the rate of competition between molecular attachment and detachment:<sup>54</sup>

$$\Psi = \Gamma \nu \frac{\Delta G_C}{k_B T} \exp \frac{-\Delta G'}{k_B T} \quad (3.7)$$

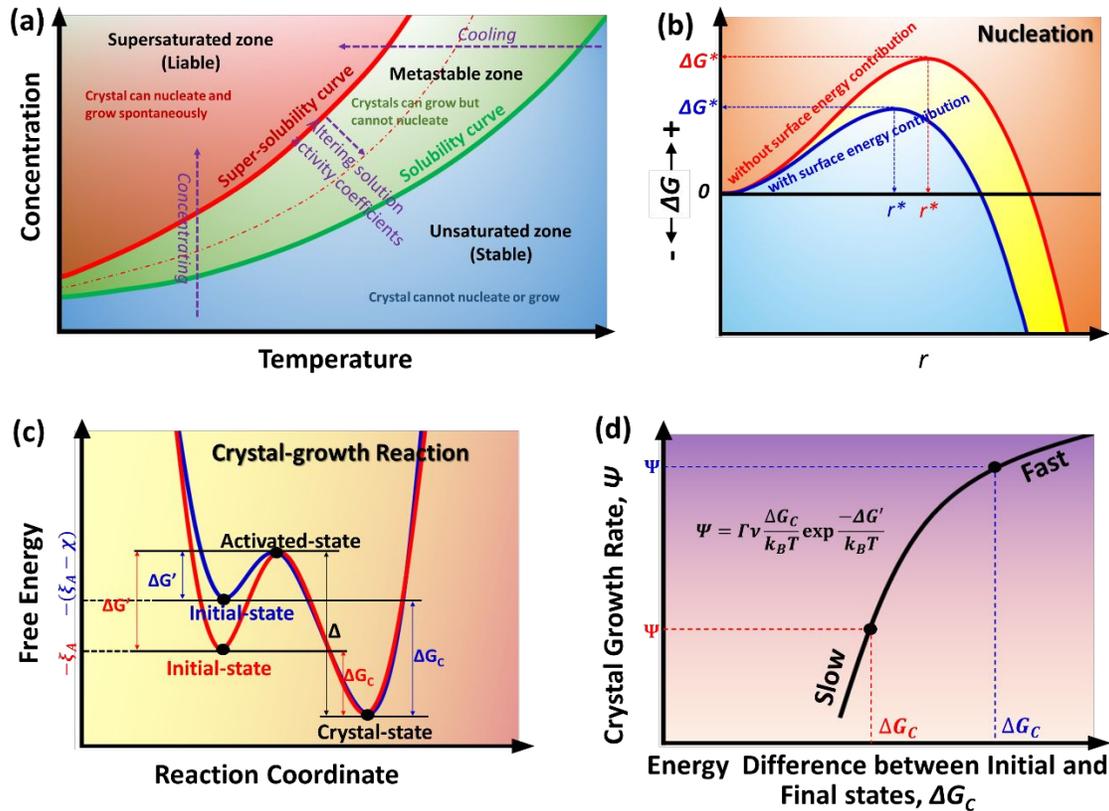
$$\Delta G' + \Delta G_C = \Delta \quad (3.8)$$

$$\Delta G' = G_a - G_i \quad (3.8a)$$

$$\Delta G_C = G_f - G_i \quad (3.8b)$$

$$\Delta = G_f - G_a \quad (3.8c)$$

where  $\Gamma$  is a geometric factor,  $\nu$  is an attempt frequency,  $\Delta G'$ ,  $\Delta G_C$  and  $\Delta$  are the free energy difference between initial ( $G_i$ ) and activated ( $G_a$ ), between initial ( $G_i$ ) and final ( $G_f$ ), and between activated ( $G_a$ ) and final states ( $G_f$ ), respectively, as can be seen in **Figure 3c**. Compared to the inner solution, at the '*solution/air*' interface, the additional surface tensile stress contributes to a higher energy in the initial state (blue line in **Figure 3c**). Therefore, according to the **Equation (3.7)**, larger crystal growth rate ( $\Psi$ ) is acquired. **Figure 3d** depicts the relationship between crystal growth rate ( $\Psi$ ) and the free energy difference between initial and final states ( $\Delta G_C$ ). A larger  $\Delta G_C$  renders a higher  $\Psi$ . As a result, a faster lateral growth along the *solution/air* interface against the vertical growth is expected in the inner solution.

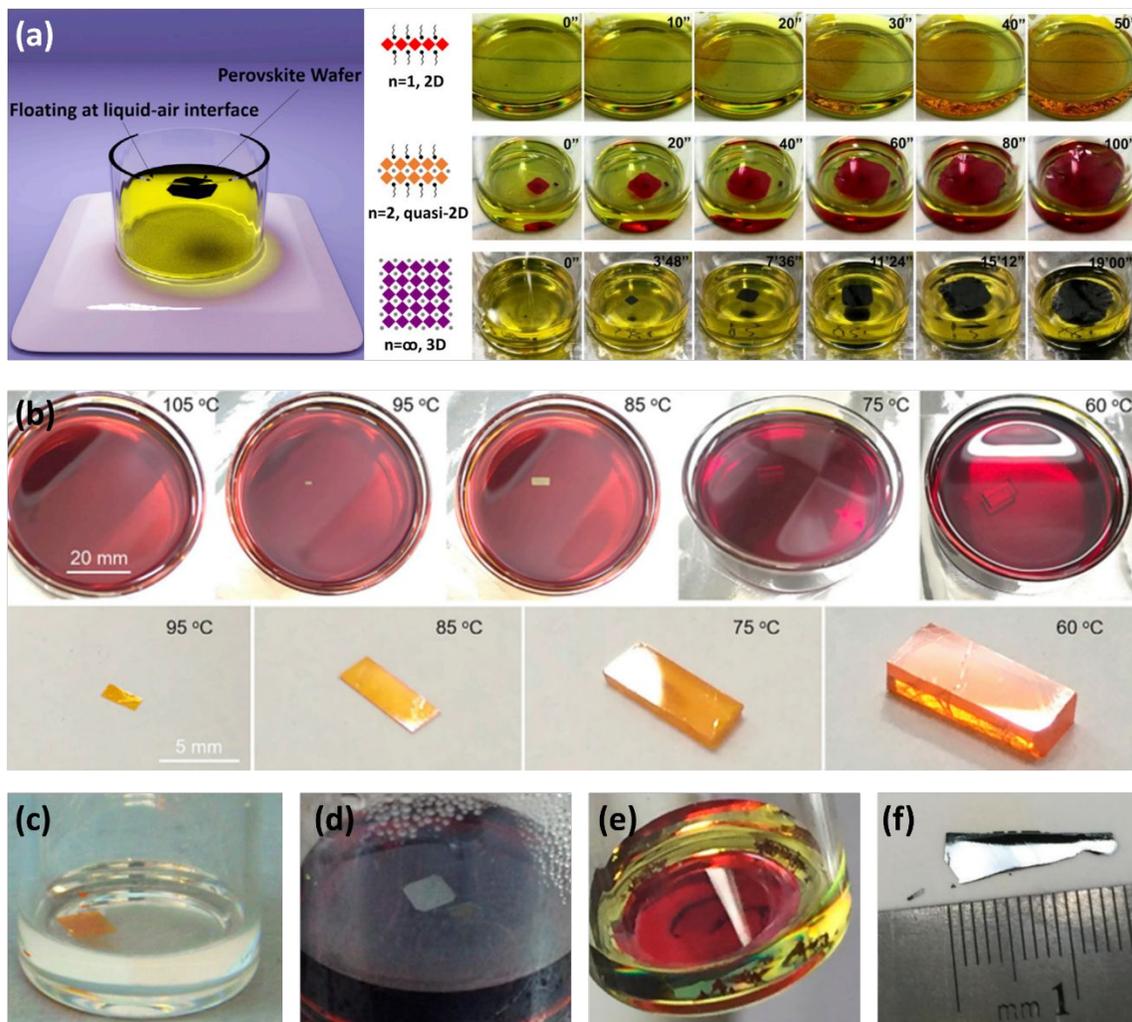


**Figure 3 Crystallization theory.** (a) Solubility Curve and Metastable Zone plotted against temperature and concentration. (b) Total free energy versus cluster size, (c) reaction coordinate diagram, and (d) crystal growth rate versus energy difference between initial and crystal states, showing that the surface tensile stress contributes to both lower nucleation barrier and faster crystal growth rate.

Relying on this mechanism, *mono-HP* wafer/thin film can be achieved from the *Floating method*. Several groups have demonstrated the free-standing *mono-HP* wafer from the *solution/air* interface. **Figure 4a** exemplifies the *mono-HP* wafer growth of two-dimensional (2D), quasi-2D, and three-dimensional (3D) perovskites of  $\text{BA}_2\text{MA}_{n-1}\text{Pb}_n\text{I}_{3n+1}$ , with  $n$  being 1 (2D), 2, 3, ... (quasi-2D),  $\infty$  (3D).<sup>54</sup> Here BA is  $n$ -butylammonium ( $\text{CH}_3(\text{CH}_2)_3\text{NH}_3^+$ ) and MA is methylammonium ( $\text{CH}_3\text{NH}_3^+$ ). It should be noted that the  $\text{BA}^+$  cation is amphiphilic long molecule consisting of a hydrophilic ammonium cation head and a hydrophobic alkyl chain. Such an amphiphilic molecule can align itself with a head-down pattern at the water-air interface. The ammonium cation head can further template the molecular assembly underneath to direct the facet orientation during the crystal growth. By controlling the chemical composition, *i.e.*, the ratio between BA and

MA in the solution, the final crystal can be tuned from 2D multi-quantum-well (MQW) structure to 3D perovskite.<sup>54</sup> Similarly, for other 2D perovskite system such as the  $(\text{PEA})_2\text{PbI}_4$  (PEA is phenylethylammonium, *i.e.*,  $\text{C}_6\text{H}_5(\text{CH}_2)_2\text{NH}_3^+$ ), free-standing single-crystals can be obtained from *floating method*. As can be seen in **Figure 4b**, Liu *et al.* reported the single crystal synthesis floating at the solution surface.<sup>56</sup> By tuning the temperature, the aspect ratio can be controlled as well. Other 3D perovskite materials such as  $\text{MAPbBr}_3$ ,  $\text{MAPbI}_3$ , and  $\text{MASnBr}_3$  can also be achieved using similar method. **Figures 4c-f** displayed the corresponding 3D *mono-HP* wafer/thin films from different groups.<sup>55,57</sup>

Notably, the advantages of the *floating method* include the ability to control the crystal facet, as spontaneous alignment of an amphiphilic nano-template can direct the assembly in a predictive pattern. Understanding the operating mechanism of a surfactant monolayer that adapts the perovskite precursive ions at the *solution/air* interface and guides the epitaxial growth of nanosheets can bring more insights to this field. Similar attempts have been successfully applied in growing the ZnO nanosheets, which is termed as the adaptive ionic layer epitaxy (AILE) method.<sup>58</sup> In addition, scaling up the *mono-HP* wafer by enlarging the area of the solution surface may boost the development of the *mono-HP* based applications. Coincidentally, an analogical methodology called “Float Glass Process” for manufacturing the flat glasses in industry has been well developed and widely applied. Actively utilizing these learnings from related glass fields may further accelerate the development of *mono-HP* wafer/thin film-based optoelectronics.



**Figure 4** Various mono-HP wafer/thin films synthesized using the Floating method. (a)  $BA_2MA_{n-1}Pb_nI_{3n+1}$ , with  $n$  being 1, 2, 3, ...,  $\infty$ , adapted from reference<sup>6,54</sup>. Copyright © 2018 Elsevier Inc. Copyright © 2018 American Chemical Society. (b)  $(PEA)_2PbI_4$ , adapted from reference.<sup>56</sup> Copyright © 2019 Copyright Clearance Center, Inc. (c)  $MAPbBr_3$ , (d)  $MAPbI_3$ , and (e)  $MASnBr_3$ , adapted from reference.<sup>55</sup> Copyright © 2017 American Chemical Society (f) Photograph of 1.5 cm length  $MAPbI_3$  single crystal piece of wafer, adapted from reference.<sup>57</sup> Copyright © 1999-2019 John Wiley & Sons, Inc.

### 3.2 Space-limited growth method

In order to obtain the single-crystal with a flat and large aspect ratio, the *floating method* takes advantage of the ‘energy confinement’ where surface energy contribution confines the crystal growth along the *solution/air* interface. A more straightforward way is to use the ‘space confinement’, or the ‘space-limited growth method’. In this case, the crystal growth occurs in a geometrically designed ‘container’ that has a flat chamber (Figures

**5a).** The technologies for typical bulk crystallization such as *solution temperature-lowering*<sup>59</sup>, *inverse temperature crystallization*<sup>51,60</sup>, *anti-solvent vapor-assisted crystallization*<sup>61</sup> and *melt crystallization*<sup>62,63</sup>, can be easily adopted in the *space-limited growth method*. The flexibility in designing the 'container' and accommodating it into a narrow crevice helps in achieving a flat and large aspect ratio *mono-HP* wafer/thin film. For example, by shrinking the gap between two substrates, the thickness of the membrane can be tuned from 13 nm to 4.5 mm.<sup>64</sup> Chen *et al.* employed two clean flat substrates clipped together which were then vertically dipped in a perovskite saturated solution.<sup>64</sup> The capillary pressure drives the solution to fill the gap between the substrates. The gap can be modulated by the clipping force. Upon heating the bottom precursor solution to reach a saturated state, the top solution can be tuned into a supersaturated state through top-seeded solution-growth (TSSG) method.<sup>49</sup> Hence, the crystal can be grown from the slit (**Figure 5b**). Liu *et al.* also demonstrated the early MAPbI<sub>3</sub> single crystal wafer of 150 μm thickness by building an ultrathin geometry-defined dynamic-flow reaction system.<sup>65</sup> Rao *et al.*<sup>66</sup> demonstrated the *mono-HP* thin film of CH<sub>3</sub>NH<sub>3</sub>PbBr<sub>3</sub> on FTO Glass with a large area of 120 cm<sup>2</sup> and a controllable thickness of 100-800 nm. To reduce the thickness, an optimized module with a smaller laminar distance of 16 μm and a mass-transport circulating flow to supply the precursors has been developed. This renders a *mono-HP* thin film with larger aspect ratio.<sup>67</sup> As the nucleation process takes place in the narrow channel, the adhesion of precursor molecules on the substrate surface can lead to unbalanced local concentrations, inducing multiple nuclei and transforming into a polycrystalline film.<sup>68</sup> Chen *et al.* introduced hydrophobic coaters (*e.g.*, PTAA) on the substrate to facilitate the microflow and obtained millimeter-sized *mono-HP* thin film of MAPbI<sub>3</sub> and MAPbBr<sub>3</sub> with thicknesses ranging from smaller to tens of micrometers.<sup>68</sup>

As mentioned above, the surface energy can have huge effect on the nucleation barrier. Yang *et al.*<sup>69</sup> employed substrates with prior surface treatment to modulate the energy barrier. Briefly, hydrophobically treated silicon and hydrophilically treated ITO glass are used as two substrates for crystal growth. The nucleation energy barrier was reduced on the ITO glass for supporting the selective growth of MAPbBr<sub>3</sub> *mono-HP* thin film. A thickness of 365 nm and a lateral size of > 600 nm has been obtained this way.

Normally, the solubility increases with the temperature. In certain perovskite solution system, such as MAPbI<sub>3</sub> in GBL, the solubility reaches maximum at 60 °C and further increasing the temperature will significantly decrease the solubility.<sup>70</sup> Relying on this phenomenon, *inverse temperature crystallization*<sup>51,60</sup> has been applied in growing bulk crystals. Introducing the *inverse temperature crystallization*<sup>51,60</sup> into the *space-limited growth method* can simplify the experimental procedure, as nucleation can be triggered by just elevating the solution temperature. Yu et al.<sup>71</sup> showed (**Figure 5d**) that the *space-limited growth method* coupled with the inverse temperature crystallization results in successful synthesis of *mono-HP* thin film of MAPbX<sub>3</sub>, X = Cl, Br, and I with tunable lateral size ranging from micrometers to millimeters. Yue et al.<sup>72</sup> also applied the similar strategy in growing MAPbI<sub>3</sub>. They demonstrated that unlike MAPbBr<sub>3</sub>, the MAPbI<sub>3</sub> is more difficult to be synthesized through the *space-limited growth method* due to the distinct solubilities of MAI and PbI<sub>2</sub> in GBL. A MAPbI<sub>3</sub> seed crystal is then employed to bypass the nucleation barrier and obtain a *mono-HP* thin film of MAPbI<sub>3</sub> with thicknesses of 50 μm and lateral dimensions of up to 2 mm.<sup>72</sup>

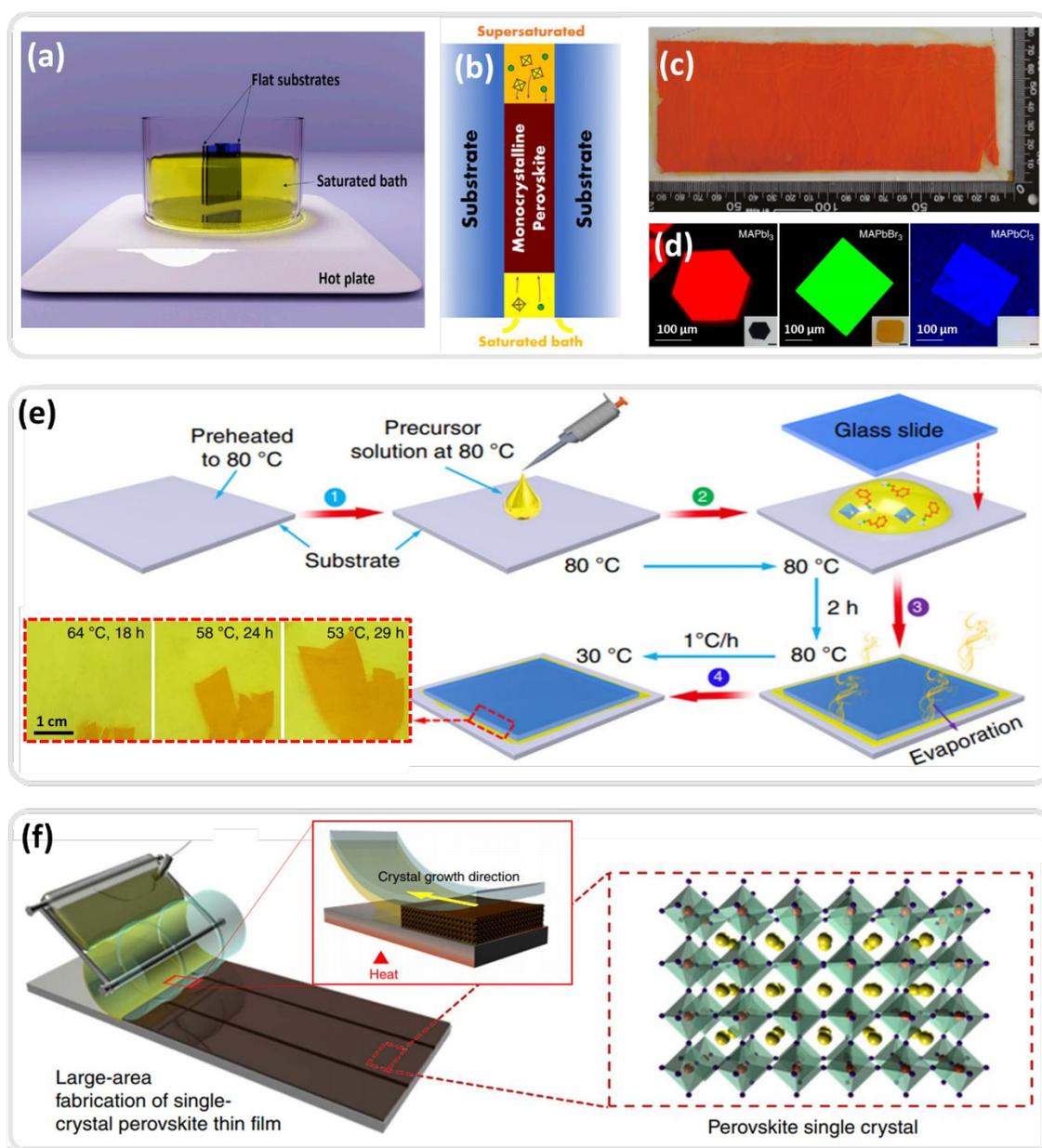
Instead of immersing the two-substrate chamber into the saturated solution in **Figure 5a**, derivatives of *space-limited growth method* can take advantage of the evaporation of solvent molecules to concentrate the solution thus reaching the *supersaturation zone* in **Figure 3a**. Therefore, the method of ‘*cast-capping*’ has been attempted that caps the wet saturated solution by a coverslip followed by evaporation of solvents to grow the *mono-HP* thin film.<sup>68,73,74</sup> Yanagi’s group has reported this method to grow millimeter size *mono-HP* thin film for laser and LED applications.<sup>73,75</sup> It should be noted that in order to optimize the crystallization, several experimental conditions such as the environmental atmosphere, solvent evaporation rate, temperature and saturated vapor pressure need to be tuned during the process. A successful example is the growth of the (PEA)<sub>2</sub>PbI<sub>4</sub> *mono-HP* thin film by Liu et al.<sup>76</sup> **Figure 5e** shows the illustration of the experimental procedure. Briefly, one drop of prepared precursor solution [PbI<sub>2</sub>: PEA (1: 2 molar ratio) was dissolved in GBL at 80 °C with a concentration of 2.12 M] is pipetted onto a glass substrate preheated to 80 °C. A second glass slide with smaller size is then placed onto the solution drop that pushes the solution to spread evenly in the channel. After

keeping the system at 80 °C in enclosed oven, the evaporation of solvent from the edge will concentrate the solution into the *oversaturated* zone and lead to the nucleation and crystal growth successively. With an optimal temperature ramp rate, the resultant (PEA)<sub>2</sub>PbI<sub>4</sub> *mono-HP* thin film exhibited a size of > 73 × 35 mm<sup>2</sup> and thickness of 0.6 μm, which was the first time synthesis of a large *mono-HP* thin film with area exceeding 2500 mm<sup>2</sup> but thickness lower than 10 μm.<sup>76</sup>

Another innovation building upon the *space-limited growth method* can be obtained in combination with a roll-to-roll printing technology. Lee *et al.*<sup>77</sup> demonstrated the wafer-scale patterned *mono-HP* thin film based on “geometrically confined lateral crystal growth (GC-LCG)” method. **Figure 5f** displays the schematic of the manufacturing setup. A spatially limited micro-chamber was constructed for crystal growth with a cylindrical metal roller wrapped with poly(dimethylsiloxane) (PDMS) mold. It had a periodic array of wide and shallow channels with 10 mm width, 200 nm depth and narrow 400 nm distance between the channels. In the beginning, roller mounted with an ink supplier, which is filled by the perovskite precursor ink, is placed in contact with the preheated substrate. At the open end of channel, the crystallization occurred instantly when the ink contacted the hot substrate due to the rapid solvent evaporation. With an optimal mold rolling speed, the seed crystals at the end can direct the crystal growth from the solution near the end. The crystal growth in the vertical direction is confined within the mold, and the lateral crystal growth is also regulated by the channel hence there is no misaligned growth. Patterned (10-mm-wide strips with 400-nm-wide spacing and 200-nm-thick) *mono-HP* thin film (3×3 inch) on SiO<sub>2</sub> substrate has been obtained using this process. The striking feature of this technology is the fast and large-scale production, as well as the ability to control the crystal growth direction.<sup>77</sup>

The “*space-limited method*” offers a straightforward way for growing *mono-HP* thin films using these strategies for bulk crystals. Nevertheless, several open questions need to be addressed before moving on to the next stage: (i) the first difficulty lies in the proper construction of an optimal container of large aspect ratio on inch-scale in basal plane but nanometer-scale in height with satisfactory inner surface homogeneity, as the surface morphology of the single crystal membrane grown inside the container is largely dependent

on the nanostructures of the container surface; (ii) the post-process of exfoliating the crystal from the container remains as another challenge, since the physical release inevitably will induce structural damages during the mechanical cleavage between perovskite and container wall; (iii) careful facet-control-growth needs to be reconsidered as the charge behavior may anisotropically depend along the reciprocal lattice orientation, particularly in lower dimensional perovskite, whereas the “*space-limited method*” cannot govern the facet orientation due to the random nucleation inside the narrow space.



**Figure 5 Examples of space-limited growth method. (a)** Basic experimental setup for the space-limited growth method. **(b)** Schematic illustration of a spatially confined crystal grown in a narrow crevice constructed by two flat substrates. Adapted from reference<sup>6</sup>. Copyright © 2018 Elsevier Inc. **(c)** Photograph of a MAPbBr<sub>3</sub> crystal thin films grown from this method, exhibiting a 0.4 mm thickness and 120 cm<sup>2</sup> area. Adapted from reference<sup>78</sup>. Copyright © 1999-2019 John Wiley & Sons, Inc. **(d)** Fluorescence microscopy images of MAPbI<sub>3</sub>, MAPbBr<sub>3</sub>, and MAPbCl<sub>3</sub> single crystalline flakes grown from the space-limited growth method. Adapted from reference<sup>71</sup>. Copyright © 2018, Springer Nature. **(e)** A schematic illustration of a capping method, coupled with the photographs of the resultant single crystal flakes. Adapted from reference<sup>76</sup>. Copyright © 2018, Springer Nature. **(f)** Schematic of a geometrically confined lateral crystal growth (GC-LCG) method. Adapted from reference<sup>77</sup>. Copyright © 2017, Springer Nature.

### 3.3 Vapor phase epitaxy (VPE)

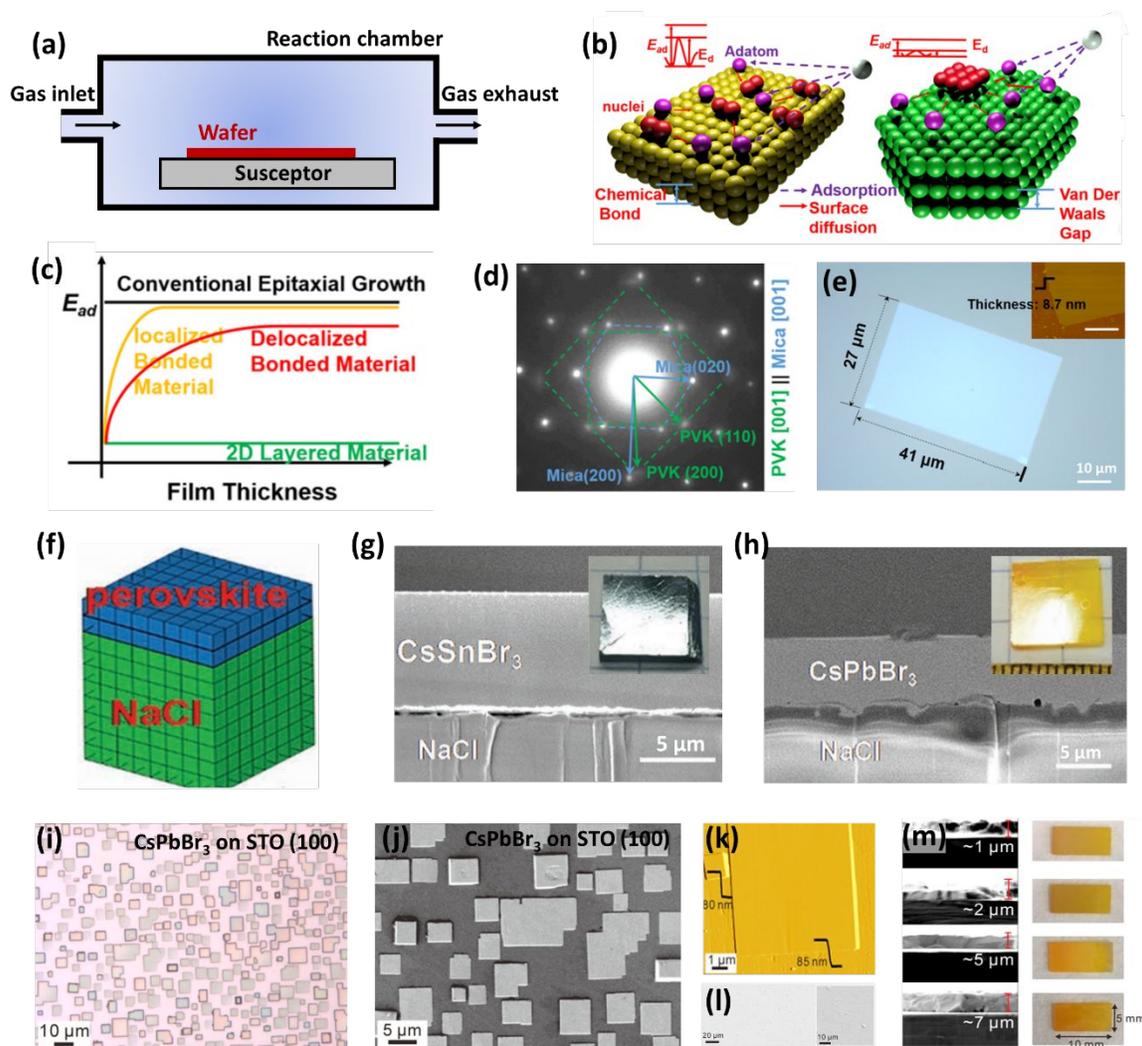
Vapor phase epitaxy (VPE) is a ubiquitously powerful technique for growing IIIA-VA semiconductors such as GaAs, GaP, InP, GaAsP, and InGaAsP *etc.* **Figure 6a** displays a simple setup of VPE, where the vapor-phase precursors are transported into the reaction chamber to trigger and grow the single-crystalline thin film directly on a susceptor. The VPE has been documented previously to be a successful technique in growing *p*-type GaN for blue LED.<sup>79</sup> This method can provide high phase purity and ultrathin single-crystal thin films that have a thicknesses at the monolayer level.<sup>80</sup> Nevertheless, the major challenges are the difficulties in finding a compatible substrate whose lattice constant and expansion coefficient could match well with that of objective materials. Meanwhile, to vaporize the precursor molecules, temperature control and material stability, particularly for organic ammonia that has a lower thermal stability, also need to be taken into consideration. So far, there has been a hinderance in applying this method to grow organic-inorganic *mono-HP* thin film.

It was not until recently, Shi's group developed the VPE assisted *mono-HP* thin film growth on van der Waals (VDW) substrate.<sup>80</sup> As shown in **Figure 6b**, they compared the atomistic nucleation between a conventional and a VDW epitaxy process. For the conventional case, the strong chemical bond between adatom and substrate leads to a very small critical nucleus (down to single atom) and a large diffusion barrier ( $E_d$ ). While for the VDW case, the inert substrate is free from dangling bonds and only small dipole moments are present. Thus, there is a small adsorption energy ( $E_{ad}$ ) in this case, which

leads to a more difficult nucleation process since more “simultaneous” collisions of adatoms on the substrate are needed. In addition, the higher energy VDW bonding state makes the diffusion barrier ( $E_d$ ) extremely low, according to several simulation works.<sup>81</sup> By quantifying the lifetime of adatoms ( $\tau_a$ ) during the nucleation process by

$$\tau_a = \nu^{-1} \exp\left(\frac{E_{ad}}{kT}\right) \quad (3.9)$$

where  $\nu$  is the vibration frequency and  $k$  the Boltzmann constant, and analyzing using the Walton’s model, the nucleation barrier ( $\Delta G^*$ ) can be calculated on either conventional or the VDW epitaxy process. For the *HP* with extremely low cohesive energy and strong ionic character, a significant percentage of large-scale monolayer growth with proper growth conditions is expected (**Figure 6c**). They obtained MAPbCl<sub>3</sub> *mono-HP* of large-scale ultrathin sheet with high crystalline phase purity (**Figures 6d & 6e**).<sup>80</sup> By adjusting the substrate and target material in terms of lattice constant, *mono-HP* thin films of CsSnBr<sub>3</sub> and CsPbBr<sub>3</sub> have been grown on the NaCl substrate. **Figures 6f-6h** show the heterostructure illustration and corresponding SEM images. The obtained *mono-HP* thin films exhibit smooth surfaces with uniform and adjustable thicknesses of ~ 200 nm to ~ 7  $\mu$ m.<sup>82</sup> Besides, the SrTiO<sub>3</sub> (STO) can also act as a good susceptor substrate, due to a low lattice mismatch factor with CsPbBr<sub>3</sub>.<sup>83</sup> By increasing the reaction temperature to 450 °C, atomic diffusion is accelerated to foster the nucleation and crystal growth. A large-area continuous *mono-HP* thin films of CsSnBr<sub>3</sub> with good single crystallinity and orientation (**Figures 6i & 6j**) can be readily grown on the (100) face of STO substrates, with adjustable thickness from 80 nm (**Figure 6k**) to 7  $\mu$ m (**Figure 6m**). Specifically, this method is particularly used for synthesizing all-inorganic perovskite materials, but for organic-inorganic perovskite such as MAPbI<sub>3</sub>, FAPbI<sub>3</sub>, the high reaction temperature over 400 °C will degrade the organic moieties significantly.



**Figure 6** Vapor phase epitaxy (VPE) method for growing mono-HP thin films. (a) A simply prototype VPE reactor. (b) Schematic drawing displaying different atomistic processes on a conventional (yellow) and VDW (green) substrate in terms of adsorption energy ( $E_{ad}$ ), diffusion barrier ( $E_d$ ), and nuclei sizes. (c) Schematic drawing of how  $E_{ad}$  changes with thickness for three types of materials. (d) Electron diffraction pattern of mono-HP on a mica substrate. (e) Optical image of an individual large-scale ultrathin mono-HP sheet (inset showing the atomic force microscopy measurement of the film thickness). Adapted from reference<sup>80</sup>. Copyright © 2015 American Chemical Society. (f) The heterostructure illustration of mono-HP grown on NaCl substrate. SEM images of (g) CsSnBr<sub>3</sub> and (h) CsPbBr<sub>3</sub> mono-HP on NaCl substrate, coupled with the photograph of a real sample. Adapted from reference<sup>82</sup>. Copyright © 1999-2019 John Wiley & Sons, Inc. (i) Optical microscopy and (j) SEM image of the CsPbBr<sub>3</sub> nanoplates grown on STO (100) substrate. (k) Representative AFM images and (l) Top down SEM image of the CsPbBr<sub>3</sub> mono-HP film with 7 μm thickness. (m) Cross-sectional SEM images and photographs of the CsPbBr<sub>3</sub> mono-HP film with varying thickness of 1, 2, 5, and 7 μm. Adapted from reference<sup>83</sup>. Copyright © 2017 American Chemical Society.

### 3.4 Bulk-crystal Slicing

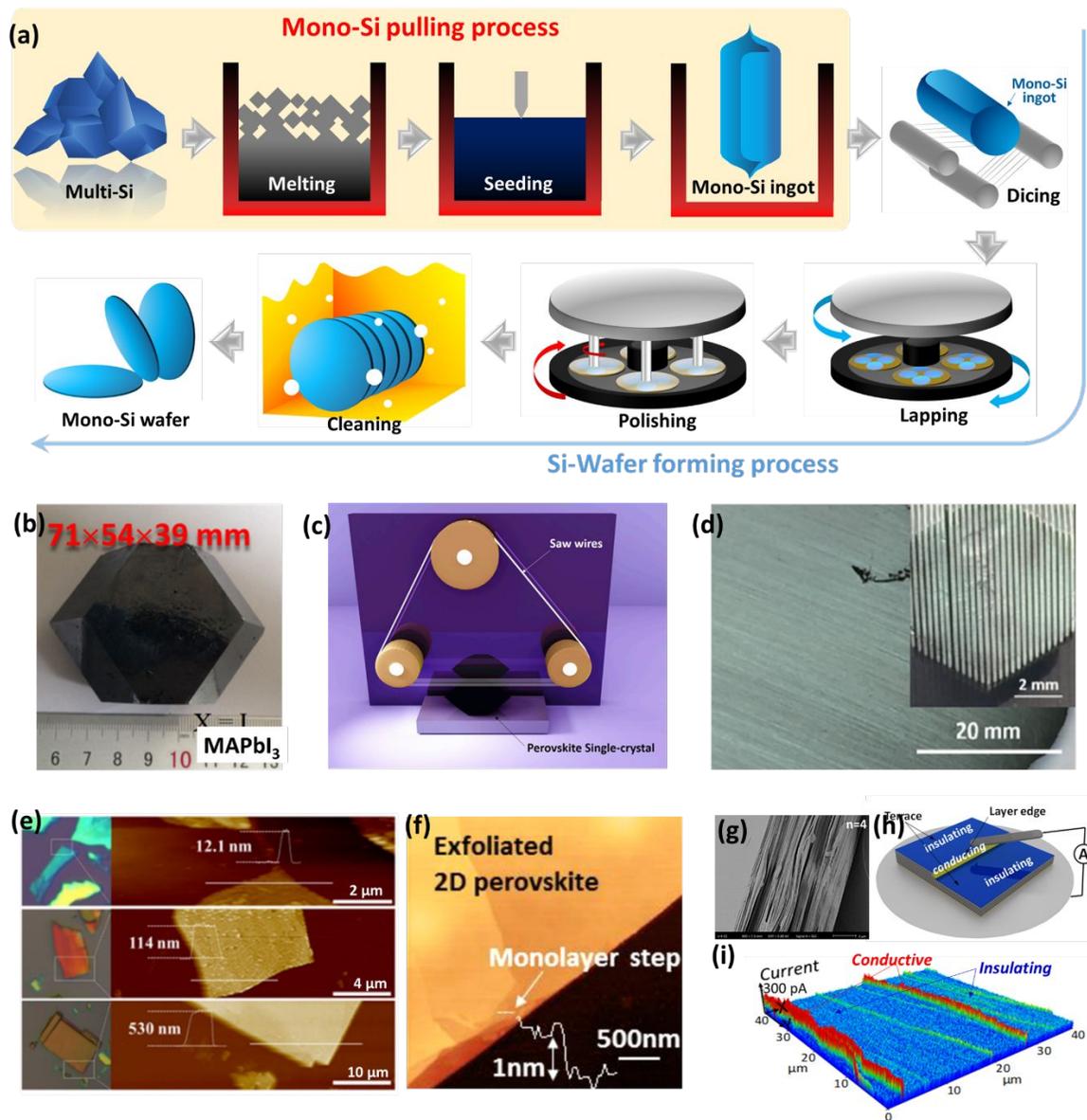
Above we have shown the current technologies for growing *mono-HP* wafer/thin film, starting from solution. The geometric feature of flat, large basal size but small thickness is confined either by energetics barriers (surface energy in floating method, adhesion and diffusion energy in VPE method) or spatial objects (narrow channel in space limited method). On the other hand, industrial *mono-Si* wafer manufacturing either for solar panel application or chip industry are exclusively based on a *bulk-crystal slicing* technology, following a top-down procedure. **Figure 7a** displays the simplified manufacturing flow chart consisting of a *mono-Si* ingot pulling process and a Si-wafer forming process. Briefly, raw materials such as silica are smelted and refined into polycrystalline silicon, which is further manufactured into a monocrystalline silicon ingot through the Czochralski method that uses chunks of virgin polycrystalline silicon. These chunks are melted down and placed in a quartz crucible along with small quantities of dopants such as boron for *p*-type doping, and phosphorus, arsenic and antimony for *n*-type doping. After heating over a melting temperature of Si to  $\sim 1420^{\circ}\text{C}$ , a seed is put on top to nucleate the Si and direct the orientation of the crystal. By modulating the pulling speed, the *mono-Si* ingot with minimized defects can be obtained. The wafer-manufacturing starts from the slicing into a raw wafer with specified dimensions, followed by lapping, polishing and cleaning processes (**Figure 7a**). In accordance with SEMI<sup>®</sup> standard, the ultra-flat disk needs to be ultra-clean, virtually free of microparticles or other impurities and polished to a mirror-like surface. As for Si-PV, material needs to have high purity of 99.9999% (wt%) and for chip application, it is 99.999999999%.<sup>84</sup>

For *mono-HP* wafer manufacturing, attempts relying on the Bulk-crystal Slicing technology have been reported starting from 2016. The large perovskite crystal (**Figure 7b**) was sliced into thin wafers (**Figure 7d**) at Xi'an LONGI Silicon Materials by Liu's group.<sup>85</sup> Compared with other slicing facilities such as laser cutting, inner circle slicing, multiple wire slicing, *etc.*, that usually cracked or burnt the crystal into fragments, the diamond wire sawing machine exhibited a good compatibility to acquire complete *mono-HP* wafer. They optimized the conditions by using the diamond wire with a diameter of 0.08 mm, and MAI saturated IPA solution as the coolant, with a sawing speed of 20 m/s,

and the feeding rate of 0.7 mm/min, obtaining the thin *mono-HP* wafer with 120 mm lateral size and  $\sim 100$   $\mu\text{m}$  thickness.<sup>85</sup> It should be noted that perovskite materials have lower Young's module ( $\sim 19$  GPa<sup>86</sup>) than Si (140-180 GPa<sup>87</sup>) and are extremely sensitive to moisture. These require particular protection when slicing the perovskite materials. Particularly, typical wire cutting and mechanical polishing could shrink the thickness of *mono-HP* wafer to  $\sim 200$   $\mu\text{m}$ . But further polishing upon this thickness level would easily cause mechanical damage due to its high fragility. Lv *et al.*<sup>88</sup> developed a wet-etching method to engineer the wafer thickness. They used the residual mother liquor that was used to grow the crystal to etch the surface of a *mono-HP* wafer. By immersing a  $\sim 200$   $\mu\text{m}$  thick MAPbI<sub>3</sub> wafer in the etching solution by modulating the immersion time, temperature and concentration, desired thickness down to 15  $\mu\text{m}$  has been achieved.<sup>88</sup> Similar wet-etching strategies can also be seen in the field of *mono-Si* wafer area. For example, Lin *et al.*<sup>89</sup> reported the fabrication of a 30  $\mu\text{m}$  thickness *mono-Si* chip using a chemically etching method. Li *et al.*<sup>90</sup> obtained 18  $\mu\text{m}$  free-standing *mono-Si* membranes by wet-etching a 500  $\mu\text{m}$ -thick wafer. Taking advantages of the mature slicing technique from *mono-Si* field, such as its ability in controlling the crystal-facet orientation, flexibility in product dimension, technical maturity with streamlined and high throughput process, and good compatibility with existing manufacturing market, transferring this technology to *mono-HP* wafer can be a promising direction. Nevertheless, several fundamental problems need to be taken into consideration before the transition, which includes (i) slicing- and lapping-caused surface defects, (ii) short of proper materials for surface treatment such as damage etching, atomicscale polishing, and ultrapure cleaning, (iii) concerns on the high sensitivity to oxygen and moisture of perovskite, (iv) dynamic material degradation, crack, brittle fracture and poor mechanical property, and (v) kerf loss.

On the other hand, following the nature of slicing the crystal in mechanical aspect, another derivative is the mechanical exfoliation, which has been widely employed in the field of traditional 2D materials such as graphene and molybdenum disulfide (MoS<sub>2</sub>). The lower-dimensional perovskites such as the well-known BA<sub>2</sub>MA<sub>n-1</sub>Pb<sub>n</sub>I<sub>3n+1</sub>,<sup>54</sup> PEA<sub>2</sub>MA<sub>n-1</sub>Pb<sub>n</sub>I<sub>3n+1</sub>,<sup>91</sup> have good compatibilities to this technique because of their unique van der waals heterostructures.<sup>92,93</sup> The inorganic [PbI<sub>6</sub>]<sup>4-</sup> octahedral layer are separated by the

organic bilayers of BA or PEA, and the intermolecular interaction between neighboring organic layers is the van der Waals bond, the bonding energy of which is orders of magnitude lower than the covalent and ionic bonds. This gives an easy way to exfoliate several single-crystalline layers from the bulk crystal. Peng et al.<sup>94</sup> prepared the 2D *mono-HP* wafer of  $(\text{C}_6\text{H}_5\text{C}_2\text{H}_4\text{NH}_3)_2\text{PbI}_4 \cdot (\text{CH}_3\text{NH}_3\text{PbI}_3)_{n-1}$  ( $n = 1, 2, \text{ and } 3$ ) using this method. Similarly, Niu et al.<sup>95</sup> reported mono- and few-layer thick 2D *mono-HP* wafer of  $(\text{C}_6\text{H}_9\text{C}_2\text{H}_4\text{NH}_3)_2\text{PbI}_4$ . Particularly, they found a clear difference in the exciton properties between “bulk” ( $> 15$  layers) and very thin ( $< 8$  layer) regions, and ascribed that to the structural rearrangement of organic molecules around the inorganic sheets. As the mechanical exfoliation typically cannot obtain a large complete sample with uniform layers, then hierarchical terrace-like feature with planner inner terrace region and layer-edge region is usually observed (**Figure 7e**)<sup>96</sup>. As can be seen in **Figure 7f**, the exfoliated 2D perovskite displays the layer-edge step,<sup>97</sup> quantified by the unit thickness multiplied by layer-numbers. A side-view example of a  $(\text{C}_4\text{H}_9\text{NH}_3)_2(\text{CH}_3\text{NH}_3)_{n-1}\text{Pb}_n\text{I}_{3n+1}$ ,  $n = 4$ , 2D *mono-HP* crystal can be viewed in **Figure 7g**.<sup>54</sup> These layer-edges have been observed with conductive feature with the help of conductive atomic force microscopy (C-AFM) measurement (**Figure 7h**).<sup>43</sup> A topographical feature of “insulating/conductive/insulating” across the layer-edge (**Figure 7i**) suggests potential applications in microscopic electronics.<sup>43</sup> Overall, in spite of these exciting findings from 2D *mono-HP* thin film prepared from the mechanical exfoliation method, the intrinsic drawbacks such as low reproducibility, small area, and low homogeneity limit its up-scale applications.



**Figure 7 Bulk-crystal Dicing technology.** (a) Industrial mono-Si wafer manufacturing scheme showing the mono-Si ingot pulling process from multicrystalline silicon (multi-Si), through melting, seeding, and pulling. Si-wafer forming process from bulk mono-Si ingot dicing, lapping, polishing, and cleaning. Dicing technology for mono-HP wafer processing starting from (b) single HP bulk, adapted from reference<sup>98</sup>, Copyright © 1999-2019 John Wiley & Sons, Inc. through (c) dicing by diamond wire saw, adapted from reference<sup>6</sup>. Copyright © 2018 Elsevier Inc. (d) A real photograph showing the sliced mono-HP wafer of MAPbI<sub>3</sub>, adapted from reference<sup>85</sup>. Copyright © 2017, Science China Press and Springer-Verlag GmbH Germany. (e) Optical and AFM images of the exfoliated (C<sub>4</sub>H<sub>9</sub>NH<sub>3</sub>)<sub>2</sub>(CH<sub>3</sub>NH<sub>3</sub>)<sub>n-1</sub>Pb<sub>n</sub>I<sub>3n+1</sub>, n = 3, 2D perovskite microplates with different thicknesses. Adapted from reference<sup>96</sup>. © 2018 IOP Publishing Ltd. (f) AFM image with the height profile of an exfoliated layer. The layered structure of the Br-based perovskite with n = 1 is evident with a monolayer step of 1 nm as shown in the inset. Adapted from

reference<sup>97</sup>. Copyright © 2017 American Chemical Society. **(g)** Side-view SEM of a  $(C_4H_9NH_3)_2(CH_3NH_3)_{n-1}Pb_nI_{3n+1}$ ,  $n = 4$ , 2D mono-HP crystal. Adapted from reference<sup>54</sup>. Copyright © 2018 American Chemical Society. **(h)** A C-AFM setup detecting the layer edge of a 2D mono-HP crystal, and **(i)** an example of C-AFM current mapping showing the conductive layer-edge. Adapted from reference<sup>43</sup>. © 2019 American Association for the Advancement of Science.

#### 4. Mono-HP photovoltaics

The absence of GB and the significantly minimized trap densities in single-crystals leads to the superb charge transport property and a scenario of approaching and even breaking the Shockley-Queisser limit. For example, recent investigations revealed the below-bandgap absorption in *mono-HP* photovoltaics, which could be expected to break the limit by taking advantage of photons in the NIR to IR region *via* an in-direct band transition.<sup>68</sup> The findings of intrinsic twin domains in tetragonal  $CH_3NH_3PbI_3$  *HP* by Rothmann *et al.*<sup>99</sup> also provide additional room for relaxing the stress and strain within the perovskite lattice to improve the device performance. The persistent ferroelectric domains in  $MAPbI_3$  *mono-HP* confirmed by Garten *et al.*<sup>100</sup> provide the evidence for the early conjectures on the contribution from ferroelectric domain walls<sup>41,42,100</sup> that can provide charge transport highways for photocarriers and also provide the opportunity of “Ferroelectric photovoltaics” that can surpass the Shockley-Queisser limit with the ferroelectric domain wall contribution.<sup>101,102</sup> Multi-photon excitations,<sup>103,104</sup> nonlinear optical preproperties,<sup>105</sup> and up-conversion<sup>106</sup> phenomena observed in *mono-HP* suggests the potential in taking advantages of photons with long wavelength beyond the absorption edge. Recent discoveries themed on photon recycling in analogous to a solar concentration effect<sup>45</sup> and hot-carrier cooling to use the hot carriers before thermalization<sup>44</sup> in *HP* imply a potential PCE of 66%. Back to the *mono-HP* photovoltaics, designing and constructing a device architecture that can maximize these effects is of the first priority to obtain the proof-of-concept ultrahigh performance devices.

##### 4.1 Lateral Mono-HP PV device

The solar cell can be constructed in either lateral or vertical architectures depending on the alignment between the photocarrier transport direction and the illumination direction.

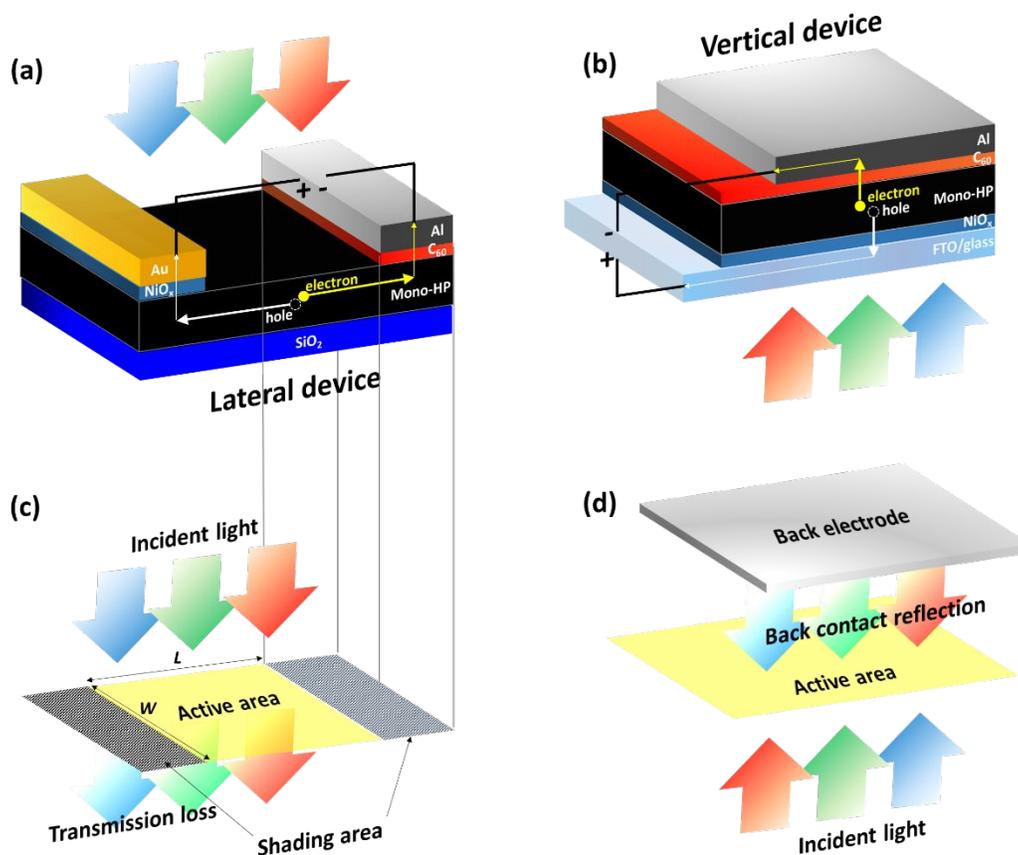
**Figure 8** displays two exemplified device architectures of lateral and vertical device. Normally, in any solar cell an internal electrical potential gradient (e.g., “*p-n* junction” in Si solar cell,<sup>107</sup> “electron donor: acceptor heterojunction” in organic solar cell<sup>108</sup>) is required to arouse a depletion region responsible for separating the photo-generated charge carriers and/or driving each type of carriers to their corresponding electrodes. This internal electrical field can be provided by the work function difference of electrode materials, heterostructures induced potential gradient, dipole, space charge and interfacial effects by various buffer layer materials.<sup>109</sup> Meanwhile, to passivate the surface traps, minimizing the Schottky barrier at the interface, with the help of various *n*-type and *p*-type interfacial modification materials, have been widely attempted in solar cells, photodetectors, and LED. Similarly, for *mono-HP* PVs, *n*-type buffer layers including  $\text{TiO}_x$ ,<sup>108,110</sup>  $\text{ZnO}$ ,<sup>111</sup>  $\text{SnO}$ ,<sup>112</sup>  $\text{C}_{60}$ ,<sup>111</sup> PCBM,<sup>111,113</sup> etc., and *p*-type buffer layers including PEDOT:PSS,<sup>114</sup>  $\text{NiO}_x$ ,<sup>115</sup> Spiro-OMeTAD,<sup>116</sup> P3HT,<sup>117</sup> etc., can also be applied. **Figure 8a** shows an exemplified lateral device, where a *mono-HP* is supported by a  $\text{SiO}_2$  substrate and different electrodes (coupled with/without buffer layers) are deposited separately on the crystal, leaving an open channeled area for receiving the photons. Such a design enables the fabrication of a whole device only on one side of the crystal, hence the issues about crystal thickness or the deposition of transparent electrode can be ignored. However, one deadly drawback is the low-usage of the light exposure area. As shown in **Figure 8c**, there is a shading area of electrode that blocks the light absorption, leaving a smaller uncovered open channel with dimension of  $L \times W$  being the effective device area. In addition, such area is also limited by the charge carrier diffusion length of *mono-HP*. For example, when the channel length  $L$  exceeds the diffusion length (hyper-micro-scale), the photogenerated charge carriers are prone to recombine to produce the energy loss the before arriving at the electrodes. Meanwhile, the deficiency of back-contact reflection also leads to a large optical transmission loss (**Figure 8c**). All these jointly lead to low PCEs for lateral *mono-HP* PVs. The early attempt for lateral *mono-HP* PVs relies on a piezoelectric poling effect to evoke the device asymmetry.<sup>118</sup> Chen *et al.*<sup>118</sup> reported a strong piezoelectric effect in  $\text{MAPbI}_3$  *mono-HP* (**Figure 9a**), which enables the poling within the single crystals under a nonuniform electric field. The strain-generated grain boundaries provide paths for the ion

migration and finally form a *p-i-n* structure (**Figure 9b**). As a result, a lateral Au/*mono-HP*/Au device with sufficient polling treatment exhibit a  $V_{OC}$  of 0.61 V,  $J_{SC}$  of 2.28 mA  $cm^{-2}$  and PCE of 1.88% (**Figure 9c**). Despite of its low PCE, the lateral *mono-HP* PV device can be a new route to efficient low-cost solar cells due to its simple device configuration of metal/*mono-HP*/metal. Such a design eliminates the need for more expensive transparent electrodes. In the meantime, instead of electrical poling, intentionally doping the *mono-HP* and/or introducing *n*-type and *p*-type buffer layers at the cathode and anode, respectively, to preserve longer carrier depletion length is a good way to improve the PCE. Following the buffer layer interfacial modification strategy, Lee *et al.*<sup>77</sup> designed a *mono-HP* solar cell using metal electrodes with different work functions and a *n*-type cathode buffer layer of PCBM (**Figures 9e & 9f**). The best lateral *mono-HP* device exhibits a  $J_{SC}$  of 18.33 mA  $cm^{-2}$ ,  $V_{OC}$  of 0.801 V, FF of 0.329 and PCE of 4.83% which is significantly higher than the polycrystalline lateral device with a maximum PCE of 0.194% (**Figure 9f**). This can be ascribed to the higher mobility, *i.e.*, 45.64  $cm^2V^{-1}s^{-1}$  of the *mono-HP* vs. the 0.2512  $cm^2V^{-1}s^{-1}$  of the polycrystalline film. Similarly, Liu *et al.*<sup>57</sup> constructed an analogous device structure using the  $C_{60}$ /BCP as the cathode buffer layer (**Figures 9g-9i**). The lateral device exhibits a PCE of 5.9% under 0.25 sun light, with a  $J_{SC}$  of 5.06 mA  $cm^{-2}$ ,  $V_{OC}$  of 0.66 V and FF of 0.44. As the single-crystal has an extremely low trap-density within its crystal, the SRH recombination loss may still occur at the crystal surface. Technically, the surface trap is the major reason for those low efficiencies in terms of recombination loss. Modifications on the *mono-HP* surface to minimize the trap density using learnings from various interfacial modification cases is expected to improve the device efficiency.

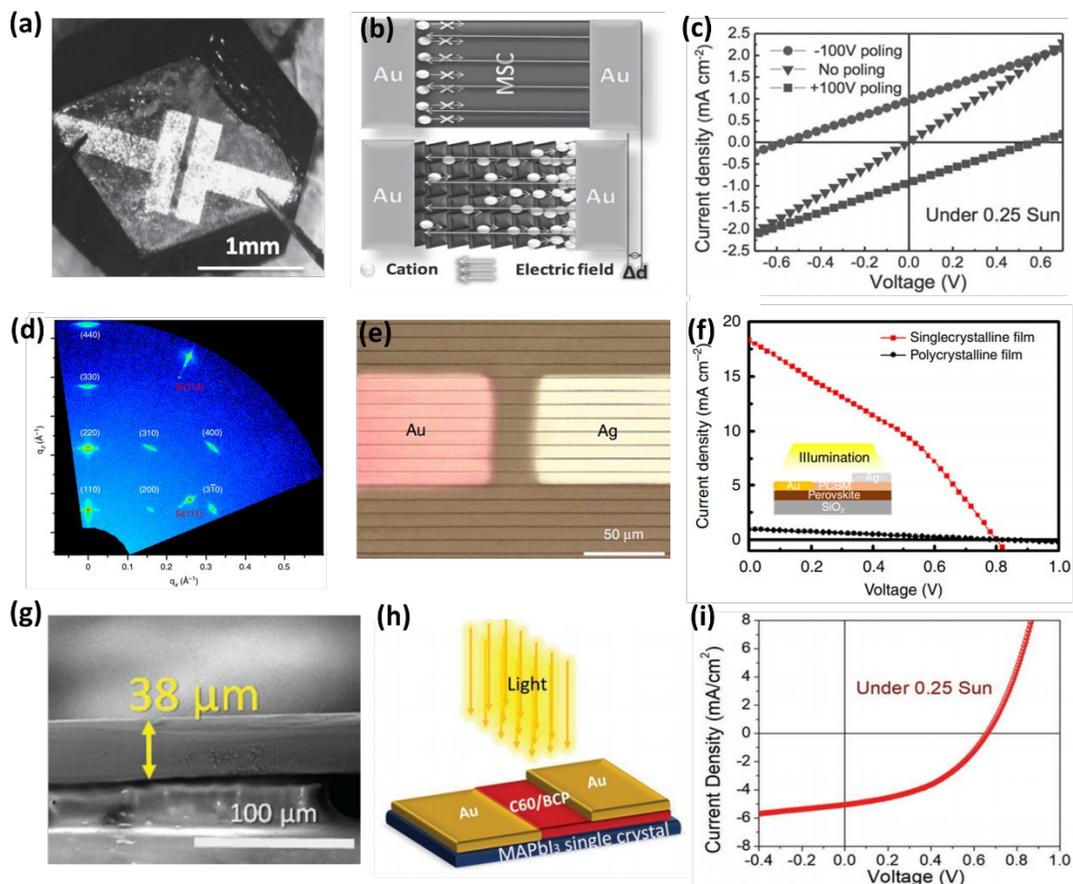
Bearing the diffusion length of several or more micrometers (*e.g.*, 175  $\mu m$  in the prototype  $MAPbI_3$  single crystal), a thinner wafer is of greater importance in terms of depletion width and diffusion length, either of which set up the limit distance for charge traveling before recombination. Otherwise, a thicker film will cause the charge loss in the region beyond the limit distance. However, handling an ultrathin wafer with micrometers scale thickness seems practically challenging. Alternatively, enhancing the diffusion length/depletion width by proper doping may provide the solutions to the thickness issue.

As the ultimate goal is to secure sufficient charge carriers reaching the electrodes and thereby minimize the charge loss from recombination, an introduction of localized electrical field especially at the interface can sufficiently adjust the depletion region and regulate the drifting-diffusion balance, which can sufficiently improve the device performance. For example, the employment of ionic liquid in Light-Emitting Electrochemical Cells (LEC),<sup>119,120</sup> can provide mobile ions that are driven to boundaries under bias at elevated temperatures and frozen at room temperature to give an ion-generated electrical field. This electrical field can help charge separation and transport in the device. Similar mechanism facilitating the charge separation, extraction, transport, and collection can be found in the organic photovoltaics (OPVs), where such a localized electric field can be provided by the interfacial “dipoles”,<sup>121</sup> coercive electrical field from functional nanoparticles,<sup>122</sup> and functional ferroelectric interlayers.<sup>123</sup> In the case of perovskite, constructing a *p-i-n* structure by perovskite self-doping is a good attempt to break the electrode symmetry and simplify the device architecture through eliminating the necessity for expensive transparent conductive electrode (TCE). Typical methods including electrical poling induced by ion migration and self-doping dominantly rely on the grain boundary that provide the ion migration path in polycrystalline perovskite.<sup>124</sup> While in single crystal perovskite, as the twice larger energy barrier for ion migration within in single crystal domain than the grain boundary, the ion-assisted self-doping seems difficult to realize in single crystal perovskite. But the primitive demonstration on the self-doping of single crystal perovskite through a “Piezoelectric Poling” effect<sup>118</sup> can be a good try.

Alternatively, since the “*Space-limited method*” provide the direct perovskite crystal growth on transparent conductive substrate, building the device upon these single crystal membranes coated transparent electrode is then regarded as the promising techniques. Therefore, various strategies growing *mono-HP* on FTO and/or ITO substrate and constructing the solar cell device upon it have been reported, which turns out into the ‘vertical device’.



**Figure 8** Two exemplified device architectures for the mono-HP solar cell. (a) A lateral device structure where the photocarrier transport direction in the mono-HP is perpendicular to the photon incident direction. (b) A vertical device structure where the photocarrier transport direction in the mono-HP is parallel to the photon incident direction. Photoactive area of (c) lateral device and (d) vertical device.



**Figure 9** Lateral mono-HP device and performance. **Piezoelectric poling strategy for antisymmetric device.** (a) An image of MAPbI<sub>3</sub> lateral structure single-crystal device. (b) Scheme of electromechanical strain generated grain boundaries and ions migration in mono-HP. (c) Switchable photovoltaic effect of a MAPbI<sub>3</sub> lateral mono-HP solar cell with positive and negative poling. Adapted from reference<sup>118</sup>. Copyright © 1999-2019 John Wiley & Sons, Inc. **Buffer layer strategy for antisymmetric device.** (d) Two-dimensional X-ray diffraction (2D XRD) image of the mono-HP thin film. (e) An optical microscopic image of a lateral mono-HP solar cell with metal electrodes. The light brown and dark brown lines indicate mono-HP and spaces, respectively. (f) J-V curves of single crystalline (red) and polycrystalline (black) perovskite thin film lateral mono-HP cell. The inset shows a schematic device structure of a lateral perovskite solar cell and the direction of illumination. Adapted from reference.<sup>77</sup> Copyright © 2017, Springer Nature. (g) SEM images of cross-section of MAPbI<sub>3</sub> mono-HP wafer. (h) Scheme of MAPbI<sub>3</sub> mono-HP lateral-structure solar cell. (i) The J-V curve of showing a PCE of 5.9%. Adapted from reference<sup>57</sup>. Copyright © 1999-2019 John Wiley & Sons, Inc.

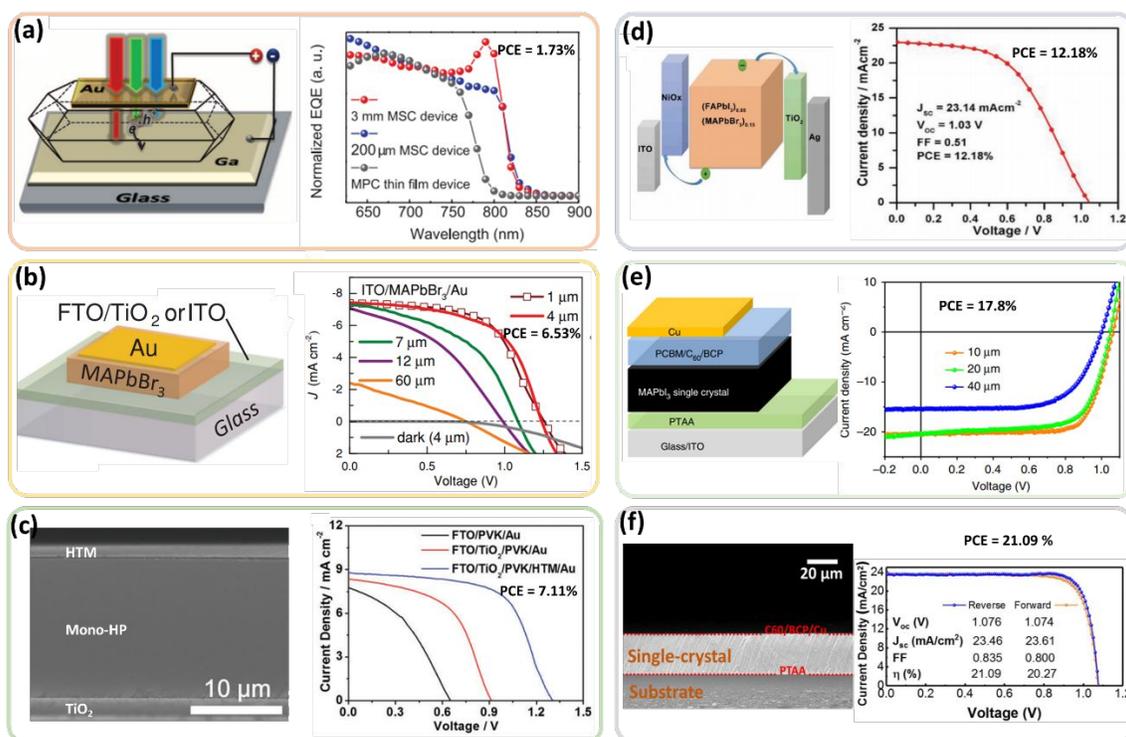
#### 4.2 Vertical Mono-HP PV device

To better accommodate the crystal dimension with the carrier diffusion length, the vertical *mono-HP* device design incorporating *mono-HP* with thickness at microscale or smaller is proposed, which can give a higher efficiency. The earliest *mono-HP* vertical device was built based on a bulk single crystal of MAPbI<sub>3</sub> with millimeter thickness<sup>49</sup> (the device is schematized in **Figure 10a**). Bearing the maximal diffusion length of 175  $\mu\text{m}$  for MAPbI<sub>3</sub> single crystal, such a large thickness causes dramatic charge carrier recombinations during the vertical transport through the bulk single crystal.<sup>98,125</sup> Furthermore, to construct the electrical asymmetry for separate electron and hole collection, different metals of Ga and Au are used as the electrodes. This design is not compatible for solar cell application as no light path is provided to pass through any electrode, rather it is good for gammavoltaic application.<sup>49</sup> Using an intense cesium-137 source, a gammavoltaic PCE of 1.73% has been observed. Constructing solar cell devices upon the *mono-HP* requires a small crystal thickness. A study focusing on the PCE dependence on the *mono-HP* thickness was reported in the *mono-HP* of MAPbBr<sub>3</sub> by Peng *et al.*<sup>126</sup> As can be seen in **Figure 10b**, they tuned the *mono-HP* thickness from 4 to 60  $\mu\text{m}$ , and modified the cathode side with the *n*-type buffer layer, TiO<sub>2</sub>. Device with *mono-HP* of smaller thickness delivered higher PCE due to the significantly improved the fill factor (FF). Since FF is closely correlated with the charge carrier mobilities in the device. A larger FF in the thinner *mono-HP* device suggests the improved carrier mobilities. Using a simple ITO/*mono-HP*/Au structure without any buffer layers, a nearly 100% IQE (internal quantum efficiency) and PCE >5% has been obtained.<sup>126</sup> While modification on the electrode further improve the PCE to 6.5% with a remarkable V<sub>OC</sub> of  $\sim 1.4$  V.<sup>126</sup> The positive role of interface engineering has been evidenced in the *mono-HP* device. It should be noted that the MAPbBr<sub>3</sub> *mono-HP* has a cubic crystal structure at room temperature and easy to grow than the MAPbI<sub>3</sub>. Hence, lots of early attempts of *mono-HP* devices are built upon the MAPbBr<sub>3</sub> material. Rao *et al.*<sup>66</sup> also utilized the MAPbBr<sub>3</sub> *mono-HP* to construct the solar cells (**Figure 10c**). Particularly, they modified both the cathode and anode with different buffer layers, *i.e.*, TiO<sub>2</sub> and spiro-MeOTAD, respectively, to minimize the Schottky barrier. A MAPbBr<sub>3</sub> *mono-HP* with thickness of 16  $\mu\text{m}$  and a size of 6 $\times$ 8 mm displays the highest PCE of 7.11%. Another

milestone for *mono-HP* device can be seen in the  $(\text{FAPbI}_3)_{0.85}(\text{MAPbBr}_3)_{0.15}$  *mono-HP*.<sup>127</sup> Such a mixed *mono-HP* is believed to deliver high photocurrent due to the smaller bandgap of  $\text{FAPbI}_3$ . With  $\text{NiO}_x$  and  $\text{TiO}_x$  interfacial modification layers (**Figure 10d**), the device has a better extraction and anti-charge blocking effect, rendering a PCE of 12.18%. Later in 2017, Chen *et al.*<sup>68</sup> fabricated the  $\text{MAPbI}_3$  *mono-HP* solar cell with a decent PCE of 17.8%. By adjusting the thickness at the level of tens of micrometer, they found the spectral response of the  $\text{MAPbI}_3$  *mono-HP* solar cell is extended to 820 nm, which is 20 nm broader than the corresponding polycrystalline thin-film solar cells. They ascribed such phenomena to the indirect bandgap absorption or Urbach band tail, which might be expected to challenge the Shockley-Queisser limit by utilization of such additional photons. The highest PCE of *mono-HP* devices was reported in 2019, with an efficiency of 21.09%<sup>128</sup> for  $\text{MAPbI}_3$  *mono-HP* device. By shrinking the thickness down to  $\sim 20$   $\mu\text{m}$ , and employing a device structure of ITO/poly(triarylamine) (PTAA)/ $\text{MAPbI}_3$  *mono-HP*/ $\text{C}_{60}$ /BCP/Cu,  $J_{\text{SC}}$  of 23.46  $\text{mA cm}^{-2}$ ,  $V_{\text{OC}}$  of 1.076 V, and FF of 83.5% has been obtained. It should be noted that such values are measured in the inert nitrogen atmosphere. They observed the performance could drastically decrease when the device was measured under ambient conditions (22 °C, 50-55 RH), particularly for the  $J_{\text{SC}}$ .<sup>128</sup> Overall, the *mono-HP* device seem more promising in achieving ultrahigh device performance, compared to their polycrystalline counterparts. However, current studies revealed a general lower PCE of the *mono-HP* solar cell compared to the *poly-HP* device. The major reason is the thickness of the *mono-HP* layer, which is extremely difficult to control in a sub-micrometer scale, let alone the surface homogeneity and surface traps of the *mono-HP*.

Clearly, beyond the thickness concern, the buffer layers that can induce depletion region, extract charge carriers, select/block and transport/collect electrons or holes are also crucial to the overall PCE. The functionality of these buffer or interfacial modification layers are similar to those already applied in the photoelectronics using polycrystalline perovskite thin films.<sup>108</sup> Besides the traditional small area devices, incorporating the perovskite single crystal into large area solar module has also been researched. A good try can be seen in the wafer-scale *mono-HP* patterned thin films based on the geometrically-confined lateral crystal growth, which displaying the 3 × 3 inch solar module with a PCE

of 4.83%.<sup>77</sup> It should be mentioned that the (i) lateral device structure with long lateral distance between electrodes and the (ii) improper contact with direct electrode without buffer layer may act as the main reason for the insufficient PCE. Additionally, other device structures fabricated by different manufacturing methods such as “top-down approach”,<sup>129</sup> atomically scissoring,<sup>130</sup> molecular bonding, self-assembled monolayer (e.g., APTES) assisted bonding,<sup>47</sup> “two slides sandwiching”<sup>131</sup> may bring additional insights to the processing. But overall, only sophisticated techniques capable of growing homogeneous, flat, surface-trap-free, thin and large *mono-HP* wafer/thin film are developed, the efficiency could further complete over the *poly-HP* devices.



**Figure 10** Milestone vertical *mono-HP* device and performance. (a) Schematic device structure of the  $\text{MAPbI}_3$  *mon-HP* devices. Normalized EQEs of 3-mm-thick and 200- $\mu\text{m}$ thick  $\text{MAPbI}_3$  *mon-HP* devices compared with a thin-film device. Adapted from reference<sup>49</sup>. Copyright © 2015, American Association for the Advancement of Science. (b) A  $\text{MAPbBr}_3$  *mon-HP* devices with/without cathode buffer layer and device performance of device based on  $\text{MAPbBr}_3$  *mon-HP* of different thicknesses. Adapted from reference<sup>126</sup>. Copyright © 1999-2019 John Wiley & Sons, Inc. (c) Cross-sectional SEM image of  $\text{MAPbBr}_3$  *mon-HP* devices with a highest PCE of 7.11%. Adapted from reference<sup>67</sup>. © The Royal Society of Chemistry 2017. (d) The band alignment and J-V curve of the highest PCE of *mon-HP* devices using  $\text{ITO}/\text{NiO}_x/(\text{FAPbI}_3)_{0.85}(\text{MAPbBr}_3)_{0.15}/\text{TiO}_2/\text{Ag}$ . Adapted from

reference<sup>127</sup>. Copyright © 1999-2019 John Wiley & Sons, Inc. (e) Device structure and J-V curve of single crystal device using MAPbI<sub>3</sub> mono-HP with different thickness. A PCE of 17.8% has been obtained. Adapted from reference<sup>68</sup>. Copyright © 2017, Springer Nature. (f) Cross-sectional SEM image of a MAPbI<sub>3</sub> mon-HP device with the J-V curves showing a record PCE of 21.09%. Adapted from reference<sup>128</sup>. Copyright © 2019 American Chemical Society.

### 4.3 Ultrahigh PCE?

Although in principle single crystal devices could outperform their polycrystalline counterparts because of the GB absence and minimal defect density, the current device performance is still unsatisfying. **Table 1** summarizes the performance parameters of the state-of-the-art single crystal perovskite solar cells in last three years. The PCE derives from 0.75% to 21.09%, where most works reported < 10% PCE, which is clearly lower than the typical value of their polycrystalline counterpart devices (*ca.* 18% from various current researches). The inferiority in PCE can be associated with several factors: (i) *Surface trap*. Although the bulk trap density is orders of magnitudes lower in single crystals, it is noted that there still exists large density of surface traps,<sup>132</sup> which can induce ionic charges due to the uncoordinated sites at the surface. To finely tune the surface properties, methods including surface passivation by fullerene,<sup>133</sup> ionomer,<sup>134</sup> ionic liquid<sup>120</sup> and Lewis base<sup>135</sup>, and compositional regulation by argon plasma treatment (APT),<sup>136</sup> have been applied. Additionally, the structural asymmetry at the surface can induce non-trivial physical properties, especially in lower-dimensional perovskite materials. Recently, we found highly conductive crystal edges in the 2D BA<sub>2</sub>PbI<sub>4</sub> perovskite multiple quantum well (MQW) structures exhibiting a super high carrier density of 10<sup>20</sup> cm<sup>-3</sup>, approaching that in metal. As several intrinsic surface properties of perovskite crystal still remains unclear, further physical and chemical investigations may bring new insights. (ii) *Surface hydration*. Structural asymmetry generated terminal crystallographic ions are vulnerable to various environmental stimuli such as moisture and oxygen.<sup>137</sup> Definitely, single-crystal devices with hydrated facets will form a poor contact with electrodes, result in high leakage currents and severe resistive losses despite their excellent bulk properties. Overcoming the integration challenges associated with the hydrated or degraded interfaces require a profound understanding of the surface characteristics and the eventual chemical

transformation.<sup>138</sup> (iii) *Buffer layer*. In any solar cells, buffer layer is crucially important for efficient extraction and transport of certain type of charges to the electrodes. In this context, energy level, mobility, transparency (front layer), and stability need to be considered basically. Various relevant researches in OPVs, DSSCs, Si, GIGC solar cells can be revisited regarding to the buffer layer materials.<sup>108</sup> (iv) *Thickness tradeoff*. Thicker single crystal wafer enables the indirect band absorption (thus higher photocurrent) and ease in handling and processing, but may also introducing more traps and recombination loss. Thus, balancing the potential risk in recombination loss by designing suitable thickness of the *mono-HP* needs to be carefully considered.

**Table 1** Performance parameters of the state-of-the-art *mono-HP* devices.

Device type	Device architecture	Light source	Thickness	J <sub>sc</sub> (mA cm <sup>-2</sup> )	V <sub>oc</sub> (V)	FF	PCE (%)	ref
vertical	ITO/PEDOT:PSS/MAPbI <sub>3</sub> /PCBM/Ag paste or Al			0.04	0.55	34.1	0.75	129
vertical	ITO/PEDOT:PSS/MAPbI <sub>3</sub> /PCBM/ZnO/Al	AM 1.5G	300 nm ~ 3 mm	8.69	0.52	0.38	1.73	139
vertical	Ga/MAPbI <sub>3</sub> /Au	intense cesium-137 source	3 mm				3.90	49
vertical	ITO/PEDOT:PSS/MAPbI <sub>3</sub> /PCBM/Ag	AM 1.5G	50 μm	22.15	0.75	0.27	4.40	140
vertical	ITO/MAPbBr <sub>3</sub> /Au	AM 1.5G	1 μm	7.39	1.25	0.59	5.49	
vertical	ITO/MAPbBr <sub>3</sub> /Au	AM 1.5G	4 μm	7.42	1.24	0.58	5.37	
vertical	ITO/MAPbBr <sub>3</sub> /Au	AM 1.5G	7 μm	7.19	1.11	0.46	3.7	
vertical	ITO/MAPbBr <sub>3</sub> /Au	AM 1.5G	12 μm	7.09	1.03	0.39	2.82	126
vertical	ITO/MAPbBr <sub>3</sub> /Au	AM 1.5G	60 μm	2.27	0.94	0.31	0.65	
vertical	FTO/TiO <sub>2</sub> /MAPbBr <sub>3</sub> /Au	AM 1.5G	1 μm	6.69	1.36	0.69	6.53	
vertical	FTO/MAPbBr <sub>3</sub> /Au	AM 1.5G	16 μm	7.77	0.65	0.39	1.98	
vertical	FTO/TiO <sub>2</sub> /MAPbBr <sub>3</sub> /Au	AM 1.5G	16 μm	8.35	0.91	0.53	4.08	67
vertical	FTO/TiO <sub>2</sub> /MAPbBr <sub>3</sub> /HTM/Au	AM 1.5G	16 μm	8.77	1.31	0.62	7.11	
vertical	FTO/TiO <sub>2</sub> /MAPbI <sub>3</sub> /Spiro-OMeTAD/Ag	AM 1.5G		22.283	0.668	0.59	8.78	141
vertical	ITO/NiOx/(FAPbI <sub>3</sub> ) <sub>0.85</sub> (MAPbBr <sub>3</sub> ) <sub>0.15</sub> /TiO <sub>x</sub> /Ag	AM 1.5G	24.5 μm	23.14	1.03	0.51	12.18	127
vertical	ITO/PTAA/MAPbI <sub>3</sub> /PCBM/C <sub>60</sub> /bathocuproine (BCP)/Cu	AM 1.5G	10 μm	21	1.08	0.786	17.80	68
vertical	ITO/PTAA/MAPbI <sub>3</sub> /PC <sub>61</sub> BM/C <sub>60</sub> /BCP/Cu	AM 1.5G	15 μm	21.2	1.05	0.73	16.30	
vertical	ITO/PTAA/MAPbI <sub>3</sub> /PC <sub>61</sub> BM/C <sub>60</sub> /BCP/Cu, w/ APT treatment for 2 s	AM 1.5G	15 μm	22.5	1.11	0.816	20.40	136
vertical	ITO/PTAA/MAPbI <sub>3</sub> /C <sub>60</sub> /BCP/Cu	AM 1.5G	~20 μm	23.46	1.076	0.835	21.09	128
lateral	Au/MAPbI <sub>3</sub> /PCBM/Au	AM 1.5G		3.84	0.802		4.83 <sup>a</sup> , 6.6 <sup>b</sup>	77
lateral	Au/MAPbI <sub>3</sub> /Au, Piezoelectric poling treatment	25 mW cm <sup>-2</sup> (0.25 sun)		2.28	0.82		5.36 <sup>c</sup> , 1.88 <sup>d</sup>	118
Lateral	Au/MAPbI <sub>3</sub> /C <sub>60</sub> /BCP/Au	25 mW cm <sup>-2</sup> (0.25 sun)		5.06	0.66	0.44	5.9	57

<sup>a</sup> average PCE, <sup>b</sup> champion PCE, <sup>c</sup> obtained at 170 K and <sup>d</sup> obtained at room temperature.

#### 4.4 Device Stability

The public acceptance of *HP* PV technology is on basis of its reliability not only in terms of high efficiency but also a satisfying lifetime. The *HP* materials are suffering from their low stability against moisture, heat and radiation.<sup>142</sup> The answer to the stability problem may also be firstly found in the *mono-HP* devices.

The moisture is usually regarded as the chief culprit for the device degradation of *HP* PV. With the presence of moisture, various degradation mechanisms including the formation of hydrate product of  $(\text{MA})_4\text{PbI}_6 \cdot 2\text{H}_2\text{O}$ ,<sup>143</sup> phase transition from  $\alpha$  to  $\delta$  in  $\text{FAPbI}_3$  and  $\text{CsPbI}_3$  systems,<sup>144,145</sup> *etc.*, have been researched. Moisture infiltration into the inner perovskite typically starts from the grain boundaries (GBs)<sup>146</sup> and a high trap-density will also facilitate the moisture induced degradation via an ion-migration mechanism<sup>146,147</sup>. Because of the virtue of ultralow trap density and free of GBs, the *mono-HP* is expected to have years stability in air. For example, an unencapsulated  $\text{MAPbI}_3$  *mono-HP* device can endure 30 days in dark air (23 °C and RH 30%) and shows no degradation.<sup>68</sup> A *mono-HP* device using a structure of  $\text{FTO}/\text{TiO}_x/\text{mono-HP}/\text{Spiro-MeOTAD}/\text{Au}$  has been reported to maintain 93% of its initial PCE after aging for 1000 *hrs*.<sup>66</sup> The all-inorganic  $\text{CsPbBr}_3$  *mono-HP* device exhibits three-month stability in air of RH 20% at room temperature.<sup>83</sup> It should be noted that all these devices are freshly made and no further encapsulation techniques were applied. Recent wrapping methods such as atomic level protection using the fluorination treatment<sup>148</sup>, can also be used to these *mono-HP* device for prolonging their lifetime.

In addition to moisture, heat can also induce stability issues such as phase transition and chemical decomposition. For example,  $\text{MAPbI}_3$  could have phase transition from tetragonal ( $I4cm$ ) to cubic ( $Pm\bar{3}m$ ,  $Z = 1$ ) phase when the temperature increases across 327 K ( $\sim 54$  °C).<sup>149</sup> In *poly-HP*, decomposition at GBs can be triggered at relatively lower temperatures and accelerated at elevated temperatures due to the corrosive contaminants that are typically stored in voids and GB. For example, the  $\text{MAPbI}_3$  *poly-HP* thin film usually exhibits a decomposition temperature of  $\sim 150$  °C, while the *mono-HP* wafer can sustain higher temperatures up to 240 °C.<sup>65</sup> Similarly, the *mono-HP* wafer of  $\text{MAPbCl}_3$ ,  $\text{MAPbBr}_3$  and  $\text{FAPbI}_3$  are reported to have a high decomposition temperature of 214, 257,

and 300 °C, respectively.<sup>46</sup> Additionally, for the all-inorganic perovskite of CsPbI<sub>3</sub>, it can go up to 567 °C until melting, which not only displays a good thermal stability but also provide a potential way for casting the crystal film using a ‘*melting method*’.<sup>150,151</sup>

Photoinduced degradation process can be another mechanism inducing the degradation of *HP* device, as the ions in *mono-HP* can be activated upon photon radiation and the migration of these ions as well as the photocatalytic effects can trigger the damaged contacts at the interface between different layers.<sup>152–154</sup> The GBs and trap states are known to accelerate the ion migration by providing percolation pathways,<sup>147,155–158</sup> which together with the photon energy that activates the ions jointly leads to the photodegradation process for *poly-HP* devices. In contrast, the *mono-HP* can be a good platform to reduce and/or eliminate the ion migration and hence the mass transport induced material degradation. Particularly, for (quasi-)2D perovskite materials that have extremely low in-plane and out-of-plane ion migration properties,<sup>159</sup> the mass transport (ion migration) induced degradation can be circumvented.

## 5. *Mono-HP* transistors

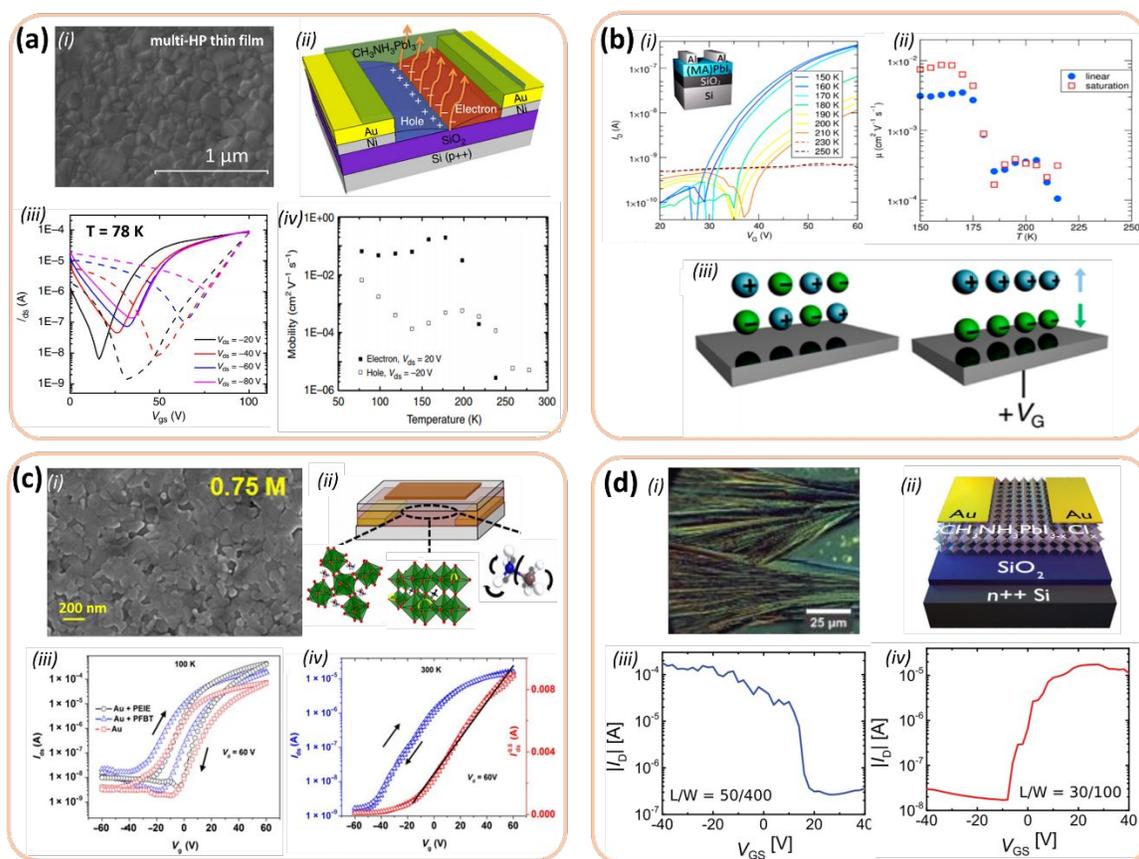
The *HP* materials display extremely low effective mass of electron and hole and hence large carrier mobilities as well as the ambipolar transport characteristics,<sup>160–162</sup> which makes them good candidate for field-effect transistors (FETs). However, limited number of research efforts have been conducted in this direction due to the device unreliability. The ion migration and accumulation at the interface of dielectric layer and the gate-field screening effect in *HP* polycrystalline films,<sup>158,163</sup> substantially reduces the charge carrier mobility that damages the normal functionality of the transistor device. Minimizing the ion migration in the *poly-HP* materials *via* the application of *mono-HP* can be a promising solution to mitigate or even overcome such gate-field screening effect.

### 5.1 *Ion migration influence*

The prototype *HP* material, MAPbI<sub>3</sub>, with the experimentally determined large intrinsic charge carrier mobility and ambipolar conductivity, seems to be a good material for transistor application. However, several studies from different research teams coincidentally

found the MAPbI<sub>3</sub> *poly-HP* based device only show the FET characteristics at very low temperatures but no FET behavior at room temperature.<sup>164–166</sup> Building upon MAPbI<sub>3</sub> *poly-HP* thin film, Chin *et al.*<sup>164</sup> fabricated the first light-emitting FET in 2015 (**Figure 11a**). Using a bottom contact/bottom gate (BC/BG) device configuration and spin-coated MAPbI<sub>3</sub> *poly-HP* film on prepatterned Au/Ni (50 nm/10 nm) electrodes, tunable electroluminescence was observed at a low temperature range from 78 to 178 K, through the mechanism of recombination of balanced electron & hole injection from the opposite metal electrodes. Linear regime at drain-to-source voltage  $V_d = \pm 20$  V was obtained at 78 K, while both electron and hole mobilities drop quickly upon temperature increasing (**Figure 11a (iv)**) and no transistor characteristics were obtained at room-temperature. They attributed the absence of room-temperature transistor characteristics to the ion screening effects, which are associated to the presence of the ions accumulated at the perovskite/dielectric interface that block further charge injection.<sup>164</sup> Similarly, Labram *et al.*<sup>165</sup> fabricated a top contact/bottom gate (TC/BG) FET using spin-coated MAPbI<sub>3</sub> *poly-HP* film with aluminum electrodes on top, as illustrated in the inset of **Figure 11b**. They found that the electrical characteristics exhibited low source-drain currents and no field induced current modulation at room temperature, but there was a field-effect below 220 K and the drain current continues to increase as the temperature further decreases. This might be linked to the temperature dependence of charge carrier mobility (**Figure 11b (ii)**). And a screen mechanism has been provided, as the MAPbI<sub>3</sub> might exhibit substantial polarization susceptibility an electric field through the mobile ions or alignment of the dipolar molecular cation, and these polarization responses would lead to an electronic screen layer that electrically block that field (see **Figure 11b (iii)**). Such a mechanism is expected to result in a screening of applied gate voltage in the FETs and thereby inhibiting the carrier accumulation and electrical conductivity of the channel. Both the polarization due to local molecular motion and the diffusion of ionic species in the *HP* solid are expected to be temperature-activated.<sup>167–169</sup> In parallel, as the ion migration is closely related with the activation energy of ions, and in *poly-HP* film with high GB and trap densities, such active ions and vacancy can be much more. This will give a high ionic contribution in poorer quality *poly-HP* films. Inversely, optimization of the *poly-HP* film

to reduce the GB and trap density can be an avenue to efficient FET devices. For example, Senanayak *et al.*<sup>163</sup> reported that through optimization of the microstructure of a *poly-HP* film as well as the modifications at source-drain contact, it is possible to significantly minimize the instability and hysteresis in FET characteristics and demonstrate an electron field-effect mobility of  $0.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  at room temperature. Briefly, they employed the  $\text{Pb}(\text{Ac})_2$  based precursor mixture and acquired a uniform thin film with a small root-mean-square (RMS) roughness of  $\sim 5.4 \text{ nm}$ . Through optimizing the device by tuning the grain size from 38 to 150 nm from adjusting the precursor concentrations, modifying the gold S-D contacts with self-assembled monolayer (SAM) of pentafluorobenzenethiol (PFBT,  $\sim 1 \text{ nm}$ ) and the polymer surface modification layer of polyethylenimine ethoxylated (PEIE,  $\sim 2 \text{ nm}$ ), excellent room-temperature *n*-type transfer behavior has been realized in the  $\text{MAPbI}_3$  FET device, showing negligible hysteresis.<sup>163</sup> Similarly, Zeidell *et al.*<sup>170</sup> employed the solvent vapor annealing method to adjust the microscopic structure of the *poly-HP* film. As can be seen in **Figure 11d (i)**, vapor annealing treatment can foster the crystal forming the needle like feature. And by controlling the experimental conditions, a significant morphological change in which the preferential orientation can be modulated and the grain size can be increased drastically with healing the GBs into intermediate phases upon the solvent molecules. As a result, they demonstrated high-performance ambipolar perovskite FETs that exhibit mobilities greater than  $10 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  at room temperature. Representative ( $I_D$ - $V_{GS}$ ) characteristics for both hole and electron transport in the saturation regime (drain-source voltage,  $V_{DS} = -40 \text{ V}$ ) are shown in **Figure 11d (iii) & (iv)**, respectively.<sup>170</sup>

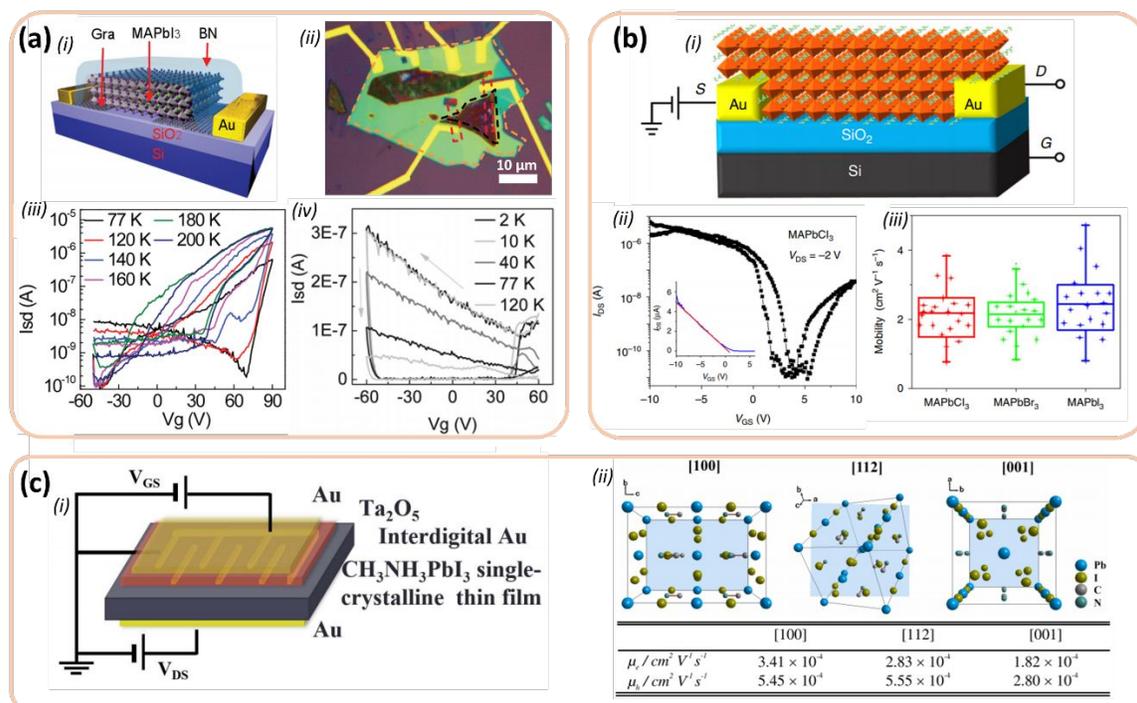


**Figure 11 Poly-HP FETs.** (a) MAPbI<sub>3</sub> poly-HP film (i) and corresponding FET device configuration (ii). Transfer characteristics obtained at 78 K (iii). Temperature dependence of field-effect electron and hole mobilities (iv). Adapted from reference<sup>164</sup>. Copyright © 2015, Springer Nature. (b) Transfer curves of MAPbI<sub>3</sub> poly-HP FET measured at various temperatures between 150 and 250 K. The device has a length and width of 200 and 2600  $\mu\text{m}$ , respectively, and a geometric capacitance of the dielectric was 23  $\text{nF cm}^{-2}$ . Inset: schematic representation of the FET. Si labels the silicon gate electrode, SiO<sub>2</sub> the 150 nm silicon oxide dielectric, (MA)PbI<sub>3</sub> the semiconductor layer, and Al the aluminum source and drain electrodes (i). Approximated field-effect mobility evaluated using the gradual-channel approximation as a function of measurement temperature (ii). Schematic illustration of proposed polarization mechanism of mobile ionic species in MAPbI<sub>3</sub> poly-HP, under the influence of external applied gate field (iii). Adapted from reference<sup>165</sup>. Copyright © 2015 American Chemical Society. (c) SEM images of an optimized MAPbI<sub>3</sub> mono-HP film fabricated from 0.75 M precursor solutions (i). Schematic of top-gate bottom-contact poly-HP FETs summarizing the different sources of disorder mechanisms prevalent in a perovskite (left: vibrations of inorganic cage; middle: defect migration; right: MA<sup>+</sup> polarization disorder) (ii). Transfer characteristics at 100 K for different S-D contact modification (iii) and 300 K for PEIE-treated Au contacts (iv). Adapted from reference<sup>163</sup>. © 2017 American Association for the Advancement of Science. (d) Optical microscopic image of the MAPbI<sub>3-x</sub>Cl<sub>x</sub> poly-HP film in the channel region after 20 min of solvent exposure; note the formation of large needle-shaped crystals (i). Poly-HP FET geometry (ii). Representative plot of I<sub>D</sub>-V<sub>GS</sub> characteristics (V<sub>DS</sub> =  $\pm$  40 V) for holes (iii) and

electrons (iv), respectively. The values of the channel lengths and widths are included in the inset. Adapted from reference<sup>170</sup>. Copyright © 1999-2019 John Wiley & Sons, Inc.

Overall, any strategy that can minimize the charged point defects located at GBs, decrease the polarization fluctuation of the ions with larger grains, and optimize the contact to induce highly crystalline order as well as isolate the S-D electrode from the perovskite is effective to efficient FET devices. Certainly, *mono-HP* with extremely low defect density, high mobility, free of GB and high structural order is a better platform. However, corresponding investigations based on *mono-HP* FET device is rarely reported. Until recently, Li *et al.*<sup>166</sup> reported the FET based on the MAPbI<sub>3</sub> *mono-HP* microplates. They grew the *mono-HP* microplates adopting a method of patterned growth of regular arrays of perovskite microplate crystals.<sup>171</sup> In the meantime, they also incorporated the mono- and bilayer graphene stripes as the source-drain contact electrodes for the *mono-HP* FETs, for not only tuning the barrier height at the interface of graphene/*mono-HP* but also reducing the contact profile to enable a smooth device capable of fully encapsulation by a boron nitride (BN) layer for higher device stability (**Figure 12a (i)**). By examining the field effect, they found the temperature can modulate the doping type of the MAPbI<sub>3</sub> *mono-HP*. At low temperature, the material exhibits a *p*-type behavior, which gradually diminishes when the temperature increases and finally vanishes around 180 K (**Figure 12a (iii)**). At even lower at 2 K, the *p*-type behavior retains and the source-drain current continuously increases with decreasing temperatures, as can be seen in **Figure 12a (iv)**.<sup>166</sup> It should be noted, as the device is built upon the *mono-HP* crystal, the electron mobility determined from such FET device displays a large value of 4 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> at 77 K, which is dramatically larger than those in *poly-HP* FET devices. Yu *et al.*<sup>71</sup> demonstrated high-performance FET devices based on MAPbX<sub>3</sub> (X = Cl, Br, and I) *mono-HP* with both in BGTC and BGBC device configurations (**Figure 12b**). The on/off current ratio ranging from 10<sup>3</sup> to 10<sup>5</sup> was readily achieved at room temperature. The devices showed lower operating voltages than 5 V and BCBG design even displays the lowest voltages < 2 V. Maximum room temperature mobilities of 2.6-4.7 and 0.26-2.2 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> have been obtained for electron and holes, respectively. Interestingly, as the MAPbCl<sub>3</sub> has a wide bandgap, the device is almost transparent in the visible range, making it promising candidates for applications in

transparent and imperceptible electronics.<sup>71</sup> On the other hand, the form of *mono-HP* also enables people to understand its anisotropy in charge transport. For example, Lv *et al.*<sup>172</sup> constructed a MAPbI<sub>3</sub> *mono-HP* FET device (**Figure 12c (i)**). They built the vertical-structured FET devices using MAPbI<sub>3</sub> *mono-HP* with specific crystal directions (*i.e.*, [100], [112], [001]) parallel to the device out-of-plane direction and investigated their ambipolar field-effect characteristics in dark along these directions. Compared to the [100] and [112] orientation, charge carriers have lower mobility along the [001] direction.<sup>172</sup> Some materials have the birefringence which differentiates the moving speed of photons along different directions in crystals. The birefringence can be used for time-resolved double-slit experiment with entangled photons.<sup>173</sup> Analogously, the electrical anisotropy in *mono-HP* might be a good platform for similar time-resolved double-slit experiment of electrons.



**Figure 12 Mono-HP FETs.** (a) Schematic of the back-gate, back-contact MAPbI<sub>3</sub> *mono-HP* FET built on a 300 nm SiO<sub>2</sub>/Si substrate with monolayer graphene as contact, covered by a BN layer (i). The optical image of the BN covered device with the graphene (red dashed lines), perovskite (black dashed line), and BN (dark yellow dashed line) highlighted by different color lines. The *mono-HP* thickness is  $\sim 150$  nm (ii). The temperature dependent transfer characteristics in low temperature (iii) and ultralow temperature range (iv). Adapted from reference<sup>166</sup>. Copyright © 1999-2019 John Wiley & Sons, Inc. (b) Schematic representation of bottom-gate, bottom-contact FET device (i). The *mono-HP* is

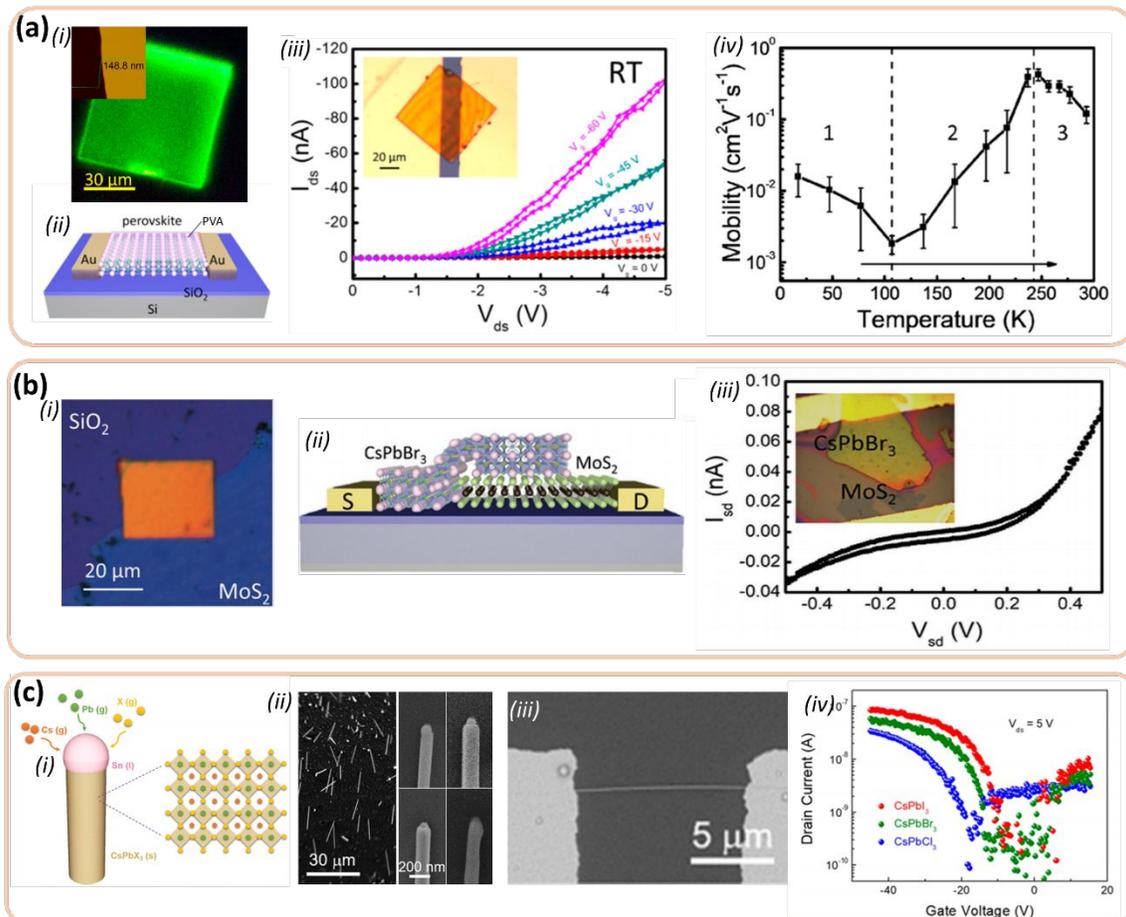
$\text{MAPbX}_3$  ( $X = \text{Cl}, \text{Br}, \text{I}$ ). A representative transfer characteristic of  $\text{MAPbCl}_3$  mono-HP FET device (ii), using forward/reverse gate voltage sweeps from  $-10$  to  $10$  V at a rate of  $0.05 \text{ V s}^{-1}$ , with  $V_{\text{DS}} = -2$  V. Inset: the linear regime of the respective devices. Field-effect hole mobility distribution for 20 devices fabricated and tested for each halide perovskite (iii). Adapted from reference<sup>71</sup>. Copyright © 2018, Springer Nature. (c) Sketch of a vertical-structured mono-HP FET of  $\text{MAPbI}_3$  (i). Views of crystal structure along  $[100]$ ,  $[112]$ , and  $[001]$  orientation and corresponding FET mobility in each direction (ii). Adapted from reference<sup>172</sup>. © Copyright 2019 IEEE.

## 5.2 $\text{CsPbX}_3$ mono-HP based FET

Above we have mentioned the ion migration issues in most  $\text{MAPbI}_3$  based HP FETs. However, besides the low activation energy of the  $\text{MA}^+$  from the lattice, the organic cation is also sensitive to moisture and heat. Comparatively, replacing the A-site organic cation with the inorganic alkalis would provide stronger moisture and thermal stability. Considering the ion size as well as the tolerance factor<sup>174</sup> that describes the geometric stability of the crystal lattice,  $\text{CsPbX}_3$  represents the principle inorganic perovskite material for optoelectronic applications.<sup>175–177</sup> Meanwhile, several other HPs, e.g.,  $\text{Cs}_x(\text{MA}_{0.17}\text{FA}_{0.83})_{1-x}\text{Pb}(\text{Br}_{0.17}\text{I}_{0.83})_3$ ,<sup>160</sup> using mixed components have also been reported. For example, Huo *et al.*<sup>178</sup> reported the  $\text{CsPbBr}_3$  mono-HP based FETs (**Figure 13a (i) & (ii)**). The  $\text{CsPbBr}_3$  mono-HP micro platelet was obtained by van der Waals epitaxy, and transferred to the FET substrates using a pick-up method with no liquid involved, hence no surface damage in the platelets. Field effective hole mobility ( $\mu_h$ ) of  $0.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and on-off ratio of 6,700 at room temperature, along with a  $\mu_h$  of  $1.04 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and on-off ratio  $> 10^4$  at 237 K, have been obtained, respectively (**Figure 13a (iv)**). The mobility in  $\text{CsPbBr}_3$  mono-HP FETs is still determined by the interaction between the charge carriers, ions, and phonons at the semiconductor-dielectric interface. While the ion migration plays an important role in the electrical-transport process at a relatively higher temperature than  $\sim 237$  K, and the interaction of charge carriers and phonon scatterings dominates at low temperature (below  $\sim 237$  K). The  $\text{CsPbBr}_3$  mono-HP devices also displayed one-month ambient stability, owing to the material's intrinsic robust stability as well as the protentional functionality of the poly(vinyl alcohol) (PVA) film coated outside the perovskite.<sup>178</sup> Additionally, they further constructed a heterojunction of mono-HP and traditional 2D materials such as graphene,  $\text{MoS}_2$  (**Figure 13b (i)**), and hexagonal BN (h-

BN).<sup>179</sup> Such a CsPbBr<sub>3</sub> *mono-HP/2D* material (graphene, MoS<sub>2</sub>, and h-BN) heterostructures were achieved by the van der Waals epitaxy.<sup>178</sup> As the MoS<sub>2</sub> has the best energy level alignment with the CsPbBr<sub>3</sub> *mono-HP*, the CsPbBr<sub>3</sub>/MoS<sub>2</sub> heterojunction FET (**Figure 13b (ii)**) exhibits the best device performance in the study. Using a channel length of 100 μm, the FET exhibits a hole mobility of 0.08 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> in dark, and 0.28 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> under a 442 nm laser illumination with an intensity of 0.2 mW cm<sup>-2</sup>, driven by a low voltage of 0.5 V at room temperature in ambient air. Such a van der Waals heterojunction of perovskite/2D material combines the excellent properties of both perovskite and 2D materials and reduce the resistance loss into heat through a minimized Schottky barrier, which may help to minimize the device size and the corresponding power dissipation.<sup>179</sup> Additionally, CsPbX<sub>3</sub> based quantum dot (QD) materials that have nanometer size or smaller and coated with organic ligands have also been employed in the FET, particularly for light emitting diode (LED) applications. The confinement energy in smaller QDs due to the energy levels split increase the total emission energy and the emission at various wavelengths. And the organic ligands are supposed to protect the QDs against moisture. Such HP-QD light emitting FET has been reported in the field of quantum LED (QLED), QD display, *etc.*<sup>180–182</sup> Beyond these 0D (QD) and 2D (microplate) *mono-HPs*, the one-dimensional (1D), *i.e.*, nanowire HP, is another type material for FET application. In particular, 1D *HP* has been demonstrated to exhibit many interesting properties, attracting various potential applications, such as optical communication, computing, imaging, Fabry-Perot cavity and the gain medium for optical amplification.<sup>183–186</sup> Recently, Meng *et al.*<sup>187</sup> developed a CsPbX<sub>3</sub> 1D *mono-HP* FET device. They employed the catalytic vapor-liquid-solid (VLS) growth method for growing the CsPbX<sub>3</sub> 1D nanowire. **Figure 13c (i)** displays the schematic diagram illustration of the VLS growth process of CsPbX<sub>3</sub> NW (X = Cl, Br, or I) using the Sn catalysts. The SEM image of the vertical CsPbBr<sub>3</sub> NWs grown on SiO<sub>2</sub>/Si substrates and the titled SEM images of different individual CsPbBr<sub>3</sub> NWs grown with the Sn catalytic seeds are shown in **Figure 13c (ii)**. A FET device is constructed by bridging the CsPbBr<sub>3</sub> NW between two electrodes (**Figure 13c (iii)**). The corresponding transfer characteristics using logarithm *y*-coordinate is shown in **Figure 13c (iv)**. Upon illumination from visible regime, the CsPbX<sub>3</sub> 1D *mono-HP* opto-FET device exhibits responsivity

exceeding 4489 A/W and detectivity over  $7.9 \times 10^{12}$  Jones. The dark FET exhibits superior hole field effect mobility of  $3.05 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  at room temperature. The VLS-grown perovskite NWs seem to be versatile platforms for exploring the fundamentals and potential applications on basis of the 1D *mono-HP*.<sup>187</sup>



**Figure 13** CsPbX<sub>3</sub> mono-HP FET. (a) FET based on van-der-Waals-Grown and dry transferred CsPbX<sub>3</sub> mono-HP ultrathin platelets. PL image of a CsPbBr<sub>3</sub> mono-HP ultrathin platelet, with the inset of an AFM image showing the cross-section profile (i). Output characteristic of CsPbBr<sub>3</sub> mono-HP FET at room temperature, with the inset of an optical image of the FET device (ii). Temperature dependence of the FET mobility (iii). Adapted from reference<sup>178</sup>. Copyright © 2017 American Chemical Society. (b) FET based on CsPbBr<sub>3</sub>/2D crystal van der Waals heterojunctions. Optical images of typical CsPbBr<sub>3</sub> thin platelet on MoS<sub>2</sub> (i). Schematic illustration of a CsPbBr<sub>3</sub> mono-HP/MoS<sub>2</sub> heterojunction FET (ii). I<sub>sd</sub>-V<sub>sd</sub> curves of the heterojunction in darkness, with an inset of the optical image of the corresponding device (iii). Adapted from reference<sup>179</sup>. Copyright © 1999-2019 John Wiley & Sons, Inc. (c) 1D nanowire CsPbX<sub>3</sub> mono-HP FET. Schematic diagram illustrating the VLS growth process of CsPbX<sub>3</sub> NW (X = Cl, Br, or I) using the Sn catalysts (i). SEM and titled SEM image of CsPbBr<sub>3</sub> NWs (ii). SEM image of the as-

*fabricated NW FET (iii). Transfer characteristics of the typical single VLS-grown CsPbX<sub>3</sub> (X = Cl, Br, or I) NW FETs using logarithm y-coordinate (iv). Adapted from reference<sup>187</sup>. Copyright © 2019 American Chemical Society.*

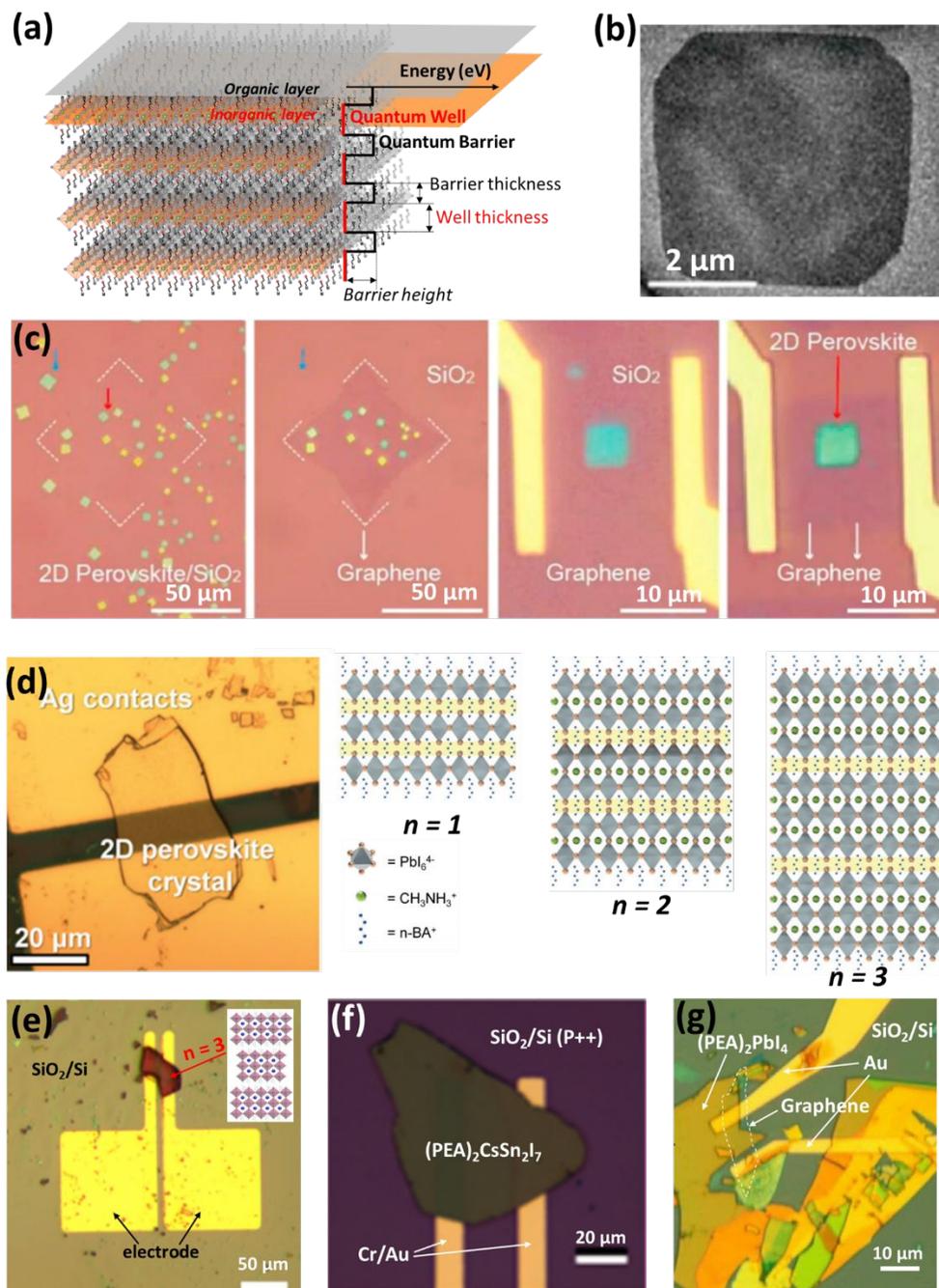
### 5.3 Quasi-2D mono-HP based FET

Compositionally, the prototype *HP* has a chemical formula of ABX<sub>3</sub>, with A being small organic cations and/or alkali metal cations such as Cs<sup>+</sup>, B being bivalent metals such as Pb<sup>2+</sup>, Sn<sup>2+</sup>, and X being the halogen. The size of ions at each crystallographic site need to accommodate with the tolerance factor,<sup>174</sup>  $t = (r_A + r_X)/\sqrt{2}(r_B + r_X)$  with  $r_A$ ,  $r_B$ ,  $r_C$  being the radii of ions at A-, B- and X-sites, respectively. As  $t$  is close to 1, the crystal maintains a 3D structure, while enlarging the  $r_A$ ,  $t$  becomes larger than 1 and the crystal will have lower structural dimensionality, such as the layered two-dimensional (2D) HP. The 2D *HP* has a generic formula of (RNH<sub>3</sub>)<sub>2</sub>(CH<sub>3</sub>NH<sub>3</sub>)<sub>n-1</sub>B<sub>n</sub>X<sub>3n+1</sub>, where R is an alkyl or aromatic moiety, B is a metal cation, and X is a halide.<sup>6</sup> An organic layer consists of the large organic moiety, RNH<sub>3</sub><sup>+</sup>, is typically insulating and playing a role of barrier layer, while the inorganic layer, [(CH<sub>3</sub>NH<sub>3</sub>)<sub>n-1</sub>B<sub>n</sub>X<sub>3n+1</sub>]<sup>2-</sup>, is semiconducting. As the thickness of each layer is scaled down to angstrom and nanometer level, quantum effect takes place in these 2D HPs. Hence, the 2D *HP* structure is also termed by the multiple quantum well (MQW) structure, as shown in **Figure 14a**. The inorganic layer consists the quantum well which confines the charge carriers in the inorganic plane by quantum and dielectric confinement.<sup>188</sup> Hence, typically 2D *HP* is not good material for solar cells, as the photogenerated electron-hole pair is strongly connected with a large exciton binding energy up of 0.5 eV,<sup>189</sup> dramatically higher than the thermal energy at room temperature (0.025 eV). Moreover, the 2D *HP* has an anisotropic charge transport property. In the out-of-plane direction, the organic insulating layer can block the charge transport and the quantum tunneling probability is very low. In the in-plane direction, the charges are easier to move within each inorganic plane, making them having magnitude higher in-plane electrical conductivity than out-of-plane.<sup>6</sup> For example, for BA<sub>2</sub>PbI<sub>4</sub> 2D HP, the in-plane hole mobility is  $8.2 \times 10^{-2} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ , which is over one order of magnitude higher than the out-of-plane mobility of  $4.7 \times 10^{-3} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ .<sup>6</sup> Hence, taking advantages of such an anisotropic transport property, 2D *mono-HP* FET device can be of great interest.

2D *HP* materials have been employed into FET applications since early times. For example, by replacing the A-site cation with large aromatic and aliphatic cations, 2D *HP* such as phenylethyl ammonium tin iodides ((PEA)<sub>2</sub>SnI<sub>4</sub>) or ((C<sub>6</sub>H<sub>5</sub>C<sub>2</sub>H<sub>4</sub>NH<sub>3</sub>)<sub>2</sub>SnI<sub>4</sub>),<sup>190,191</sup> and alkyl ammonium tin iodides ((C<sub>n</sub>H<sub>2n+1</sub>NH<sub>3</sub>)<sub>2</sub>SnI<sub>4</sub> (*n* = 4 to 12)),<sup>192</sup> have been introduced into FETs. Notably, the (PEA)<sub>2</sub>SnI<sub>4</sub><sup>193</sup> was the first *HP* material utilized in FET device, which is initially intended for the channel materials. The reported field effect mobility of (C<sub>n</sub>H<sub>2n+1</sub>NH<sub>3</sub>)<sub>2</sub>SnI<sub>4</sub> (*n* = 4 to 12) are very low about  $\sim 10^{-3}$  to  $10^{-2}$  cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>. Recently, Matsushima *et al.*<sup>194</sup> demonstrate a record field effective hole mobility ( $\mu_h$ ) of up to 15 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> of (PEA)<sub>2</sub>SnI<sub>4</sub> at room temperature by solving the aforementioned issues of low perovskite quality, high carrier trap density, and inefficient carrier injection, through surface treatment of the substrate with a self-assembled monolayer in combination with the adoption of a top-contact/top-gate (TC/TG) structure with hole-injection layers. And a field effective electron mobility ( $\mu_e$ ) of 2.1 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> has also been reported in this 2D (PEA)<sub>2</sub>SnI<sub>4</sub> *poly-HP* thin film.<sup>195</sup> It should be noted that the MASnI<sub>3</sub> *mono-HP* has been observed to have ultrahigh mobility of 2320 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>, significantly higher than its *poly-HP* thin film counterparts.<sup>196</sup> Hence, the (PEA)<sub>2</sub>SnI<sub>4</sub> *mono-HP* is also expected to have extra room for higher mobilities.<sup>194</sup> However, most Sn-2D *HP* FETs are built upon *poly-HP* thin films using spin-casting method for sample preparation and their monocrystalline devices are rarely reported due to the instability of the Sn-2D *HP* materials (Sn<sup>2+</sup> in Sn-2D *HP* can be easily oxidized into Sn<sup>4+</sup>). Comparatively, Pb-2D *HP* materials tend to have higher ambient stability.<sup>197</sup> So far, most studies of Pb-2D *HP* materials also have been concentrated on *poly-HP* thin films, while there are limited reports focusing on the ultrathin 2D *mono-HP* based FETs.<sup>166,171,198</sup> Only a few photo-response FETs based on 2D *mono-HP* have been reported. For example, Tan *et al.*<sup>199</sup> demonstrated the first 2D *mono-HP* based photodetectors with a FET structure, assisted with the protection and electric contact of monolayer graphene. **Figure 14b** shows the low-magnification TEM image of a thin (C<sub>4</sub>H<sub>9</sub>NH<sub>3</sub>)<sub>2</sub>PbBr<sub>4</sub> crystal with a micrometer scale. The devices show promising optoelectronic properties, such as a high current on/off ratio up to 10<sup>3</sup>, low dark current of  $\sim 10^{-10}$  A, demonstrating high photodetection efficiency. Particularly, they used a sub-millimeter-sized single-crystalline graphene film as the medium to convey the as-

synthesized 2D perovskite crystals on to the channel between two electrodes of the FET device (**Figure 14c**). Another well studied material,  $(\text{BA})_2(\text{MA})_{n-1}\text{Pb}_n\text{I}_{3n+1}$ , known as a Ruddelsden-Popper (RP) HP, has also been investigated in FET. Li *et al.*<sup>200</sup> demonstrated a series of 2D *mono-HP* FETs based on high-quality exfoliated 2D  $(\text{BA})_2(\text{MA})_{n-1}\text{Pb}_n\text{I}_{3n+1}$  crystals with varying  $n$  values (**Figure 14d**), under different temperatures. They found the unipolar  $n$ -type transport dominated the electrical properties of all these  $(\text{BA})_2(\text{MA})_{n-1}\text{Pb}_n\text{I}_{3n+1}$  2D RP *mono-HPs*. The transport behavior exhibits a strong dependence on the  $n$  value and the mobility substantially increases as  $n$  increases. The corrected FET mobility values for  $n = 1, 2$ , and  $3$  are  $2 \times 10^{-3}$ ,  $8.3 \times 10^{-2}$ , and  $1.25 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  at  $77 \text{ K}$ , respectively. Additionally, by correlating the temperature-dependent electrical transport and optical measurements, it is found that the origin of the carrier mobility dependence on the phase transition is different between 2D and 3D *mono-HPs*.<sup>200</sup> Li *et al.*<sup>96</sup> also constructed their FET on the basis of the same  $(\text{BA})_2(\text{MA})_{n-1}\text{Pb}_n\text{I}_{3n+1}$  2D RP *mono-HPs*. **Figure 14e** shows the optical image of a FET device based on  $(\text{BA})_2(\text{MA})_{n-1}\text{Pb}_n\text{I}_{3n+1}$  ( $n = 3$ ) 2D *mono-HP* plates. In particular, they also controlled the phase purity by the mechanical exfoliation method. Using this exfoliation method, 2D *mono-HP* microplates with the thickness of around  $20 \text{ nm}$  are obtained, which turns out several repeating unit layers in those *mono-HPs*. By integration with other 2D layered materials such as boron nitride and transferred to prefabricated electrodes, the FET device with photo-response was obtained.<sup>96</sup> Additionally, FET using 2D *mono-HP* materials with different A-site large organic cations have also been investigated. For example, Shen *et al.*<sup>201</sup> reported on a new type of 2D lead-free *mono-HP*, namely,  $(\text{C}_6\text{H}_5\text{C}_2\text{H}_4\text{NH}_3)_2\text{CsSn}_2\text{I}_7$ , with millimeter size and high field-effect hole mobility. They used X-ray diffraction and low-temperature photoluminescence studies to verify the crystalline quality and phase purity, and energy-dispersive spectrometry measurements to confirm the presence of Cs element but absence of  $\text{Sn}^{4+}$  (usually  $\text{Sn}^{2+}$  can be easily oxidized into  $\text{Sn}^{4+}$ , the absence of  $\text{Sn}^{4+}$  indicates the high material purity). Using the as-synthesized 2D *mono-HP*, a high electrical conductivity and a high hole mobility up to  $34 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  at  $77 \text{ K}$  has been obtained. In terms of photoresponse, the corresponding FET device (**Figure 14f**) also exhibit good performance, owing to the excellent optical properties and high electrical conductivity of the 2D *mono-*

*HP*. It should also be noted that the reported  $(\text{C}_6\text{H}_5\text{C}_2\text{H}_4\text{NH}_3)_2\text{CsSn}_2\text{I}_7$  *mono-HP* is free of lead element, suggesting a less-risk material for optoelectronic applications.<sup>201</sup> So far, the 2D *mono-HP* FET has shown great charge carrier mobility and due to the incorporation of large hydrophobic organic cations the 2D *mono-HP* is expected to have higher stability.<sup>202,203</sup> While recently, Zhao *et al.*<sup>204</sup> revealed the spontaneous iodide loss process in 2D *mono-HP*, which acts as an important degradation pathway of the crystal, inducing *n*-type doping of the perovskite semiconductor by generating positively charged iodide vacancies. Moreover, they demonstrated that covering the 2D *mono-HP* with graphene could sufficiently suppress the iodide loss, significantly improving perovskite stability. **Figure 14g** displays the photo-FET with a graphene/2D *mono-HP*/graphene structure, which shows no degradation for 75 days. This, together with above studies from different groups implies that the design using 2D *mono-HP* onto other conventional 2D materials such as graphene and boron nitride can be a promising sensitive diagnostic tool for stable and efficient FET device.



**Figure 14** 2D mono-HP based FET. (a) A general molecular structure of a 2D mono-HP material, showing the MQW structure with energy diagram denoting the organic layer is the quantum barrier and the inorganic layer is the quantum well layer. (b) & (c)  $(C_4H_9NH_3)_2PbBr_4$  2D mono-HP and FET. (b) Low-magnification TEM image of a  $(C_4H_9NH_3)_2PbBr_4$  2D mono-HP. (c) From left to right: optical images of  $(C_4H_9NH_3)_2PbBr_4$  2D mono-HP grown on 300 nm  $SiO_2$ /silicon substrate before, after dry transfer of the graphene film. Within the white dotted line, the 2D crystals are covered by a graphene film, whereas the outside area is uncovered. Optical images of graphene protected

$(C_4H_9NH_3)_2PbBr_4$  2D mono-HP before cutting out a channel, and after devicing with graphene electrodes. Adapted from reference<sup>199</sup>. Copyright © 2016 American Chemical Society. **(d)** Optical image of the exfoliated  $(BA)_2(MA)_{n-1}Pb_nI_{3n+1}$  2D mono-HP with Ag contacts, with the schematic illustration of the 2D mono-HP of different quantum well layer thicknesses, i.e.,  $n = 1, 2,$  and  $3,$  respectively. Adapted from reference<sup>200</sup>. Copyright © 1999-2019 John Wiley & Sons, Inc. **(e)** Optical image of a FET device based on  $(BA)_2(MA)_{n-1}Pb_nI_{3n+1}$  ( $n = 3$ ) 2D mono-HP plates with a thickness of around 20nm. Adapted from reference<sup>96</sup>. IOP PUBLISHING, LTD. **(f)** Optical image of a FET device based on  $(PEA)_2CsSn_2I_7$  2D mono-HP. Adapted from reference<sup>201</sup>. Copyright © 2018 American Chemical Society. **(g)** Optical image of a FET device based on  $(PEA)_2PbI_4$  2D mono-HP. Adapted from reference<sup>204</sup>. © 2018 Elsevier Inc.

#### 5.4 Mono-HP FET future?

The outstanding electronic structure of HP material allows it to possess excellent electronic properties, such as large intrinsic charge carrier mobilities and ambipolar conductivity. These characteristics have imparted success in solar cell and other related applications, with some figure-of-merits approaching or even surpassing the Si- or organic-semiconductor-based counterparts. The *mono-HP* can be designed to exhibit features such as ultra-low trap density, larger charge carrier diffusion length, longer carrier lifetime, higher stability, *etc.* Currently, the state-of-the-art FET devices based on HP materials still have issues such as intrinsic ion migration and hence induced ion-screening effects. The *mono-HP* with reduced GBs and lower concentration of polar mobile ions, and 2D *mono-HPs* with minimized ion migration probability can provide good platforms for mitigating the screening effects. The strong optical response of the *mono-HP* materials coupled with the novel FET designs can provide new opportunity in launching a new wave of research efforts in terms of novel integrated on-chip light sources, wave guides, phototransistors, and electrically pumped semiconductor lasers. The ion-based optoelectronic behavior can also trigger applications such as memristors,<sup>97,205</sup> artificial synaptic connection,<sup>206,207</sup> *etc.* Rapid progress is being made in developing growth techniques for *mono-HPs*, scalable processing of *mono-HP* and in improving the FET performance. Thus, it is expected that many of the above-mentioned materials and device issues will be resolved in near future. Further, many new applications will be developed in related fields such as microprocessor, chip industry, complementary metal-oxide-semiconductor (CMOS) processing, *etc.*

## Outlook

Single crystals are highly appealing platform to investigate the fundamental, intrinsic and natural properties of a material. *Mono-HPs* offer the potential to significantly enhance our understanding of the fundamental nature of the material by removing factors such as GBs, defects, and disordered morphologies. *Mono-HPs* provide pathway towards the ultrahigh device performance due to the reduced energy losses through these imperfections. Compositional tunability of *HP* material also enables the adjustment of multiple properties to satisfy specific application-platform relevant requirements. Building upon the current understanding of the *HP* materials, including in-depth understanding of the basic materials' nature, various applications can be conceived that were not considered earlier. Availability of single crystalline data will drive the development of theory and models in elucidating the underlying mechanisms controlling the physical response of the material. This in turn will drive the design and development of synthesis techniques for *mono-HP* materials to achieve tailored responses for not only *mono-HP* PV and FETs, but also various other applications.

State-of-the-art *poly-HP* PV has set a new PCE record  $> 25\%$ . A straightforward projection suggests that the minimized Shockley-Read-Hall loss in *mono-HP* PVs could lead to a superior efficiency than the current *poly-HP* PVs, and a higher theoretically achievable PCE maximum (30.5%). This implies that the *mono-HP* PVs have the potential to outperform the commercial Si-PVs. Newly discovered nontrivial physics in *mono-HPs* such as ferroelectric electron/hole channels, conductive edge states, photon recycling and slower hot-carrier cooling phenomena, *etc.*, are shedding new light on the promise of PCE breaking the Shockley-Queisser limit. The ongoing research on manufacturing of *mono-HP* wafer/thin films covering variety of growth methods such as *floating*, *space-limited growth*, *vapor phase epitaxy (VPE)*, and *bulk-crystal slicing*, are good examples of possibility to achieve material with desired quality and quantity to explore these phenomena further. In order to boost the PCE of *mono-HP* PV, several problems need to be considered: (i) *purity* – Even though the *HP* material is expected to be defect tolerant, the material with higher crystal phase purity will lead to super electrical properties. For example, efficient Si-PV requires high purity Si of 99.9999 wt% to achieve the reliable

device efficiency. Taking into consideration the complex chemical composition and solution based synthetic routes for synthesis of the *HP* materials, there are challenges in applying the traditional purification processes such as vaporization followed by chemical decomposition to *HP* materials. The surface trap, morphological and/or topographical control can present issues for *mono-HP* devices. (ii) *Mechanics*. *HP* materials are mechanically “soft” and “brittle”. Typical processing techniques used for Si based devices may damage the *HP* materials. Thus, specialized processes need to be developed for handling these *HP* materials. (iii) *Stability*. *HP* materials are very sensitive to the ambient, where moisture, heat, and radiation can cause damage. Thus, dry rooms are required for quality control on fabrication process of *HP* materials and multifunctional coatings that can simultaneously improve hydrophobicity and reduce the surface traps. (iv) *Toxicity*. *Mono-HP* PVs consist of heavy metal which presents some health concerns. Proper encapsulation can be quite helpful at device level but contaminations occurring during materials manufacturing and recycling needs to be addressed. Material design based upon the ion exchange that provides substitute for the lead element with suitable non-toxic replacements will provide transformative progress. Reducing the thickness of the *mono-HP* and properly designing the device structure with efficient electron/hole extraction/blocking layers is important at current stage of R&D for *mono-HP* PVs.

Transistors and the conductive lines are routinely fabricated upon silicon wafer to design electronic chips that drive our smart phones, laptops and all the other electronic gadgets. Manufacturing of typical chips and functional diodes is based on high purity Si wafer that is processed using hi-tech, complex and costly manufacturing processes. Industries have long sought cost-effective and alternative substrates on which to build the next generation of electronics. Alternatives such as the Si thin films and other semiconducting materials have been attempted to manufacture transistors and similar devices. But the challenges are rather complicated manufacturing techniques, particularly the high vacuum condition and high purity processes. In contrast, the *mono-HP* materials processed using solution-based approaches are a lot simpler platforms. The success of *mono-HP*s in solar cell field shows their promise in providing promising alternative to Si in some selected applications. The design of *HP* PVs is maturing and significant progress

is being made in developing *HP* based FETs. In FET devices, charge carriers need to travel at micrometer scale, thus the transport properties of the channel material play critical role. Considering the trap-density, GBs, charge mobility and diffusion length, *mono-HP* materials can be a promising solution. Current research on *mono-HP* FET is at the beginning stage. The proof-of-concept *mono-HP* FET devices reported recently still require high voltage to drive the gate; much higher than practical FETs. Thus, more research is needed in this area to advance the implementation.

In conclusion, *mono-HP* wafer/thin film materials are potentially great platforms for ultrahigh performance PVs and FETs. However, continued research is needed to resolve the pending issues starting from crystal growth process to all the way to device construction. There is great momentum in the community to continue advancing *mono-HP* PVs and FETs and it will be vital for research agencies and industry to preserve this excitement.

### Conflicts of interest

There are no conflicts to declare.

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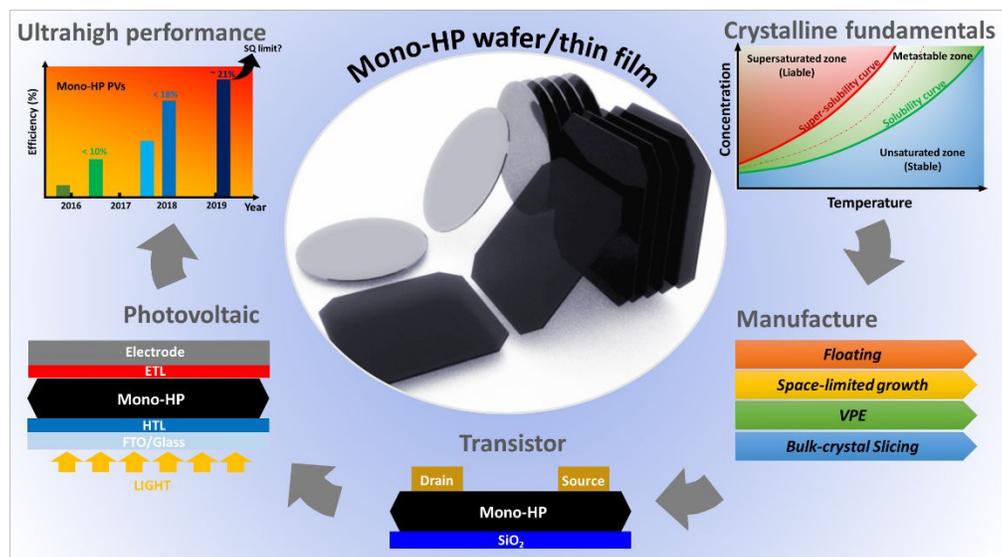
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Graphic TOC:



Text TOC: This review summarizes the edge-cutting area of the “monocrystalline perovskite wafer/thin film” and their intimate applications in photovoltaics and transistors.