



CrystEngComm

**Nanostructured silicon substrates of nanopore morphology
for buffer-layer free nanoheteroepitaxial growth of InP
films**

Journal:	<i>CrystEngComm</i>
Manuscript ID	CE-COM-07-2019-001046.R1
Article Type:	Communication
Date Submitted by the Author:	16-Aug-2019
Complete List of Authors:	Chin, Alan; nLiten Energy Corporation, ; Arizona State University, Gan, Lin; Arizona State University, Ning, Cun-Zheng; Arizona State University, Affiliate Faculty Member in Physics and Materials Science

SCHOLARONE™
Manuscripts

COMMUNICATION

Nanostructured silicon substrates of nanopore morphology for buffer-layer free nanoheteroepitaxial growth of InP films

Alan H. Chin,^{*a, b} Lin Gan,^b and Cun-Zheng Ning^b

Received 00th January 20xx,
Accepted 00th January 20xx

DOI: 10.1039/x0xx00000x

To reduce the cost of III-V solar cells, a buffer-layer free method of depositing high-quality III-V thin films onto low-cost silicon nanostructured substrates is proposed that is enabled by stress relaxation due to the nanopore morphology of the silicon substrate. As a proof-of-concept test of the proposed method, the nanoheteroepitaxial deposition of high quality InP thin film is examined. By comparing the deposition of InP (under conditions optimized for InP deposition onto InP substrates) onto nanostructured Si(100) substrates with nanopore and nanopillar morphologies, the morphology of nanopores is found to be preferred for the nanoheteroepitaxial deposition of InP films.

Despite the substantial cost reduction in solar cells over the past decade, further cost reduction is required to achieve an unsubsidized cost of solar energy that is competitive with the cost of fossil-fuel based energy sources. Compared to the currently dominant solar cells based on silicon, III-V solar cells have achieved the highest efficiencies for both single junction solar cells and multi-junction solar cells because of the high quality and direct bandgap of III-V materials; however, the high cost of III-V solar cells has limited their use to primarily niche applications. This high cost is primarily the result of the requirement for lattice matching to ensure the epitaxially grown III-V material is of high quality. As a result, the current growth of GaAs (and other III-V materials) solar cells on GaAs or

Ge substrates remains too expensive, even when utilizing an epitaxial lift off process.¹

To avoid the use of an expensive GaAs or Ge substrate in the manufacturing of III-V solar cells, the use of an inexpensive Si substrate for the growth of III-V thin films has been considered.²⁻¹⁷ Although a variety of methods (e.g., the use of a porous Si layer¹³, nanoheteroepitaxy^{15, 17}, epitaxial lateral overgrowth (ELOG) of III-V material⁹, the use of a stress-reducing buffer layer¹⁶, and aspect ratio trapping^{8, 10}) have shown promise to enable the high-quality heteroepitaxial growth of III-V materials onto nanostructured Si, issues remain (e.g., residual lattice mismatch, formation of antiphase domains, and thermal mismatch between the III-V material and Si)⁷ in using these methods to achieve the growth of a continuous III-V thin film of high quality. To produce a morphology of appropriate characteristics that provides both a high-quality crystalline substrate to initiate epitaxial growth of a large-area III-V film and stress relief in the epitaxially grown III-V film, the approach based on the use of structured Si is quite promising;^{3, 4, 11} scaling this approach down to the nanoscale may provide further benefits of stress relief in a thinner structured layer. Similarly, nanowire-assisted ELOG can provide stress relief by utilizing an array of III-V nanowires on the silicon substrate.¹⁴ However, the use of smaller structures presents issues in growing continuous III-V thin films.

To address issues with the aforementioned approaches (particularly the nanowire approach) and substantially reduce the cost of the substrate used in the III-V epitaxial growth process, the method proposed in this paper involves the use of low-cost Si nanostructured substrates of nanopore morphology that enables the epitaxial growth of III-V films without the use of a buffer layer. In the proposed method, the spacing between the nanopores and the nanopore diameter can be varied to optimize the subsequent epitaxial growth, in contrast to the difficult-to-optimize porous structure formed by etching. The proposed approach promises to avoid the need for a complex

^a nLiten Energy Corporation, 650 Castro Street, Suite 120-422, Mountain View, California, 94041, USA.

^b School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, Arizona, 85287, USA.

* E-mail: chinah@nlistenenergy.com

Electronic Supplementary Information (ESI) available:

- 1) Experimental details.
- 2) Schematic of the processes of producing nanopillars and nanopores.
- 3) Schematic of the process of producing a self-assembled monolayer of polystyrene spheres used as a mask or a template for a mask.
- 4) SEM images of etched nanopillars in a Si substrate.
- 5) SEM images of etched nanopores in a Si substrate.
- 6) Schematic comparison of the details of the stress relief at the hetero-interface between the InP film and the nanostructured Si substrate for nanopore and nanopillar morphologies.

See DOI: 10.1039/x0xx00000x

and thick (and thus expensive) buffer layer required for traditional III-V on flat Si growth because the stress relief primarily occurs in the region near the nanopore layer. As schematically shown in Figure 1a) and Figure 1d), the nanopore morphology allows the silicon lattice to expand while providing more contiguous surface for epitaxial at the top compared to the nanopillar morphology shown in Figure 1b) and Figure 1e).

In this study, nanostructured silicon substrates of nanopore and nanopillar morphologies were considered to examine the stress relief provided by such substrates for epitaxial InP film growth. Nanostructured substrates of Si were produced via nanosphere lithography combined with etching (see Figure S1 and Figure S2 in the supplementary information).¹⁸ For nanopillar fabrication, polystyrene (PS) spheres were used directly as the mask. The InP or Si wafer to be processed was etched by inductively coupled plasma (ICP) etching. After ICP etching, the PS spheres were removed via exposure in O₂ plasma for 4 min. For nanopore fabrication, a layer of Cr was deposited via thermal evaporation for use as the hard mask. Subsequently, the PS spheres coated with Cr were removed before performing ICP etching of the wafer. Nanopillars (Figure S3 in the supplementary information) and nanopores (Figure S4 in the supplementary information) were considered to determine the most appropriate nanostructured morphology for heteroepitaxial growth of InP onto Si substrates.

Epitaxial InP (lattice mismatch of approximately 8% relative to silicon) thin films were deposited onto nanostructured substrates as well as reference flat substrates of Si (see Table I). The service of SMART Photonics was used to epitaxially deposit p-type InP thin film with thickness of ca. 2 μm. Note that no effort was made to optimize the InP deposition for Si substrates, as their standard epitaxial deposition process onto InP wafers was used (confirmed by deposition onto InP substrates). Using a proprietary metal-organic chemical vapor deposition (MOCVD) process of SMART Photonics (for more information on the MOCVD deposition, see reference¹⁹), the InP film was deposited onto all of the Si substrates in the same deposition run. The Si substrates were cleaned to remove organics and particles prior to deposition. To remove the native oxide, the Si substrates were also dipped in HF solution, rinsed with water, and then dried by blowing with N₂ prior to placement into the MOCVD chamber for InP deposition. The growth rate was ca. 1 micron per hour. The growth occurred with the samples heated at a temperature in the range of 600 - 650 °C. After InP deposition, the samples were cooled to room temperature under low-pressure conditions prior to removing them from the MOCVD chamber. Note that the difference in thermal expansion coefficient also results in stress that promotes polycrystalline growth.²⁰

Figure 1 shows scanning electron microscope (SEM) images of InP on j) nanopore, k) nanopillar, and l) flat Si substrates. Note the more compact morphology of the InP deposited on the nanopore and nanopillar Si substrates compared to the InP

deposited on the flat Si substrate that is indicative of improved stress relief provided by the nanostructured substrates.

To further examine whether the Si(100) nanopore morphology is advantageous for providing stress relief that enables epitaxial deposition of InP, x-ray diffraction (XRD) measurements were performed. The XRD measurements were performed using a high-resolution diffractometer equipped with a Cu-K_α x-ray source. Figure 2a) shows XRD data for the InP film on a Si(100) substrate with 1 micron spaced pores (sample 1), a Si(100) substrate with 1 micron spaced pillars (sample 2), and a flat Si(100) substrate (sample 3). The (200) and (400) InP diffraction peaks were observed in all the InP film samples at different relative intensities (note that the (100) peak is forbidden in InP). However, the (200) and (400) InP XRD peaks for sample 2 were found to be significantly attenuated, and significant peaks from other InP diffraction planes (in particular, (211) and (220)) were observed; this observation indicates that sample 2 is polycrystalline InP (randomly oriented small grains). Similar multiple peaks were observed for sample 3, except with higher relative intensities of the (200) and (400) InP XRD peaks compared to those for sample 2. The InP layer of sample 3 is in the form of many large grains of InP crystals of various orientations produced because of the differences of the lattice constant and the coefficient of thermal expansion between InP and Si. Note that all of the XRD peaks for the InP film of sample 2 were found to be shifted to significantly higher 2θ diffraction angle relative to the XRD peaks of the polycrystalline InP film of sample 3, i.e., the InP film of sample 2 is stressed in a manner that the planes are compressed (reduction in lattice constant from 0.587 nm to ca. 0.579 nm, a relative difference of ca. 1.3%) along the surface normal. An example of the shift in the XRD peak is shown in Figure 2b), which shows a very small peak at 2θ ≈ 31.1° for sample 2 (data for sample 2 is multiplied by 10) that is significantly shifted from that of InP of 2θ ≈ 30.5° (the double-peaked structure is caused by the two Cu-K_α emission lines of the x-ray source). XRD data for an InP(100) wafer are also shown for reference. To more clearly highlight the shift in XRD peaks of sample 2 relative to the XRD peaks of samples 1 and 3, the normalized XRD 400 peaks of the samples are shown in Figure 2c). The small shift and broadening of the (400) InP peak in the XRD data of sample 1 with the 1 μm spaced nanopores indicates that the stress relief in the InP film is even more effective in sample 1 compared to sample 2. Moreover, the 1.3% relative difference in lattice constant of sample 2 indicates that the region of nanopillar morphology does not accommodate the entire 8% lattice mismatch between InP (0.587 nm) and Si (0.543 nm). This residual stress in the compact InP film is likely because the Si nanopillars provide only a small surface area at the top for epitaxial growth. Note that the free expansion of the Si nanopillars allows for growth that is different from the stressed pseudomorphic growth on a flat Si substrate that results in compression of the InP planes perpendicular to the surface normal and expansion of the InP planes along the surface normal. The InP regions on top of the nanopores can enable stress relief in the InP film at the InP-Si hetero-interface (as schematically shown in Figure S5 in the

supplementary information). Note that the (400) InP peak for sample 3 (flat silicon substrate) is almost fully relaxed because of the formation of multiple crystal grains (instead of a continuous film) on the surface of the flat Si(100) substrate.

To provide more evidence of the improved InP material quality with the use of nanostructures Si substrates, the photoluminescence of the samples at room temperature was measured (see Figure 3). The photoluminescence (PL) data from each InP film sample was obtained by illuminating the sample with infrared light (810 nm) from a Ti:sapphire laser (16 μ W average power) incident normal to the surface of the sample and focused onto the sample (ca. 3 μ m diameter spot size) and then collecting the PL using a custom near-infrared microscope setup coupled to a spectrometer with a liquid-nitrogen-cooled InGaAs linear array detector (note the InGaAs array detector cutoff at ca. 0.77 eV and the broad spectral dip at ca. 0.9 eV caused by atmospheric absorption). The average PL data of two spots were obtained for samples 1 and 2, and the average PL data of three spots were obtained for sample 3. The full width at half maximum (FWHM) of the band-edge emission peak of all the samples was found to be approximately the same as the FWHM of the reference InP(100) wafer PL, indicating primarily high-quality InP. The slight redshift of the band-edge PL peak relative to that of the InP(100) wafer PL was found to be caused by laser heating of the InP film (data with greater redshift and broadening at higher laser power is not shown). The lower integrated sub-bandgap PL defect emission of sample 1 is indicative of the higher crystalline quality of the InP film deposited onto the Si(100) nanopore structured substrate, whereas the relatively high (ca. 52% higher than sample 1) integrated sub-bandgap PL of the InP film of sample 2 on Si(100) nanopillars of 1 micron spacing is indicative of the lower crystalline quality of the InP film. The integrated sub-bandgap PL of sample 3 is slightly higher (ca. 4%) compared to that of sample 1, with the PL being lower in the region from 1 to 1.3 eV and slightly higher in the region from 0.8 to 1 eV; these differences may be related to the differences in the surface area and the number of defects at the Si-InP interface between sample 1 and sample 3.

Conclusions

Considering the XRD, PL, and morphological characteristics, the InP film grown on the substrate with nanopore morphology was found to have improved quality (fully relaxed, low defects) compared to the InP film grown on the substrate with nanopillar morphology. The nanopore morphology may be particularly advantageous for stress relief in the InP film because of the reduced stress in the InP film from the expansion of the large area of flat Si at the heterointerface allowed by the nanopore morphology. Further optimization of the InP film quality may be achieved by adjusting the nanopore morphology and the growth conditions.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

This material is based upon work supported by the U.S. Department of Energy under Award Number DE-EE0007369. The authors thank Toshihiko Honda for his help with the x-ray diffraction data collection, Dongying Li and Yueyang Yu for their help with the photoluminescence data collection, and Dr. Seyed Ebrahim Hashemi Amiri, Madhan Kumar Arulanandam, Aditya Siddhanthi, and Dr. Fan Fan for their assistance. The authors acknowledge SMART Photonics for providing the InP epitaxial deposition service. The authors also acknowledge the use of the nanofabrication facilities within the Center for Solid State Science and the characterization equipment at the Eyring Materials Center at Arizona State University.

References

1. J. S. Ward, T. Remo, K. Horowitz, M. Woodhouse, B. Sopori, K. VanSant and P. Basore, *Progress in Photovoltaics*, 2016, **24**, 1284-1292.
2. A. Bakin, D. Piester, I. Behrens, H. H. Wehmann, E. Peiner, A. Ivanov, D. Fehly and A. Schlachetzki, *Crystal Growth & Design*, 2003, **3**, 89-93.
3. R. Bergamaschini, S. Bietti, A. Castellano, C. Frigeri, C. V. Falub, A. Scaccabarozzi, M. Bollani, H. von Kanel, L. Miglio and S. Sanguinetti, *Journal of Applied Physics*, 2016, **120**, 245702.
4. C. V. Falub, H. von Kanel, F. Isa, R. Bergamaschini, A. Marzegalli, D. Chrastina, G. Isella, E. Muller, P. Niedermann and L. Miglio, *Science*, 2012, **335**, 1330-1334.
5. J. F. Geisz, J. M. Olson and D. J. Friedman, presented in part at *the 19th European PV Solar Energy Conference and Exhibition*, Paris (FR), June, 2004.
6. Y. Hiroo, *Semiconductor Science and Technology*, 2002, **17**, 762-768.
7. N. Jain and K. Hudait Mantu, *Energy Harvesting and Systems*, 2014, **1**, 121-145.
8. J. Z. Li, J. Bai, C. Major, M. Carroll, A. Lochtefeld and Z. Shellenbarger, *Journal of Applied Physics*, 2008, **103**, 106102.
9. W. Metaferia, H. Kataria, Y. T. Sun and S. Lourduoss, *Journal of Physics D-Applied Physics*, 2015, **48**, 045102.
10. T. Orzali, A. Vert, B. O'Brien, J. L. Herman, S. Vivekanand, R. J. W. Hill, Z. Karim and S. S. P. Rao, *Journal of Applied Physics*, 2015, **118**, 105307.
11. A. G. Taboada, M. Meduna, M. Salvalaglio, F. Isa, T. Kreiliger, C. V. Falub, E. B. Meier, E. Muller, L. Miglio, G. Isella and H. von Kanel, *Journal of Applied Physics*, 2016, **119**, 055301.
12. M. W. Wanlass, S. P. Ahrenkiel, R. K. Ahrenkiel, D. S. Albin, J. J. Carapella, A. Duda, J. F. Geisz, S. Kurtz, T. Moriarty, R. J. Wehrer and B. Wernsman, presented in part at *the Thirty-first IEEE Photovoltaic Specialists Conference*, Lake Buena Vista, FL, January, 2005.
13. M. M. Wilkins, A. Boucherif, R. Beal, J. E. Haysom, J. F. Wheeldon, V. Aimez, R. Ares, T. J. Hall and K. Hinzer, *IEEE Journal of Photovoltaics*, 2013, **3**, 1125-1131.
14. B. R. Yeom, R. Navamathavan, J. H. Park, Y. H. Ra and C. R. Lee, *Crystengcomm*, 2012, **14**, 5558-5563.

15. D. Zubia, S. H. Zaidi, S. D. Hersee and S. R. J. Brueck, *Journal of Vacuum Science & Technology B*, 2000, **18**, 3514-3520.
16. Y. Han, W. K. Ng, C. Ma, Q. Li, S. Zhu, C. C. S. Chan, K. W. Ng, S. Lennon, R. A. Taylor, K. S. Wong and K. M. Lau, *Optica*, 2018, **5**, 918-923.
17. D. Zubia, S. Zhang, R. Bommena, X. Sun, S. R. J. Brueck and S. D. Hersee, *Journal Of Electronic Materials*, 2001, **30**, 812-816.
18. C.-C. Ho, P.-Y. Chen, K.-H. Lin, W.-T. Juan and W.-L. Lee, *ACS Applied Materials & Interfaces*, 2011, **3**, 204-208.
19. P. J. A. Thijs, E. A. Montie, H. W. Vankesteren and G. W. Hooft, *Applied Physics Letters*, 1988, **53**, 971-973.
20. A. F. I. Morral, J. M. Zahler, H. A. Atwater, S. P. Ahrenkiel and M. W. Wanlass, *Applied Physics Letters*, 2003, **83**, 5413-5415.

Table 1. Si(100) substrates used in the epitaxial InP deposition study

#	Structure type	Distance between structures (nm)	Structure diameter (nm)	Structure height (nm)
1	pores	1000	500	400
2	pillars	1000	600	740
3	flat	n/a	n/a	n/a

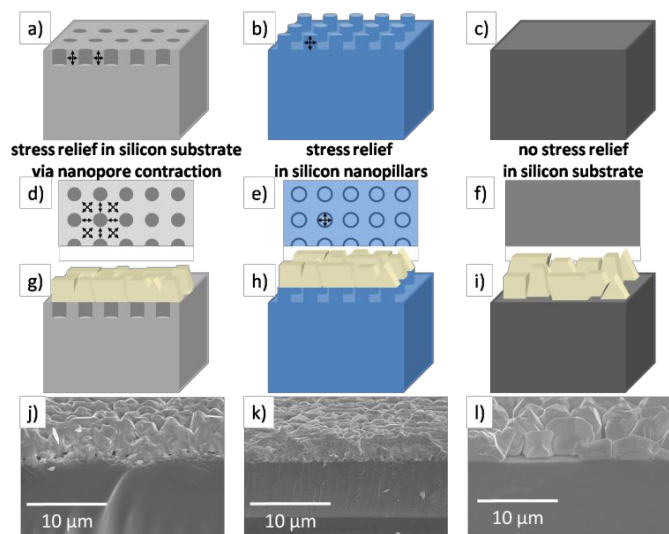


Figure 1. Comparison of Si substrates of nanopore, nanopillar, and flat morphologies: a) and d) schematics of the stress relief provided by expansion of a silicon nanopore layer (arrows denote the possibility of lattice expansion around a Si nanopore); b) and e) schematics of the stress relief provided by expansion of a silicon nanopillar layer (arrows denote the possibility of lattice expansion in a Si nanopillar); c) and f) schematics of a flat silicon substrate; InP film deposition onto a Si(100) nanopore substrate: g) schematic and j) 30° tilt scanning electron microscope (SEM) image; InP film deposition onto a Si(100) nanopillar substrate: h) schematic and k) 30° tilt SEM image; InP film deposition onto a flat Si(100) substrate shown for reference: i) schematic and l) 30° tilt SEM image.

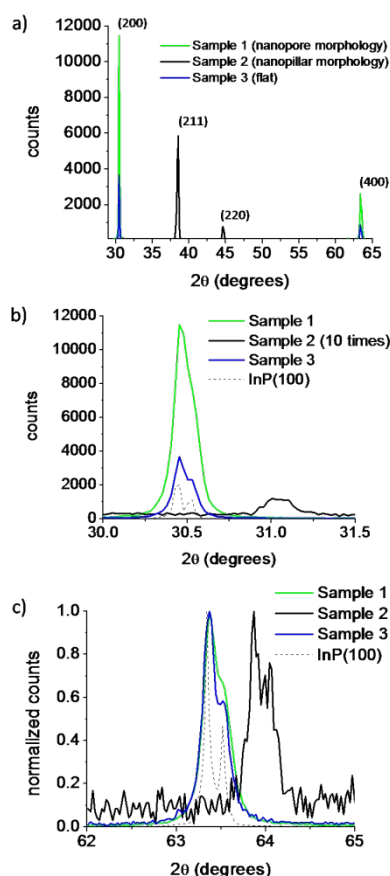


Figure 2. a) X-ray diffraction (XRD) data (with InP plane assignments for the XRD peaks) of InP films deposited onto Si(100) substrates with different nanostructured morphologies (sample 1 (1 μm spaced pores, green line), sample 2 (1 μm spaced pillars, black line), and an InP film deposited onto a flat Si(100) substrate (sample 3 (blue line)); b) XRD data in the region around the InP (200) peak at $2\theta \approx 30.5^\circ$; note the peak at $2\theta \approx 31.1^\circ$ for sample 2 (data is multiplied by 10 to highlight the small peak); c) normalized XRD data in a region around the (400) diffraction peak of InP; the InP 400 peak is at $2\theta \approx 63.3^\circ$; XRD data for an InP(100) wafer (black dashed line) are shown in b) and c) for reference.

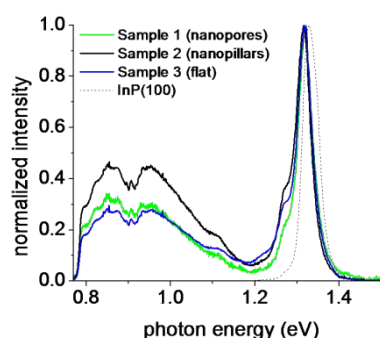
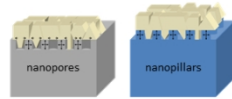


Figure 3. Comparison of photoluminescence from the InP film at room temperature on Si(100) substrates with the same Si nanostructured substrates (sample 1, green line; sample 2, black line) and the flat Si(100) substrate (sample 3, blue line) considered in Figure 2; the photoluminescence from an InP(100) wafer (black dashed line) is shown for reference.

Enhanced stress relief via nanopores



338x190mm (96 x 96 DPI)