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Fabrication of flexible high-performance organic field-effect transistors using phenacene molecules and their application toward flexible CMOS inverters

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Abstract

The transport properties of 3,10-ditetradecylpicene ($(C_{14}H_{29})_2$-picene) and [6]phenacene thin-film field-effect transistors (FETs) on Si and plastic substrates are reported, in which SiO_2 and parylene are used for gate dielectrics, respectively. These devices show p-channel normally-off FET characteristics. The μ value of 1.34 cm^2 V^{-1} s^{-1} is obtained in $(C_{14}H_{29})_2$-picene thin-film FET, where 500 μm thick polyethylene terephthalate (PET) substrate and 1 μm thick parylene are used for substrate and gate dielectric, respectively. Moreover, the excellent FET performance is obtained in $(C_{14}H_{29})_2$-picene thin-film FET using high-*k* gate dielectric, ZrO_2, which is formed on 350 μm thick PET substrate, showing p-channel normally-off FET properties and low voltage operation. The μ value reaches 6.31 cm^2 V^{-1} s^{-1} in the FET device. The FET characteristics of *N*,*N*'-dioctyl-3,4,9,10-perylenedicarboximide (PTCDIC8) thin-film FETs formed on PET are also reported, showing n-channel normally-off FET characteristics. We report the bias stress effect for flexible [6]phenacene thin film FETs which are fabricated on PEN substrate. Two types of experiments are performed for investigating bias stress effect on FET, and the bias stress effect under light irradiation is much different from that under no irradiation. This difference is well explained by the hole-filling of trap states by electron excitation. We show the characteristics of complementary MOS inverter (CMOS), constituted with [6]phenecene thin-film FET (p-channel) and PTCDIC8 thin-film FET (n-channel) formed on PET and PEN substrates, *i.e.*, flexible CMOS inverter. The maximum gain reaches 300. Furthermore, we report low-voltage operation for flexible CMOS inverter, where ZrO_2 is used as gate dielectric. Through this study, we have achieved the fabrication of flexible thin-film FETs with high μ and low voltage operation, and flexible CMOS inverters with high gain as well as low operation voltage. This study would provide the basis for the future practical / human-compatible electronic devices.

1. Introduction

In 1986, Tsumura *et al*. fabricated the first realistic field-effect transistor, FET, with organic material, polythiophene.[1] However, the field-effect mobility, μ, was ~10^{-5} cm^2 V^{-1} s^{-1}. This group fabricated the FET using polythienylenevinylene in 1993, which exhibited the μ value as high as 0.22 cm^2 V^{-1} s^{-1}.[2] Thus, the FET properties have been improved since the beginning of 1990's. Currently, the organic FET exhibiting the highest μ value is realized using a single crystal of κ-(BEDT-TTF)$_2$Cu[N(CN)$_2$]Br (BEDT-TTF: bis(ethylenedithio)tetrathiafulvalene),[3] in which μ reaches 94 cm^2 V^{-1} s^{-1}. In case of thin film, the highest μ value (= 21 cm^2 V^{-1} s^{-1}) is achieved in a 3,10-ditetradecylpicene ((C$_{14}$H$_{29}$)$_2$-picene) thin-film FET with $PbZr_{0.52}Ti_{0.48}O_3$ (PZT) gate dielectric.[4]

In addition to the organic FET, organic light emitting diodes (LEDs) and organic solar cells (or organic photovoltaic cells (OPVs)) have been fabricated using various coordination compounds and conjugated polymers.[5,6] In particular, the large area coverage may be a big advantage in their organic devices. Thus, the organic electronic devices have been expected to be a key device for future ubiquitous society, *i.e.*, organic devices should be employed for active matrix display, radio frequency identifier (RFID), electronic paper (e-paper), and diagnostic / therapeutic device.

The organic FETs have especially been studied during the past 20 years, for the ubiquitous electronics accompanying flexibility, light weight and ease of design.[7-20] The flexibility is one of the most significant benefits of organic FET. The purpose of this study is to fabricate the high-performance flexible organic FET. The high-performance means the high-speed and low-voltage operations. Recently, our group have studied the organic FETs using phenacene molecules as active layers.[20-29] The thin-film and single-crystal FETs with phenacene molecules have shown very high μ values and low-voltage

operation (~1 V). The highest μ value among phenacene thin-film FETs is now 21 cm^2 V^{-1} s^{-1} recorded for $(C_{14}H_{29})_2$-picene FET,[4] as described previously, while the highest one among phenacene single-crystal FETs is 18 cm^2 V^{-1} s^{-1} realized in [9]phenacene FET.[29]

In this study, the thin-film FETs using phenacene molecules are fully investigated to obtain the high performance, *i.e.* high μ value and low-voltage operations are pursued together with the flexibility. For this purpose, the phenacene thin-film FETs were fabricated with the high-*k* gate dielectric, ZrO_2, formed on the plastic substrates, since the phenacene molecules are well known to be excellent as active layer in the FET device.[20-29] Actually, the high μ value and stable operation are realized in the phenacene FETs fabricated on SiO_2/Si substrate owing to the suitable packing of molecules and high molecular stability. Furthermore, the high-performance logic gate circuit (inverter circuit) is fabricated on the plastic substrate. Thus, the most important purpose of this study is to provide the high-performance phenacene thin-film FET with flexibility. The properties of the FET devices and CMOS inverters fabricated in this study are clarified on the basis of their transport properties.

2. Experimental

2-1. Preliminary treatment of SiO_2 / Si and plastic substrates

The SiO_2 / Si and plastic substrates were used in this study. Before the fabrication of the FET device, the SiO_2 / Si substrate was cleaned through the following steps. (1) The substrate was washed with acetone and then with methanol under ultrasonic irradiation for each 5 min to remove organic and inorganic impurities. (2) The substrate was washed with ultra-purified water under ultrasonic irradiation for 5 min. (3) The substrate was

immersed into H_2O_2 / H_2SO_4 solution (1 : 4 in volume ratio) for 1 min to remove organic and inorganic impurities in SiO_2 layer. (4) The substrate was washed under running ultra-purified water for 5 min and stored in ultra-purified water for 10 min. (5) The substrate was finally dried by spraying nitrogen (N_2) gas. After the cleaning of the substrate, the surface of SiO_2 / Si substrate was treated with the mixed solution of hexamethyldisilazane (HMDS) and hexane (1 : 9 in volume ratio) for a half day so that it becomes hydrophobic. Subsequently, the substrate was washed with methanol and then with ultra-purified water under ultrasonic irradiation for each 5 min. The substrate was dried by spraying N_2 gas, and it was heated at 105^{o}C for 3 min.

Two types of plastic substrates, polyethylene terephthalate (PET) and polyethylene naphthalate (PEN), were used for fabricating the flexible FET. The molecular structures of PET and PEN are shown in Figure 1(a). The plastic substrates are commercially available. In this study, the above plastic substrates with different features in thickness and colour are used for the fabrication of flexible devices. The plastic substrate was washed with methanol and isopropanol under ultrasonic irradiation for each 5 min, and it was dried by spraying N_2 gas. The plastic substrate was coated with 5 nm thick chromium (Cr) and 100 nm thick gold (Au) to make the gate electrode.

2-2. Fabrication of organic thin-film FET devices and measurement of FET characteristics

Organic thin films for active layers were formed by a thermal deposition of organic molecules under vacuum of 10^{-7} Torr. Thickness of thin films was monitored by a thickness meter to make 60 nm thick thin films. The thin film was formed on each gate

dielectric. Three organic molecules were used for the active layers of the FETs; $(C_{14}H_{29})_2$-picene and [6]phenacene were used for p-channel FET, while *N*,*N*'-dioctyl-3,4,9,10-perylenedicarboximide (PTCDIC8) was used for n-channel FET. The molecular structures are shown in Figure 1(b). In addition, [6]phenacene and PTCDIC8 were used for the inverter device.

The shape of thin films was defined using metal mask. 3 nm thick 2,3,5,6-tetrafluoro-7,7,8,8-teracyano-quinodimethane (F4TCNQ) was deposited on the organic thin films, and the source and drain electrodes were formed by the thermal deposition of Au on the F4TCNQ. The F4TCNQ layer between Au source/drain electrodes and organic thin film is introduced to reduce contact resistance.

The dielectrics used in this study are SiO_2, parylene-C and ZrO_2. Commercially available SiO_2 / Si was commonly used for the FET device; thickness of SiO_2 was 400 nm. For the flexible FET device, ~1 μm thick parylene was deposited on the Au electrode on plastic substrate. The high-*k* gate dielectric, ZrO_2, was prepared on the plastic substrate by using electron-beam deposition. To avoid the leakage current, the surface of ZrO_2 was coated with 50 nm thick parylene-C, whose molecular structure is shown in Figure 1(c). The coating also led to the formation of hydrophobic surface. Through this paper, parylene-C is abbreviated 'parylene'.

All measurements were performed in a two-terminal measurement mode at room temperature using Agilent B1500A semiconductor parametric analyzer in an Ar filled glove box. The measured data were analyzed to determine the fundamental FET parameters such as μ, threshold voltage (V_{th}), on/off ratio and subthreshold swing (S) in saturation regime using the general formula:

$$I_D = \frac{\mu W C_o}{2L}(V_G - V_{th})^2 \quad (1)$$

where I_D, V_G, V_{th}, W, L and C_o refer to drain current, gate voltage, threshold voltage, channel width, channel length and capacitance per area of gate dielectric, respectively. The condition, $V_D > V_G - V_{th}$, was completely satisfied in the analysis, where V_D is drain voltage; in p-channel measurement mode, absolute values of V_D, V_G and V_{th} are employed for the analysis. Admittedly, the saturation is observed in the output characteristics of all FET devices fabricated in this study. In other words, the analysis was admittedly performed in the saturation regime. The linear part in $|I_D|^{1/2}$ *versus* $|V_G|$ is sufficiently found in all devices, so that the fitting was exactly achieved, guaranteeing the reliability of μ value evaluated in this study. Moreover, the analysis with multiple FET devices is performed to confirm the scattering of the FET properties.

3. Results and Discussion

3-1. FET properties of $(C_{14}H_{29})_2$-picene thin-film FETs with SiO_2 gate dielectric

The device structure of $(C_{14}H_{29})_2$-picene thin-film FET with SiO_2 gate dielectric is shown in Figure 2(a). Figures 3(a) and (b) show the transfer and output characteristics for $(C_{14}H_{29})_2$-picene thin-film FET formed on a SiO_2 / Si substrate; 400 nm thick SiO_2 was used as gate dielectric. The absolute drain current, $|I_D|$, increases with applying the negative gate voltage, V_G, *i.e.*, $|I_D|$ increases with increasing $|V_G|$. The drain voltage V_D was fixed at -80 V, and the drain-source voltage, V_{DS} (= V_D – V_S), was -80 V because the source voltage, V_S, was 0 V (source electrode was grounded). This transfer curve shows p-channel operation, because negative V_G was applied for the increase in $|I_D|$. The output

characteristics, $|I_D|$ - $|V_D|$ plot, at different negative V_G values exhibited typical normally-off properties. Thus, the $(C_{14}H_{29})_2$-picene thin-film FET provides the p-channel normally-off FET properties. The values of μ, $|V_{th}|$, on/off ratio and S were determined to be 3.4 $cm^2\ V^{-1}\ s^{-1}$, 4.8×10^1 V, 8.7×10^5 and 7.0 V $decade^{-1}$, respectively. In addition, the capacitance per area, C_o, for 400 nm thick SiO_2 was 8.34 nF cm^{-2}, which was determined from the extrapolation of C_o recorded at 20 – 1000 Hz to 0 Hz.

3-2. Fabrication and characterizations of flexible $(C_{14}H_{29})_2$-picene thin-film FETs with parylene gate dielectric formed on two types of plastic substrates

The characteristics of $(C_{14}H_{29})_2$-picene thin-film FETs formed on plastic substrates are fully described. The device structure of $(C_{14}H_{29})_2$-picene thin-film FET is shown in Figure 2(b). 500 μm and 125 μm thick PET substrates were used for the device. 1.0 μm thick parylene was used for the gate dielectric. Figures 3(c) and (d) show the transfer and output characteristics for $(C_{14}H_{29})_2$-picene thin-film FET formed on 500 μm PET substrate. The absolute drain current, $|I_D|$, increases with applying the negative gate voltage V_G, *i.e.*, $|I_D|$ increases with increasing $|V_G|$, in which the drain voltage V_D was fixed at -100 V, i.e., the V_{DS} was -100 V. This transfer characteristic implies p-channel operation. The output characteristics, $|I_D|$ - $|V_D|$ plots, at different negative V_G values exhibited typical normally-off properties. Thus, the $(C_{14}H_{29})_2$-picene thin-film FET formed on 500 μm thick PET substrate provides the p-channel normally-off FET properties. The FET parameters, μ, $|V_{th}|$, on/off ratio and S, obtained from nine $(C_{14}H_{29})_2$-picene thin-film FET devices are listed in Table S1. As seen from Table S1, the channel length, L, is changed from 50 to 285 μm, while the channel width, W, is fixed to 500 μm;

all parameters of the flexible FET devices fabricated in this study are listed in Tables S1 – S9 in Supplementary Information.

As seen from Table S1, the highest μ value was 1.34 $cm^2 V^{-1} s^{-1}$ among the $(C_{14}H_{29})_2$-picene thin-film FET devices with parylene gate dielectric fabricated on 500 mm thick PET. The average values of μ, $|V_{th}|$, on/off ratio and S obtained from nine devices were $7(4) \times 10^{-1}$ $cm^2 V^{-1} s^{-1}$, $6.0(2) \times 10^1$ V, $5(2) \times 10^6$ and 5(2) V $decade^{-1}$, respectively. The averaged FET parameters of this device are listed in Table 1. The μ is relatively high, but the $|V_{th}|$ is too high to be used for practical device. In addition, the capacitance per area, C_o, for 1 μm thick parylene was 2.98 nF cm^{-2}, which was determined from the extrapolation of C_o recorded at 20 – 1000 Hz to 0 Hz.

The μ was plotted against L (Figure 4) which shows a linear relationship between μ and L. Namely, the μ increases with increasing L, indicating that the contact resistance affects the μ value because the channel mobility must be constant in principle. In other words, the μ obtained from the FET device with larger L is affected by less contact resistance. Thus, the reliable μ value of channel region should be obtained from the FET device with large L. The highest μ (= 1.34 $cm^2 V^{-1} s^{-1}$) was recorded in the FET device with L of 285 μm. The above characteristic behaviour is generally observed in the various FET devices[30,31], and it is called 'short channel effect'. Namely, in case of short channel (small L) in which channel conductance is very large, the I_D is dominated by carrier injection efficiency (contact resistance), while in case of long channel (large L) in which channel conductance is small, the I_D is governed by the accumulated carriers in the channel region. As a consequence, the μ value for the FET device with large L may be exactly evaluated in terms of formula (1), indicating that the high μ value obtained for

the FET with large L is substantially reliable. In addition, the μ must become constant with further increasing L, because the μ is intrinsically independent of L.

The transfer and output characteristics for $(C_{14}H_{29})_2$-picene thin-film FET formed on 125 μm thick PET substrate were fully investigated; 1 μm thick parylene was used for gate dielectric. This transfer and output characteristics showed p-channel operation since the negative V_G was applied (not shown). The μ, $|V_{th}|$, on/off ratio and S, obtained from nine $(C_{14}H_{29})_2$-picene thin-film FET devices formed on the PET substrate are listed in Table S2. As seen from Table S2, the L is changed from 135 to 600 μm, while the W is fixed to 500 μm. The highest μ value was 7.01 $\times 10^{-1}$ cm^2 V^{-1} s^{-1} for the FET with L = 600 μm. The average values of μ, $|V_{th}|$, on/off ratio and S obtained from nine devices were 3(2) $\times$ 10^{-1} cm^2 V^{-1} s^{-1}, 6.3(1) $\times$ 10^1 V, 1.1(2) $\times$ 10^6 and 6(1) V decade^{-1}, respectively, which are listed in Table 1. The value of C_o used to determine the μ value was 2.76 nF cm^{-2}.

Thus, the $(C_{14}H_{29})_2$-picene thin-film FET formed on different PET substrates showed the p-channel normally-off FET characteristics, and the μ value of more than 1 cm^2 V^{-1} s^{-1} was recorded. This implies that $(C_{14}H_{29})_2$-picene is available for the flexible FET device. Furthermore, it was found that the μ value is largely affected by contact resistance (or carrier injection) in two-terminal measurement mode, and the L should be extended. We must reduce the operation voltage of the $(C_{14}H_{29})_2$-picene thin-film FET because of their high $|V_{th}|$. For this purpose, the high-k gate dielectric, ZrO_2, will be used in section 3-4.

3-3. Fabrication and characterizations of flexible [6]phenacene thin-film FETs with parylene gate dielectric formed on plastic substrates

The device of [6]phenacene thin-film FET was fabricated, as shown in Figure 2(b). 125 μm thick PET substrate, and 350 and 500 μm thick PET substrates were used for the FET devices. Furthermore, ~1 μm thick parylene was used for the gate dielectric. Figures 5(a) and (b) show the transfer and output characteristics for [6]phenacene thin-film FET formed on 125 μm thick PET. The $|I_D|$ increases with applying the negative V_G, *i.e.*, $|I_D|$ increases with increasing $|V_G|$, in which the V_D was fixed at -120 V. The V_{DS} was -120 V. This transfer curve implies p-channel operation. The $|I_D|$ - $|V_D|$ plots at different negative V_G values exhibited typical normally-off properties. Thus, the [6]phenacene thin-film FET formed on 125 μm thick PET substrate provides the p-channel normally-off FET properties. The values of μ, $|V_{th}|$, on/off ratio and S obtained from four [6]phenacene thin-film FET devices are listed in Table S5.

As seen from Table S5, the value of L was changed between 350 and 450 μm, while the W varied between 500 and 1000 μm. The highest μ value (= 2.1 × 10^{-1} cm^2 V^{-1} s^{-1}) was recorded in the FET device with the L of 350 μm and W of 500 μm. Exactly saying, the μ value was almost the same among four devices. The average values of μ, $|V_{th}|$, on/off ratio and S obtained from four devices were 1.9(2) × 10^{-1} cm^2 V^{-1} s^{-1}, 6.0(1) × 10^1 V, 1(1) × 10^6 and 3(2) V $decade^{-1}$, respectively; the values are listed in Table 1. Here, the C_o of 2.53 nF cm^{-2} were used to determine the μ value.

The transfer and output characteristics for [6]phenacene thin-film FET formed on 350 μm thick PET and 500 μm thick PET substrates were investigated, and the $|I_D|$

increases with applying the negative gate voltage V_G (not shown). These transfer characteristics imply p-channel operation. The output characteristics, $|I_D|$ - $|V_D|$ plots, at different negative V_G values exhibited typical normally-off properties. The FET parameters, μ, $|V_{th}|$, on/off ratio and S, obtained from multiple [6]phenacene thin-film FET devices fabricated on 350 μm thick PET and 500 μm thick PET substrates are listed in Tables S6 and S7, respectively. As seen from Table 1, the average values of μ, $|V_{th}|$, on/off ratio and S for [6]phenacene thin-film FET fabricated on 350 μm thick PET were 1.6(7) × 10^{-1} cm^2 V^{-1} s^{-1}, 5.6(2) × 10^1 V, 1(1)× 10^5 and 5(2) V $decade^{-1}$, respectively, while the average values of μ, $|V_{th}|$, on/off ratio and S for [6]phenacene thin-film FET fabricated on 500 μm thick PET were 1.6(7) ×10^{-1} cm^2 V^{-1} s^{-1}, 6.0(2) × 10^1 V, 1.3(8)× 10^5 and 6.4(5) V $decade^{-1}$, respectively. The C_o used to determine the μ value was 2.48 nF cm^{-2} and 2.74 nF cm^{-2}, respectively, for the former and latter FETs devices. Thus, the FET parameters were almost the same as each other, even if the thickness of PET substrate was changed. In this study, the first step was accomplished for the development of flexible FET device towards a practical application. However, the μ value was still in the order of 10^{-1} cm^2 V^{-1} s^{-1}, and the operation voltage was more than 50 V. For the next step, we fabricated the $(C_{14}H_{29})_2$-picene thin-film FETs with high-*k* gate dielectric, and pursued the higher μ and lower operation voltage.

3-4. Fabrication and characterizations of flexible $(C_{14}H_{29})_2$-picene thin-film FETs with high-*k* gate dielectrics for low-voltage operation

Typical device structure is shown in Figure 2(b). Figures 5(c) and 5(d) show the transfer and output characteristics for $(C_{14}H_{29})_2$-picene thin-film FET formed on 125 μm thick PET substrate; 150 nm thick ZrO_2 layer was formed on the PET substrate. The

surface of ZrO_2 layer was covered with 50 nm thick parylene to produce the hydrophobic surface and the protection of leakage current. The $|I_D|$ increases with applying the negative gate voltage V_G, *i.e.*, $|I_D|$ increases with increasing $|V_G|$, in which the V_D was fixed at -16 V (V_{DS} = -16 V). The transfer curve implies typical p-channel operation. The $|I_D|$ - $|V_D|$ plots at different negative V_G values exhibited typical normally-off properties. Thus, the $(C_{14}H_{29})_2$-picene thin-film FET with 150 nm thick ZrO_2 gate dielectric formed on 125 μm thick thick PET substrate provides the p-channel normally-off FET properties. The values of μ, $|V_{th}|$, on/off ratio and S obtained from four $(C_{14}H_{29})_2$-picene thin-film FET devices are listed in Table S3.

The average values of μ, $|V_{th}|$, on/off ratio, and S obtained from four devices were 2(2) $cm^2 V^{-1} s^{-1}$, 8(1) V, 9(6) $\times$ 10^4 and 1.32(6) V $decade^{-1}$, respectively, which are listed in Table1. The μ value is higher than those in $(C_{14}H_{29})_2$-picene thin-film FET with parylene gate dielectric described in section 3-2. Moreover, the $|V_{th}|$ is quite small, indicating high-performance / low-voltage operation. In addition, the capacitance per area, C_o, for the dielectric was 31 nF cm^{-2}, which was determined from the extrapolation of C_o recorded at 20 – 1000 Hz to 0 Hz.

The transfer and output characteristics for $(C_{14}H_{29})_2$-picene thin-film FET formed on 350 μm PET substrate showed p-channel normally-off operation (not shown) . The values of μ, $|V_{th}|$, on/off ratio, and S obtained from seven $(C_{14}H_{29})_2$-picene thin-film FET devices are listed in Table S4. The average values of μ, $|V_{th}|$ on/off ratio and S obtained from seven devices were 3(2) $cm^2 V^{-1} s^{-1}$, 6.4(7) V, 2(4) $\times$ 10^7 and 1.0(1) V $decade^{-1}$, respectively, which are listed in Table 1. As a consequence, the μ value is high, and the $|V_{th}|$ is quite small, indicating the high performance / low-voltage operation. The C_o was 31 nF cm^{-2}, which was determined from the extrapolation of C_o recorded at 20 – 1000 Hz to 0 Hz.

Thus, the $(C_{14}H_{29})_2$-picene thin-film FET device formed on ZrO_2 / PET substrate showed excellent FET properties, demonstrating that $(C_{14}H_{29})_2$-picene is a promising material for flexible FET. Thus, the high μ value and low voltage operation was achieved in the flexible organic thin-film FET.

3-5. Fabrication and characterizations of flexible PTCDIC8 FETs

For the fabrication of n-channel flexible FET, the PTCDIC8 was used for active layer of FET device. The device structure of PTCDIC8 thin-film FET is shown in Figure 2(b). 125 and 500 μm thick PET substrates were used for the devices. ~1 μm parylene was used for the gate dielectric. Figures 6(a) and (b) show the transfer and output characteristics for PTCDIC8 thin-film FET formed on 125 μm thick PET substrate. The I_D increases with applying the positive gate voltage V_G in which the V_D was fixed at 100 V. The V_{DS} was 100 V. This behaviour implies n-channel operation. The $I_D - V_D$ plots at different V_G exhibited typical normally-off properties. Thus, the PTCDIC8 thin-film FET formed on 125 μm thick PET substrate provides the n-channel normally-off FET properties. The values of μ, $|V_{th}|$, on/off ratio, and S obtained from six PTCDIC8 thin-film FET devices are listed in Table S8. The highest μ value was 7.56×10^{-2} cm^2 V^{-1} s^{-1}. The average values of μ, $|V_{th}|$, on/off ratio and S were $4(2) \times 10^{-2}$ cm^2 V^{-1} s^{-1}, $6.5(6) \times 10^1$ V, $4(2) \times 10^3$ and $1.4(3) \times 10^1$ V $decade^{-1}$, respectively, which are listed in Table 1. The C_o for 1 μm thick parylene was 2.62 nF cm^{-2}, which was determined from the extrapolation of C_o recorded at 20 – 1000 Hz to 0 Hz. This C_o was used for the determination of μ value. Here, in order to evaluate the L dependence of μ, the μ value was plotted against L (not

shown), showing a linear relationship. This behaviour also implies that the contact resistance affects the μ value even in n-channel organic FET.

The PTCDIC8 thin-film FET formed on 500 μm thick PET substrate also showed n-channel operation. The output characteristics, I_D - V_D plots, at different V_G values exhibited typical normally-off properties (not shown). Thus, the PTCDIC8 thin-film FET formed on 500 μm thick PET substrate provides the n-channel normally-off FET properties. The values of μ, V_{th}, on/off ratio and S obtained from six PTCDIC8 thin-film FET devices are listed in Table S9. The average values of μ, V_{th}, on/off ratio, and S obtained from nine devices were 1.4(4) $\times$ 10^{-1} cm^2 V^{-1} s^{-1}, 5.9(6) $\times$ 10^1 V, 7(2) $\times$ 10^3 and 1.6(1) $\times$ 10^1 V $decade^{-1}$, respectively, which are listed in Table S9. The averaged μ was higher than that, 4(2) $\times$ 10^{-2} cm^2 V^{-1} s^{-1}, of FET with 125 μm thick PET, probably because of utilizing the hard PET. In addition, the C_o for 1 μm thick parylene was 2.60 nF cm^{-2}. Thus, the n-channel flexible organic FET showing relatively high performance was successfully fabricated in this study.

3-6. Bias stress effect on FET devices

The results of bias stress effect for [6]phenacene thin-film FET fabricated on 125 μm thick PEN substrate are reported, in which 150 nm thick ZrO_2 was gate dielectric. The device structure is shown in Figure 2(b); the L and W of FET device are 200 and 500 μm, respectively. In the study of the bias stress effect, we used 125 μm thick PEN substrate instead of PET, but the FET performance is the same as the case of PET substrate. Therefore, the results obtained in this study will also be applied for the [6]phenacene thin-film FET fabricated on PET substrate.

The transfer curves of the FET device were repeatedly measured for ~51.5 h. The time required for one measurement (forward and reverse measurements) was 17 min. 180 measurements were performed within ~51.5 h. The V_G is varied from 0 to -16 V (forward transfer curve) and -16 to 0 V (reverse transfer curve) in one measurement. The V_D was fixed at -16 V. Figures 7(a) and (b) refer to transfer curves recorded at the 1st and the 180th measurements, respectively. Both show typical normally-off properties. The $|I_D|$ at $|V_G| = 16$ V in the transfer curve at 180th measurement does not vary in comparison with that at 1st measurement, and the transfer curve has no significant hysteresis. Here it should be noticed that the measurements of transfer curve were performed under either light irradiation of fluorescent lamp (light-on) or no light irradiation (light-off), as shown in Figure 7(c) and (d).

As seen from Figure 7(c), the μ value gradually decreases with repetition number of measurement, n, under light-off. Strictly speaking, the μ increases rapidly at only n = 1 – 7, and then decreases slowly at n = 8 – 20 (light-on). The μ value discontinuously drops when the fluorescent lamp was switched-off at n = 21, and then it straightforwardly decreases with n. When the light is switched-on, the μ rapidly jumps. After re-switching-off the fluorescent lamp, the μ discontinuously drops at n = 85. These results show that μ value gradually decreases with increasing n under light-off, and it rapidly increases by light irradiation, indicating the effect of light-driven μ enhancement. In addition, the μ value was almost constant or increases during the continuous light irradiation, but the jump of μ by light-on was almost constant through the repletion of light-on and light-off. Consequently, the μ clearly decreases with increasing n under no light, indicating the presence of bias stress effect.

As seen from Figure 7(d), the $|V_{th}|$ increases with n, the $|V_{th}|$ is smaller under light than under no light. Namely, the rapid jump of $|V_{th}|$ was observed when switching-off the light, suggesting that the light from fluorescent lamp tends to fill the trap states with hole which are formed in channel region. This should lead to the reduction of $|V_{th}|$. Moreover, the effect of light-driven μ enhancement (Figure 7(c)) may be due to the hole-filling of trap states. In this FET, the channel transport is made by hole. Therefore, the trapping states must be electron occupied states. The light irradiation must excite electrons from the trap states near HOMO level to those with higher energy (or far from HOMO level), which will form electron-unoccupied trap states near HOMO level (or hole-occupied trap states). This should lead to the smooth hole transport (or higher μ) and the lowering of $|V_{th}|$, because of the reduction of trap states which can capture holes. Therefore, the enhancement of μ and lowering of $|V_{th}|$ induced by light can be reasonably understood by light-driven hole-filling of trap states (or electron excitation from trap states). This scenario is schematically depicted in Figure 8.

To pursue the bias stress effect more deeply, we carried out different type of FET measurement using the same FET device as that used for bias-stress investigation described above. Namely, FET device was maintained at V_G = -16 V and V_D = -16 V for 1 h, and then the forward transfer curve was measured by changing V_G from 0 to -16 V, where V_D = -16 V. The time required for the transfer curve measurement was 8 min. The bias voltage application for 1 h (V_G = -16 V and V_D = -16 V) and measurement of forward transfer curve for 8 min were repeated by 22 cycles (n = 22); once V_G reached -16 V in the transfer curve measurement, it was maintained at V_G = -16 V and V_D = -16 V for 1 h as the next cycle. Figures S1(a) and (b) in the Supplementary Information refer to forward transfer curves recorded at the 1st and the 22nd measurements. Both shows the typical

normally-off properties. As seen from Figure S1(c), the value of μ decreases with n, and it jumped in irradiation of light from fluorescent lamp at n = 14; the lamp was switched-on at n = 1 - 3, switched-off at n = 4 -13, and switched-on at n = 14 - 22. The μ - n plot clearly shows light-driven μ enhancement. The bias stress reduces the μ value both with and without light. The slope of decrease in μ is almost the same between with and without light. As seen from Figure S1(d), the $|V_{th}|$ rapidly jumped when switching-off the light, consistent with Figure 7(d), and the $|V_{th}|$ was almost constant under light.

As seen from Figures 7(c) and S1(c), the μ decreases with applying V_G and V_D for long time although the way of bias voltage application is different between Figures 7(d) and S1(c). The constant V_D was applied for 17 min and the V_G was varied from 0 to -16 V for 17 min in Figure 7(c), while the constant V_D and V_G were applied for 1 h, and the V_G was varied from 0 to -16 V for 8 min in Figure S1(c). We can stress that the bias voltage application at least degrades the μ value.

The bias stress effect is generally related to the emergence of trap states (or traps) closely associated with the presence of H_2O.[32-37] Furthermore, it was found that the bias stress effect decreased when the interval without bias voltage is present between transfer curve measurements. The interval of 1 h provided no bias stress effect in the FET operation of [6]phenacene and [7]phenacene single-crystal FETs. Moreover, we must stress that the H_2O plays an important role for bias stress effect.[21,23] The parylene coating of ZrO_2 gate dielectric is of importance for lowering the bias stress effect. Actually, the bias stress effect found in this study is much smaller than those for phenacene thin-film FETs with HMDS-coated SiO_2 gate dielectric.[21,23] The small hysteresis observed in the transfer curves shown in Figures 7(a) and (b) also suggests the small bias stress; when the larger the bias stress is observed, the larger hysteresis is in the transfer curve. The

presence of H_2O-related trap states (density of 2×10^{12} cm^{-2}) is confirmed in the pentacene thin-film FET, which are observed at 430 meV above valence band.[32-37] To sum up, the bias stress effect observed in the [6]phenacene thin-film FET with ZrO_2 gate dielectric used in this study is small because of the formation of hydrophobic surface of ZrO_2 with parylene, but the H_2O related trap states formed by bias application must be present at the channel region.

3-7. Fabrication and operation properties of flexible CMOS inverters

Inverter (NOT circuit) is one of the fundamental building blocks in digital circuits. The equivalent circuit of CMOS inverter is shown in Figure 9(a). The CMOS inverter is constituted of p-channel and n-channel FETs. The fundamental operation properties are as follows: (1) When input voltage V_{in} is lower than threshold value, V_{TC}, the output voltage V_{out} becomes the same as the supplied voltage V_{DD}. (2) When V_{in} is higher than V_{TC}, the V_{out} becomes 0 [6]. Namely, at low V_{in} p-channel FET operates and n-channel does not, while at high V_{in} n-channel FET operates and p-channel does not. The ideal V_{out} - V_{in} curve is shown in Figure 9(a). The gain is defined as $\left|\frac{dV_{out}}{dV_{in}}\right|_{V_{in}=V_{TC}}$.

We fabricated the CMOS inverter which is composed of [6]phenacene thin-film FET as p-channel FET and PTCDIC8 thin-film FET as n-channel. The CMOS inverter was fabricated on plastic substrate. The device structure is shown in Figure 9(b). The inverter was fabricated according to the following process: (1) 100 nm thick Au gate electrode was formed on 350 μm thick PET substrate covered with 5 nm thick Cr. (2) 1 μm thick parylene film was formed as gate dielectric on Au/Cr/PET substrate. (3) 60 nm thick [6]phenacene and PTCDIC8 thin films were formed to produce the active layers. (4) 50

nm thick Au source and drain electrodes were finally formed as shown in Figure 9(b), and 3 nm thick F4TCNQ film was deposited between the Au electrodes and organic thin films. Therefore, p-channel and n-channel FETs are connected by Au electrode, where V_{out} is measured. The V_{in} is applied to the gate electrode.

Figures 9(c) and (d) show the transfer curves for [6]phenacene and PTCDIC8 thin-film FETs which constitute the CMOS inverter. The L and W were 100 and 500 μm, respectively. In this CMOS inverter device, 350 μm thick PET was employed as plastic substrate. The former shows p-channel FET characteristcs, while the latter shows n-channel FET characteristics. The V_D was fixed at -120 V. Figure 9(e) shows V_{out} - V_{in} and gain – V_{in} plots at different V_{DD}'s from 40 to 120 V. The maximum gain reaches more than 250. The V_{TC} was almost a half of the applied V_{DD} except for V_{DD} = 40 V. Thus, the high-performance CMOS inverter circuit was successfully fabricated using thin films of [6]phenacene and PTCDIC8.

Moreover, we fabricated the CMOS inverters with same structure on 125 μm thick PEN and 125 μm thick PET substrates. The V_{out} - V_{in} and gain - V_{in} plots for the inverter on PEN are shown in Figure S2(a). The V_{TC} is smaller than a half of V_{DD}, indicating an unbalanced inverter property. However, the maximum gain reached ~300. The similar behavior is observed in the V_{out} - V_{in} plots for the inverter formed on 125 μm thick PET substrate (not shown), which shows the gain as high as ~300. Thus, the maximum gain was ~300. Consequently, the flexible CMOS inverter was successfully fabricated.

Figures S2(b) and (c) show the transfer curves of [6]phenacene and PTCDIC8 thin-film FETs, respectively, in the inverter device formed on parylene/ZrO_2/Au/PEN substrate where 125 μm thick PEN was used. The structure of inverter is the same as that

shown in Figure 9(b), but 150 nm thick ZrO_2 was used as gate dielectric instead of 1 μm thick parylene gate dielectric. These show low-voltage normally-off behaviour. Figure S2(d) shows the plots of V_{out} - V_{in} and gain - V_{in} in the inverter; the applied voltage V_{DD} was 12 or 16 V. The V_{TC} was exactly a half of V_{DD}. The maximum gain reached more than 70. Thus, the flexible/low-voltage operated inverter was successfully fabricated using ZrO_2 gate dielectric formed on PEN substrate.

Finally, the stress effect on CMOS inverter was investigated by repeating the measurements of inverter properties. The inverter device used in this study is the same structure as that shown in Figure 9(b). This device was fabricated on 125 μm thick PEN substrate, and the gate dielectric was 150 nm thick ZrO_2. Figure 10 show the plots of V_{out} - V_{in} and gain – V_{in} in [6]phenacene / PTCDIC8 CMOS inverter formed on 125 μm thick PEN at 1st measurement (Figure 10(a)) and 100th measurement (Figure 10(b)); the applied voltage V_{DD} was 16 V. The V_{TC} values were almost a half of V_{DD}, as seen from V_{out} - V_{in} plots in both measurements. The maximum gain reached more than 20. The variation of the gain and V_{TC} is negligible between n = 1 and 100, indicating that this inverter operates stably even after 100 cycle repeated measurements. Figures 10(c) and 10(d) show the gain and V_{TC} as a function of n (= 1 - 100). These values refer to those obtained from the forward measurements. As seen from Figures 10(c) and (d), the gain does not change with n, while V_{TC} changes with n and it approaches a half of V_{DD} (= 16 V). Namely, the properties become ideal by repeating the measurements. Also we fabricated the [6]phenacene / PTCDIC8 CMOS inverter formed on 125 μm thick PET using ZrO_2 gate dielectric. All behaviors (V_{out} - $V_{in,}$ gain-$V_{in,}$ gain – n and V_{TC} –n) are almost the same as those shown in in Figure 10.

4. Conclusions

The organic FET has promising applications toward human-compatible devices such as electronic skin and biomedical sensor as well as ubiquitous devices such as flexible display, electronic paper and information tag. However, there are still many problems to be solved for future practical application, *i.e.*, the μ value, operation voltage, durability and stability are inferior to those of inorganic MOS FET. Furthermore, the advantages in organic FET such as flexibility and ease of design must be further advanced. In this study, the high-performance in organic FET has been pursued, *i.e.*, high μ value and low-voltage operations are pursued together with flexibility. For this purpose, the phenacene thin-film FETs have been fabricated with the high-*k* gate dielectric formed on the plastic substrates. The high-performance inverter circuit has also been fabricated on the plastic substrate.

The results achieved in this study are as follows. (1) The high-performance $(C_{14}H_{29})_2$-picene thin-film FET was fabricated with SiO_2 gate dielectric on Si substrate. The μ reached 3.4 $cm^2\ V^{-1}\ s^{-1}$, showing that $(C_{14}H_{29})_2$-picene is promising for FET device. (2) The $(C_{14}H_{29})_2$-picene thin-film FET was fabricated with parylene gate dielectric on various plastic substrates. The highest μ was 1.34 $cm^2\ V^{-1}\ s^{-1}$ (Table S1), and the averaged μ also reached $7(4) \times 10^{-1}\ cm^2\ V^{-1}\ s^{-1}$ (Table 1). (3) The [6]phenacene thin-film FET was fabricated with parylene gate dielectric on various plastic substrates. The highest μ was $2.23 \times 10^{-1}\ cm^2\ V^{-1}\ s^{-1}$ (Table S6), and the averaged μ also reached $1.9(2) \times 10^{-1}\ cm^2\ V^{-1}\ s^{-1}$ for [6]phenacene thin-film FET fabricated on 125 μm thick PET (Table 1) and $1.6(7) \times 10^{-1}\ cm^2\ V^{-1}\ s^{-1}$ for that on 350 μm thick PET (Table 1). (4) The $(C_{14}H_{29})_2$-picene thin-film FET was fabricated with ZrO_2 gate dielectric on various plastic substrates. The highest μ was 6.31 $cm^2\ V^{-1}\ s^{-1}$ (Table S4), and the

averaged μ also reached 3(2) $cm^2 V^{-1} s^{-1}$ (Table 1). Thus, the excellent flexible thin-film FET was fabricated using $(C_{14}H_{29})_2$-picene. (5) The PTCDIC8 thin-film FET was fabricated with parylene gate dielectric on various plastic substrates, indicating the realization of n-channel flexible organic FET. The highest μ was 1.82×10^{-1} $cm^2 V^{-1} s^{-1}$ (Table S9), and the averaged μ also reached $1.4(4) \times 10^{-1}$ $cm^2 V^{-1} s^{-1}$ (Table 1). (6) The bias stress effect on FET performance was investigated by repeating measurement of FET characteristics under light and no light. Under light, the FET performance is higher than that under no light. This was well explained based on the hole-filling of trap states by electron photoexcitation. The bias stress may relate to the presence of a trace of H_2O at channel region. (7) The flexible CMOS inverter was fabricated using [6]phenacene and PTCDIC8 thin-film FETs on plastic substrates. The highest gain reached 300. Also the flexible inverter with low voltage operation was fabricated using ZrO_2 / plastic substrates. The bias stress effect on inverter properties was fully investigated.

In addition, the bending effect of the flexible FET device must be examined for its practical application, *i.e.*, the high-performance operation of bent FET device is indispensable for making use of the merits of flexible FET device. In this study, the bending effect of phenacene flexible thin-film FET has not been performed, and it would be the future task. Through this study, we successfully achieved to fabricate flexible thin-film FETs showing high μ and low voltage operation, and flexible CMOS inverters with high gain and ideal V_{TC} as well as low operation voltage. This study would provide the basis for the future practical / human-compatible electronic devices.

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Table 1. Averaged FET parameters of organic thin-film FETs with various gate dielectrics formed on plastic substrates.

Active layer	Substrate (thickness)	Gate dielectric	$< \mu >$ ($cm^2 V^{-1} s^{-1}$)	$< \lvert V_{th} \rvert >$ (V)	$< ON/OFF >$	$< S >$ (V decade^{-1})	
$(C_{14}H_{29})_2$-picene	PET (500μm)	parylene	$7(4) \times 10^{-1}$	60(2)	$5(2) \times 10^{6}$	5(2)	(a)
	PET (125μm)	parylene	$3(2) \times 10^{-1}$	63(1)	$1.1(2) \times 10^{6}$	6(1)	(b)
	PET (125μm)	ZrO_2	2(2)	8(1)	$9(6) \times 10^{4}$	1.32(6)	(c)
	PET (350μm)	ZrO_2	3(2)	6.4(7)	$2(4) \times 10^{7}$	1.0(1)	(d)
[6]phenacene	PET (125μm)	parylene	$1.9(2) \times 10^{-1}$	60(1)	$1(1) \times 10^{6}$	3(2)	(e)
	PET (350μm)	parylene	$1.6(7) \times 10^{-1}$	56(2)	$1(1) \times 10^{5}$	5(2)	(f)
	PET (500μm)	parylene	$1.6(7) \times 10^{-1}$	60(2)	$1.3(8) \times 10^{5}$	6.4(5)	(g)
PTCDIC8	PET (125μm)	parylene	$4(2) \times 10^{-2}$	65(6)	$4(2) \times 10^{3}$	14(3)	(h)
	PET (500μm)	parylene	$1.4(4) \times 10^{-1}$	59(6)	$7(2) \times 10^{3}$	16(1)	(i)

Detailed information and the FET parameters in the devices ((a) – (i)) of this table are shown in Tables S1 – S9 of Supplementary Information, respectively. The values listed in (a) – (i) of this table correspond to the averaged values listed in Tables S1 – S9.

Figure caption

Figure 1. Molecular structures of (a) PET and PEN, (b) $(C_{14}H_{29})_2$-picene, [6]phenacene and PTCDIC8, and (c) parylene-C.

Figure 2. Device structures of (a) $(C_{14}H_{29})_2$-picene thin-film FET with SiO_2 gate dielectric and (b) flexible organic thin-film FET on fabricated on PET. D, S and G refer to electrodes of drain, source and gate, respectively.

Figure 3. (a) Transfer curve and (b) output curve in $(C_{14}H_{29})_2$-picene thin-film FET with SiO_2 gate dielectric. (c) Transfer curve and (d) output curve in $(C_{14}H_{29})_2$-picene thin-film FET with parylene gate dielectric formed on 500 μm thick PET.

Figure 4. $\mu - L$ plot in $(C_{14}H_{29})_2$-picene thin-film FET with parylene gate dielectric formed on 500 μm thick PET.

Figure 5. (a) Transfer curve and (b) output curve in [6]phenacene thin-film FET with parylene gate dielectric formed on 125 μm thick PET. (c) Transfer curve and (d) output curve in $(C_{14}H_{29})_2$-picene thin-film FET with ZrO_2 gate dielectric formed on 125 μm thick PET.

Figure 6. (a) Transfer curve and (b) output curve in PTCDIC8 thin-film FET with parylene gate dielectric formed on 125 μm thick PET.

Figure 7. (a) Transfer curve in 1st measurement, (b) transfer curve in 180th measurement, (c) μ – n plot and (d) $|V_{th}|$ - n plot in [6]phenacene thin-film FET with ZrO_2 gate dielectric formed on 125 μm thick PEN.

Figure 8. Schematic representation of light-driven hole-filling of trap states.

Figure 9. (a) Equivalent circuit and ideal $V_{out} - V_{in}$ plot in CMOS inverter. (b) Device structure of [6]phenacene / PTCDIC8 CMOS inverter formed on 350 μm thick PET; parylene was used for gate dielectric. Transfer curves of (c) [6]phenacene

thin-film FET and (d) PTCDIC8 thin-film FET which constitute the CMOS inverter. (e) Plots of V_{out} – V_{in} and gain – V_{in} in [6]phenacene / PTCDIC8 CMOS inverter formed on 350 μm thick PET. Both forward and reverse V_{out} – V_{in} curves are drawn in (e), while only a forward gain – V_{in} curve is shown.

Figure 10. Plots of V_{out} – V_{in} and gain – V_{in} in (a) 1st measurement and (b) 100th measurement for [6]phenacene / PTCDIC8 CMOS inverter formed on 125 μm thick PEN. ZrO_2 was used for gate dielectric. The blue and red curves refer to the forward and reverse plots, respectively. Plots of (c) gain – n and (d) V_{TC} – n in [6]phenacene / PTCDIC8 CMOS inverter formed on 125 μm thick PEN.

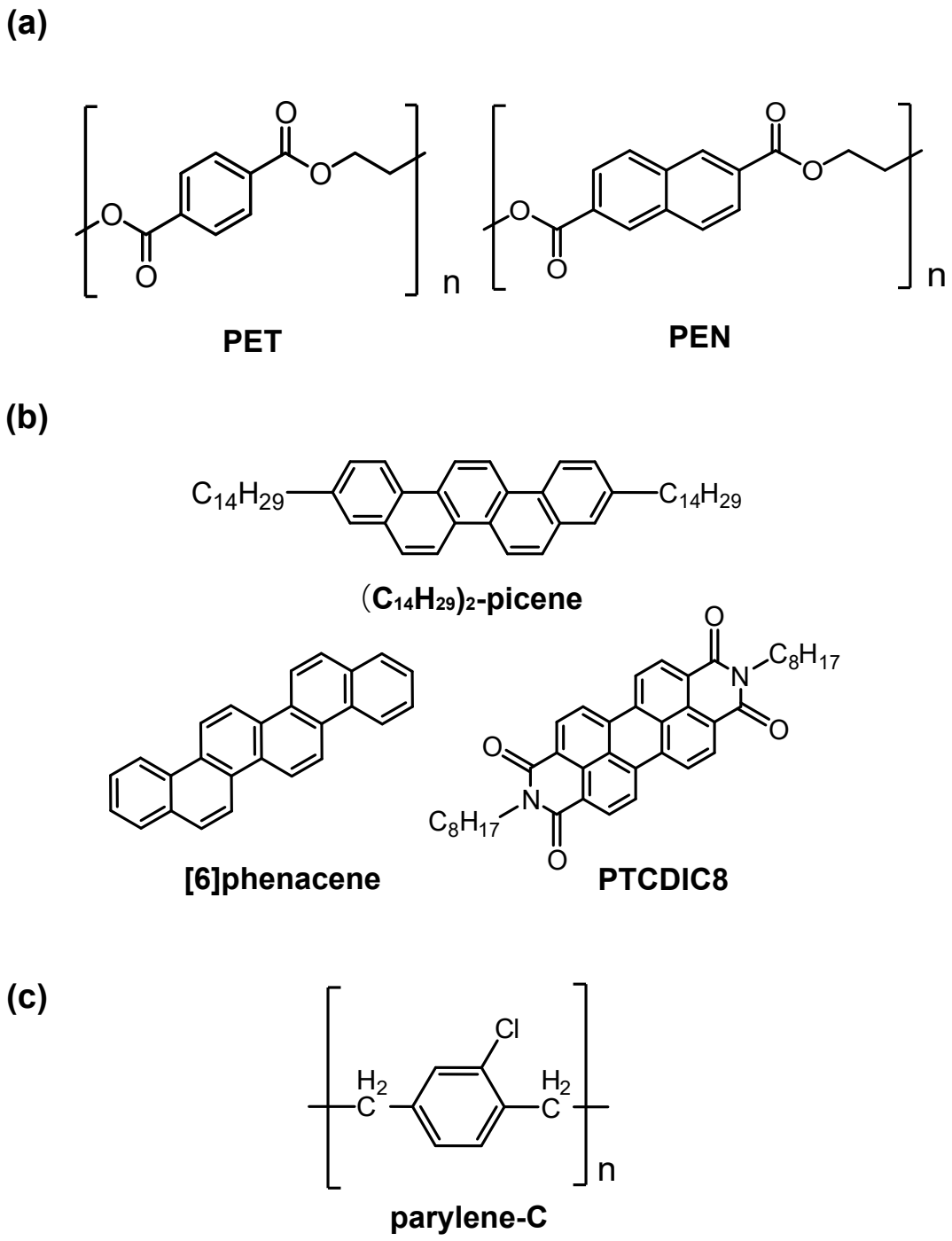
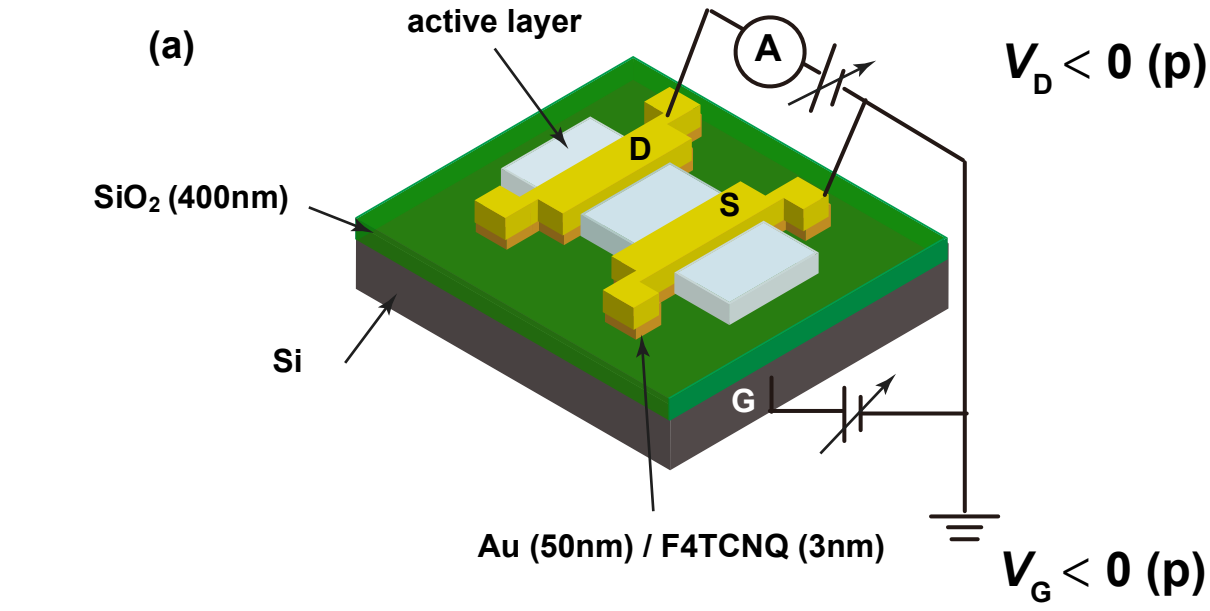


Figure 1. Pompei *et al.*



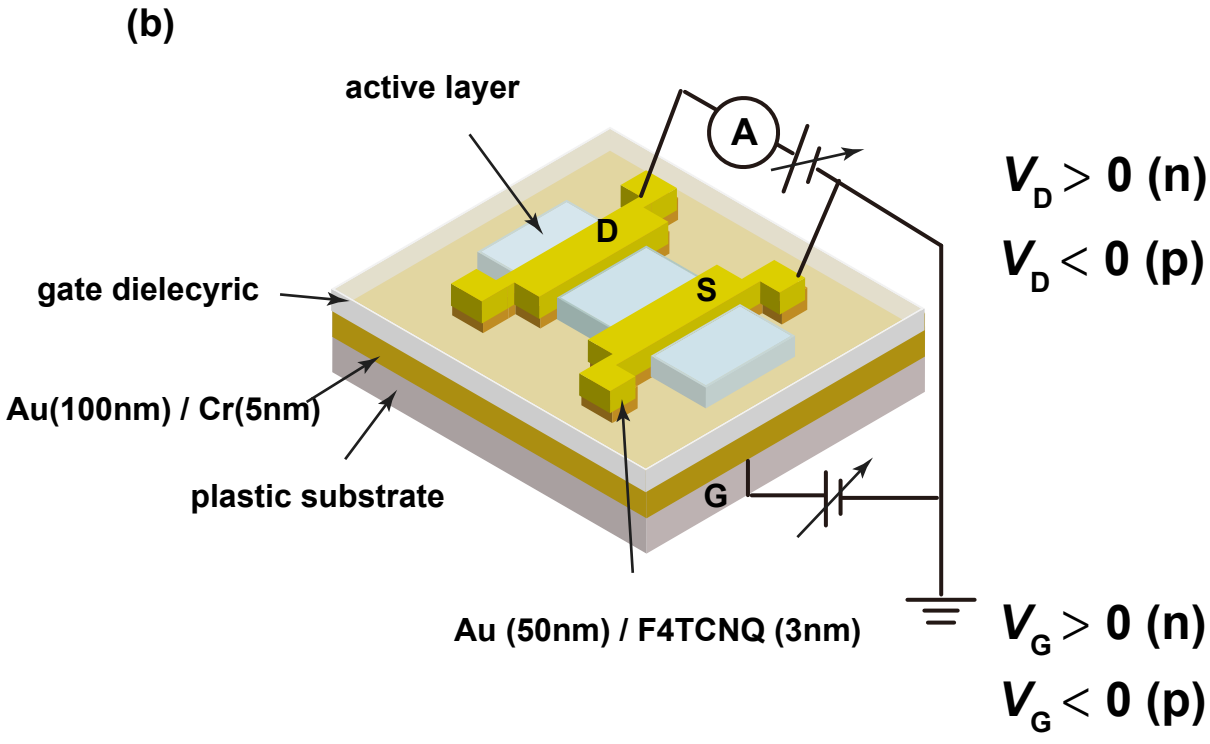


Figure 2. Pompei *et al.*

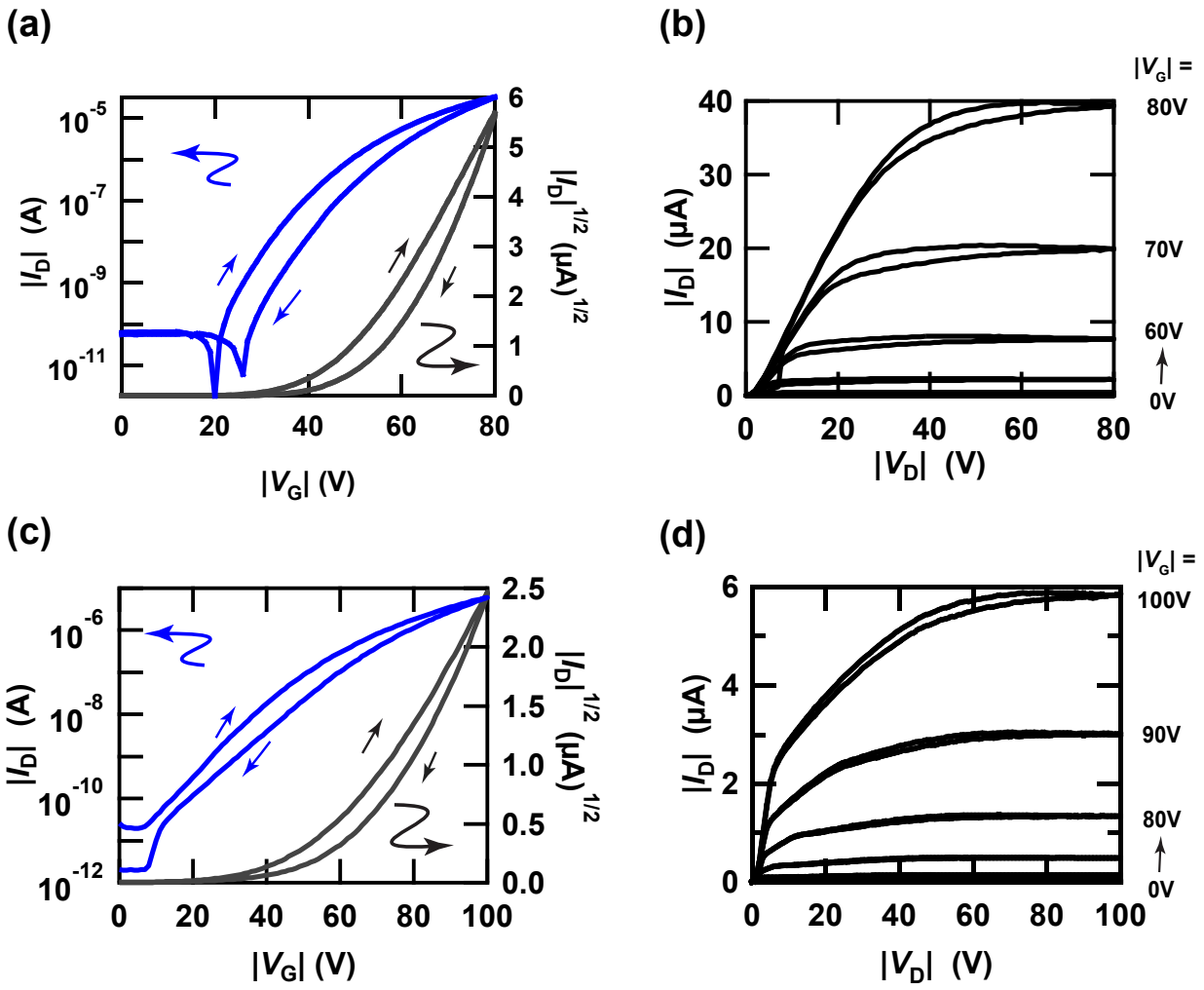


Figure 3. Pompei *et al.*

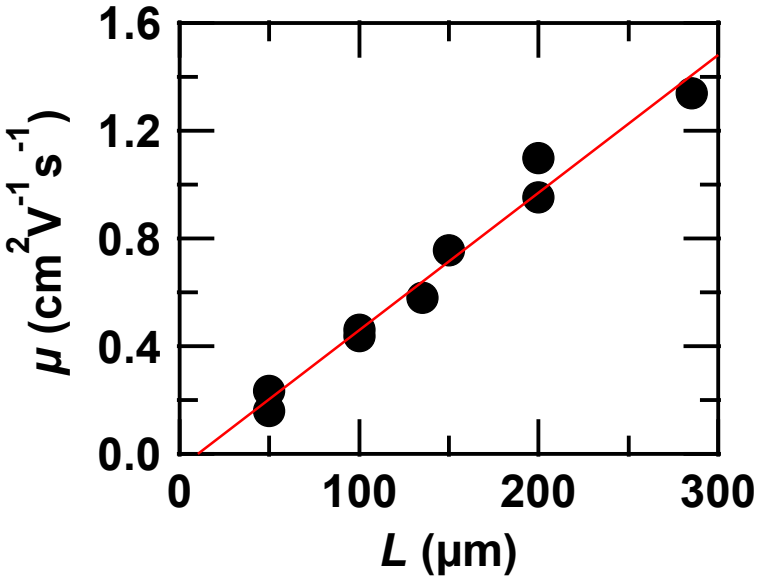


Figure 4. Pompei *et.al.*

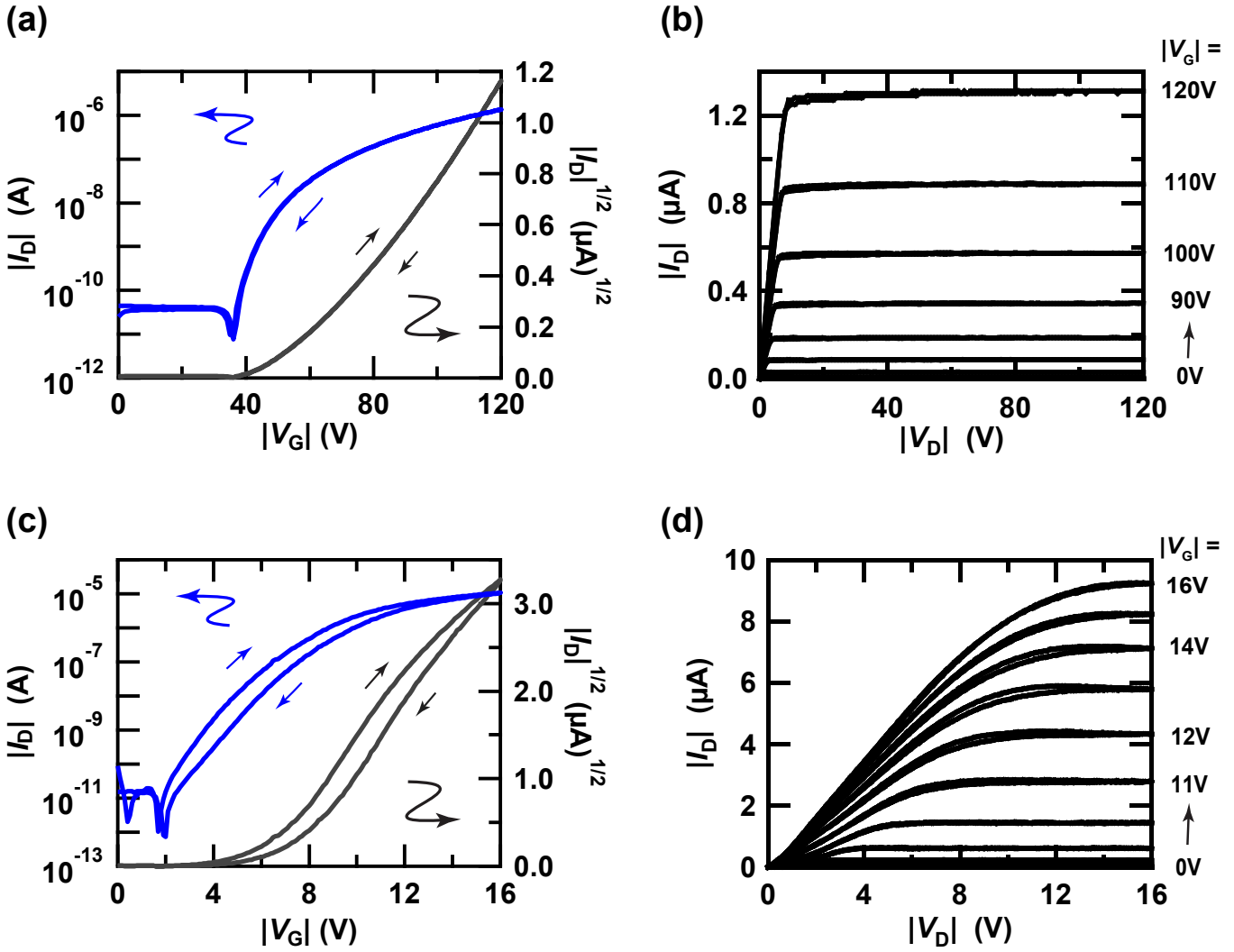


Figure 5. Pompei *et.al.*

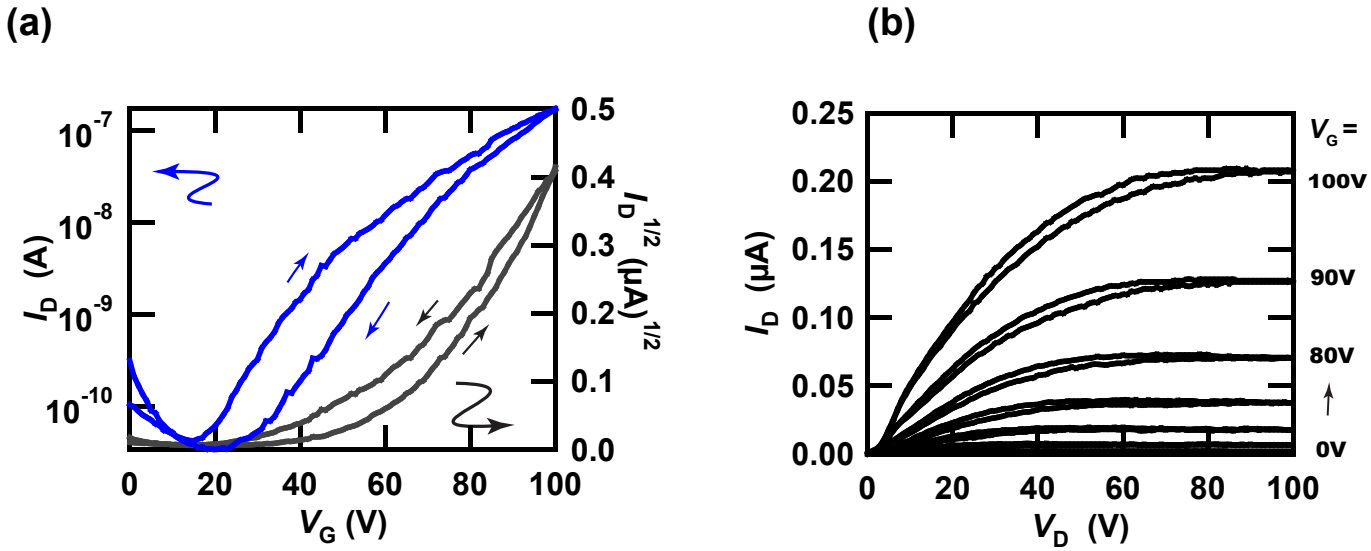


Figure 6. Pompei *et al.*

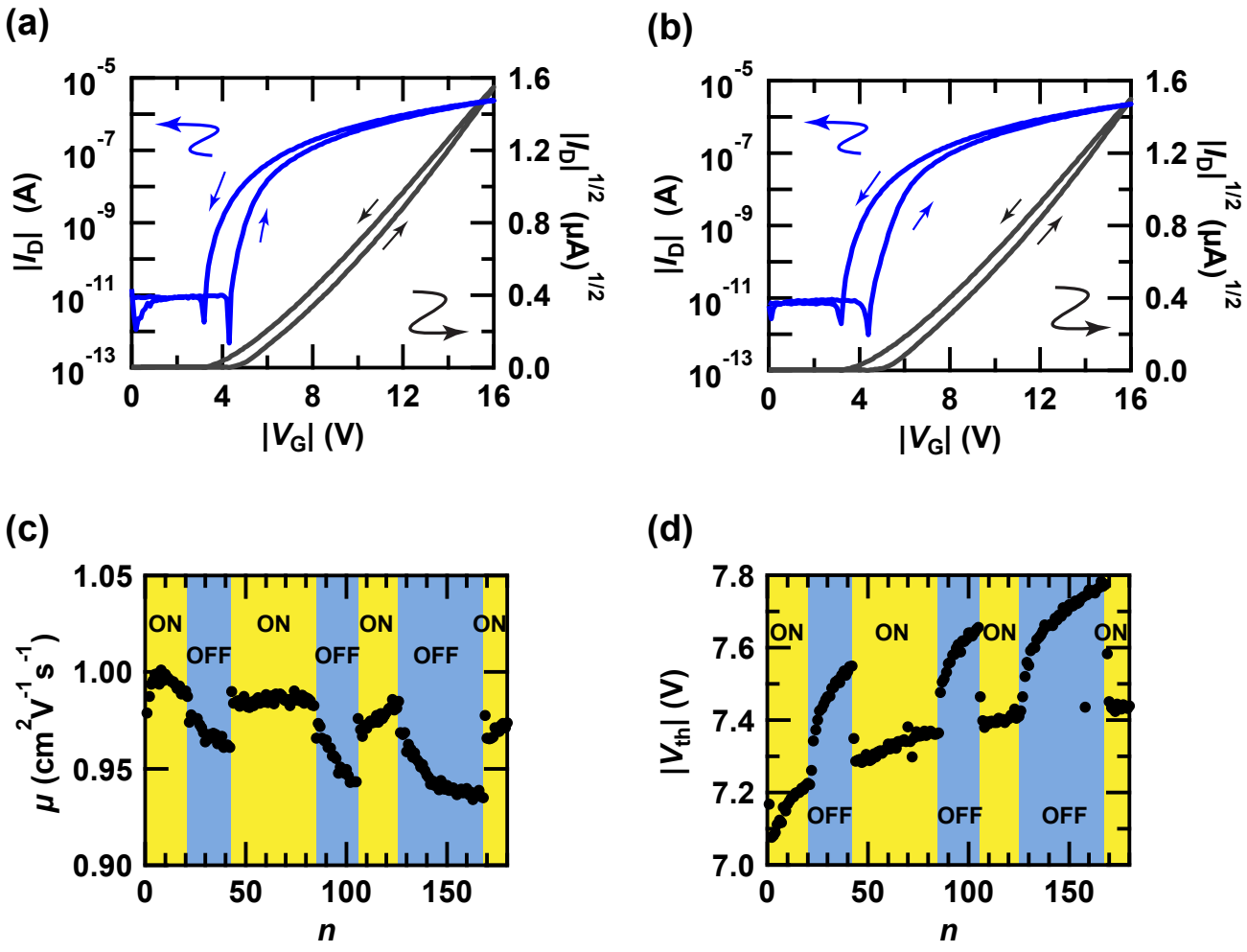


Figure 7. Pompei *et.al.*

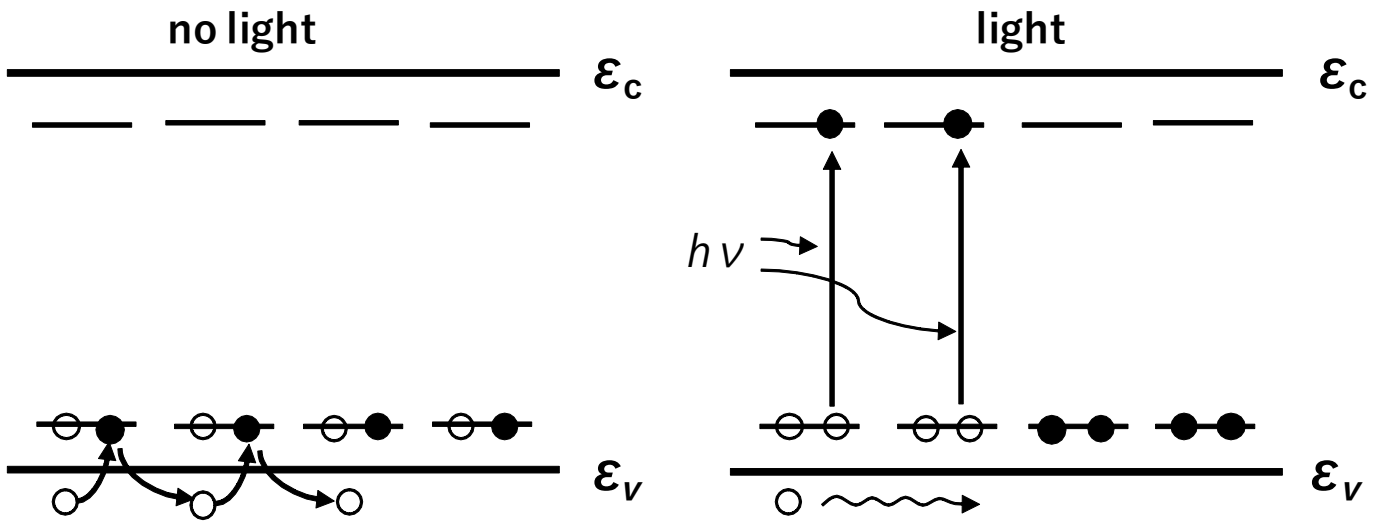


Figure 8. Pompei *et al.*

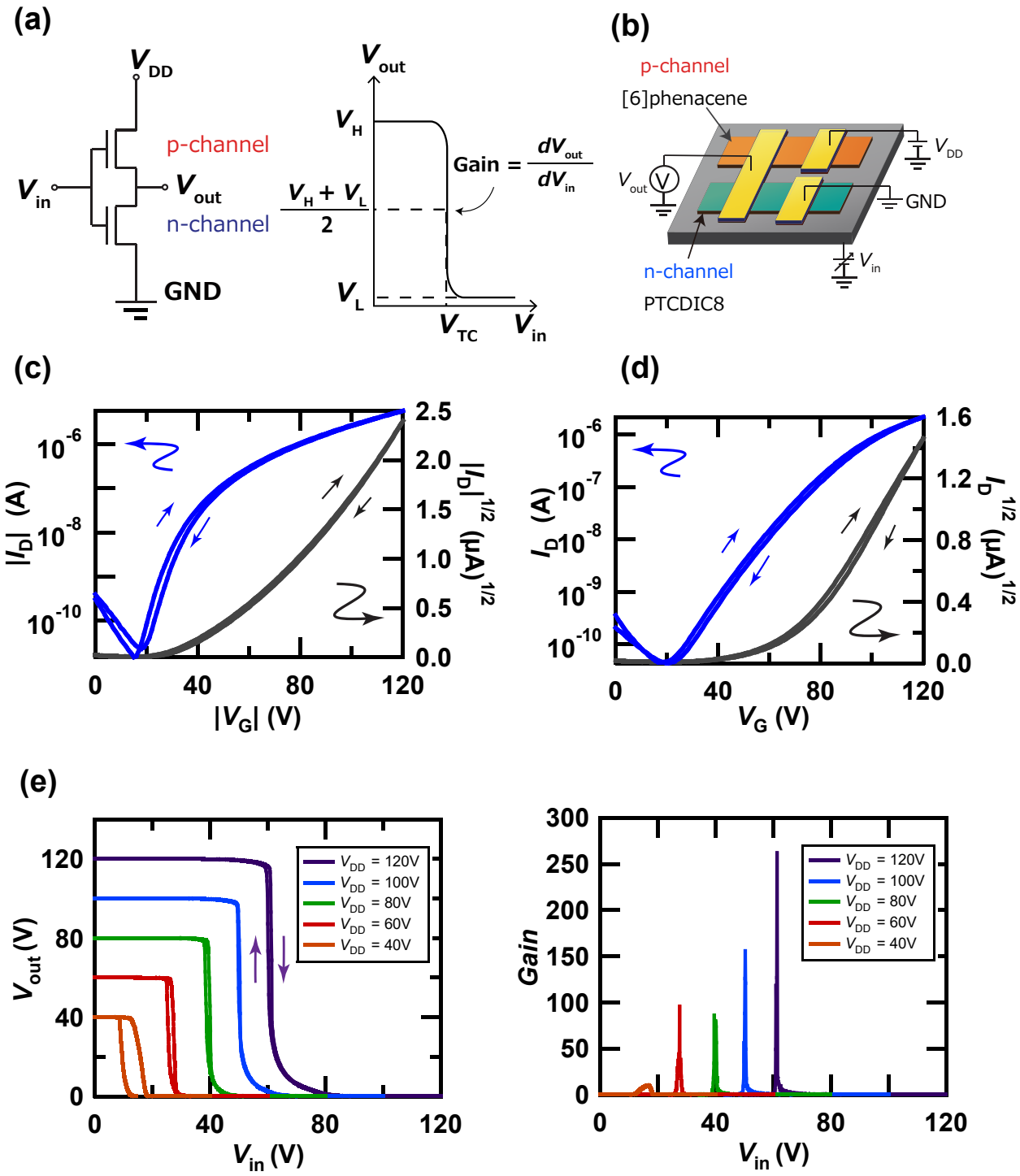


Figure 9. Pompei *et al.*

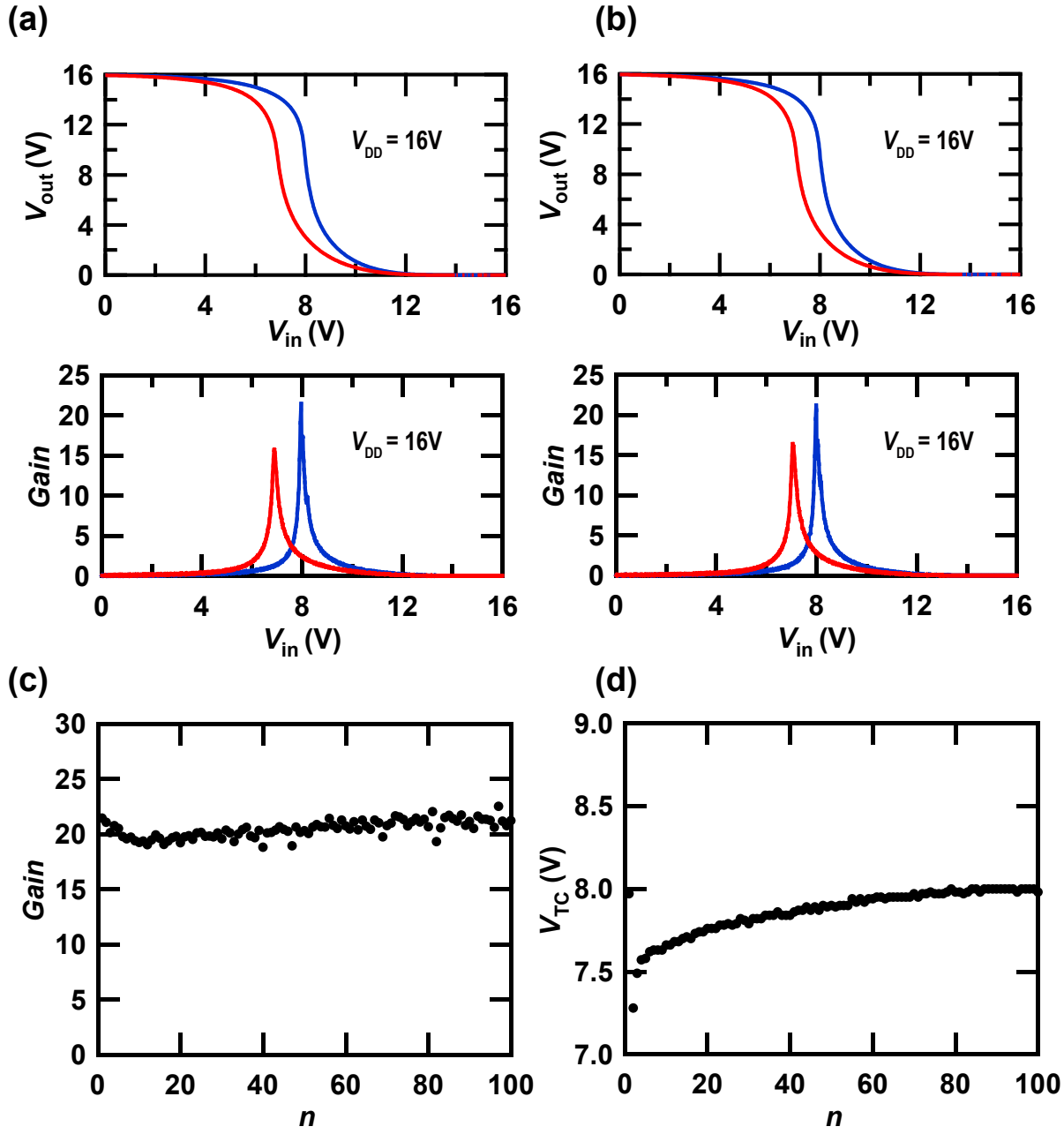


Figure 10. Pompei *et al.*