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Automated Characterization and Assembly of Individual Nanowires for Device Fabrication[†]

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The automated sorting and positioning of nanowires and nanotubes is essential to enabling the scalable manufacturing of nanodevices for a variety of applications. However, two fundamental challenges still remain: (i) automated placement of individual nanostructures in precise locations, and (ii) the characterization and sorting of highly variable nanomaterials to construct well-controlled nanodevices. Here, we propose and demonstrate an integrated, electric-field-based method for the simultaneous Automated Characterization, Manipulation, and Assembly of Nanowires (ACMAN) with selectable electrical conductivities into nanodevices. We combine contactless and solution-based electro-orientation spectroscopy (EOS) and electrophoresis-based motion-control, planning and manipulation strategies to simultaneously characterize and manipulate multiple individual nanowires. These nanowires can be selected according to their electrical characteristics and precisely positioned at different locations in a low-conductivity liquid to form functional nanodevices with desired electrical properties. We validate the ACMAN design by assembling field-effect transistors (FETs) with silicon nanowires of selected electrical conductivities. The design scheme provides a key enabling technology for the scalable, automated sorting and assembly of nanowires and nanotubes to build functional nanodevices.

1 Introduction

One-dimensional (1D) nano-materials such as nanowires, nanotubes, and nanorods, with small diameters, large surface areas and smooth surfaces, have many novel functional properties¹. For instance, extensive work has shown that nanowires or nanotubes can display unique electronic^{2–4}, optical^{5,6}, thermophysical^{7–9}, magnetic^{10,11}, and mechanical properties^{12–14}. Nanowire-based functional devices include various electronic^{15,16}, optoelectronic¹⁷, and photonic^{18,19} components, as well as batteries^{20,21}, solar-cells^{22–24}, and chemical, biological, biomedical sensors^{25–28}, among others. To fully realize the aforementioned potentials of functional nanodevices, it is highly desirable to have automated methods to characterize, manipulate, and assemble nanowires or nanotubes with desired characteristics into nanodevices at specific spatial locations and orientations. However, the automated manipulation and assembly of individual nanowires or nanotubes is still a largely unmet fundamental challenge^{29–32}. Furthermore, it has been shown that

the nanomaterials of the same composition, fabricated within the same batch, and even from the same sample, often exhibit highly variable properties, with nanowire conductivities, for example, varying by two or more orders of magnitude¹. Therefore, it is crucial to characterize the electrical properties of the nanowires and separate them before assembly. The challenges of nanodevice fabrication/manufacturing are at least twofold: (i) the automated placement of nanostructures in precise locations for functional devices and (ii) the automated characterization and separation of nanomaterials by functional properties.

The use of electric fields to position and sort micro- and nanoparticles provides one solution to address the aforementioned challenges for device fabrication. Under precisely controlled electric fields in fluid suspension, a variety of phenomena, including electrophoresis (EP), electro-osmosis (EO), dielectrophoresis (DEP), and electro-orientation, can be used as a driving force to steer, characterize and sort nanowires^{1,33–37}. Alternatively, a MEMS device is designed to characterize the electrical and mechanical properties of individual silicon nanowires in³⁸. Probe-based pick-and-place nanomanipulation inside the SEM³⁹ is needed to transfer individual nanowires from their growth substrates onto the MEMS device. Similarly, a post-processing nanowire-removal technique is developed in⁴⁰ for nanowire-based FET device fabrication. Large quantities of nanowires with uncontrolled number and varying diameters are scratched from

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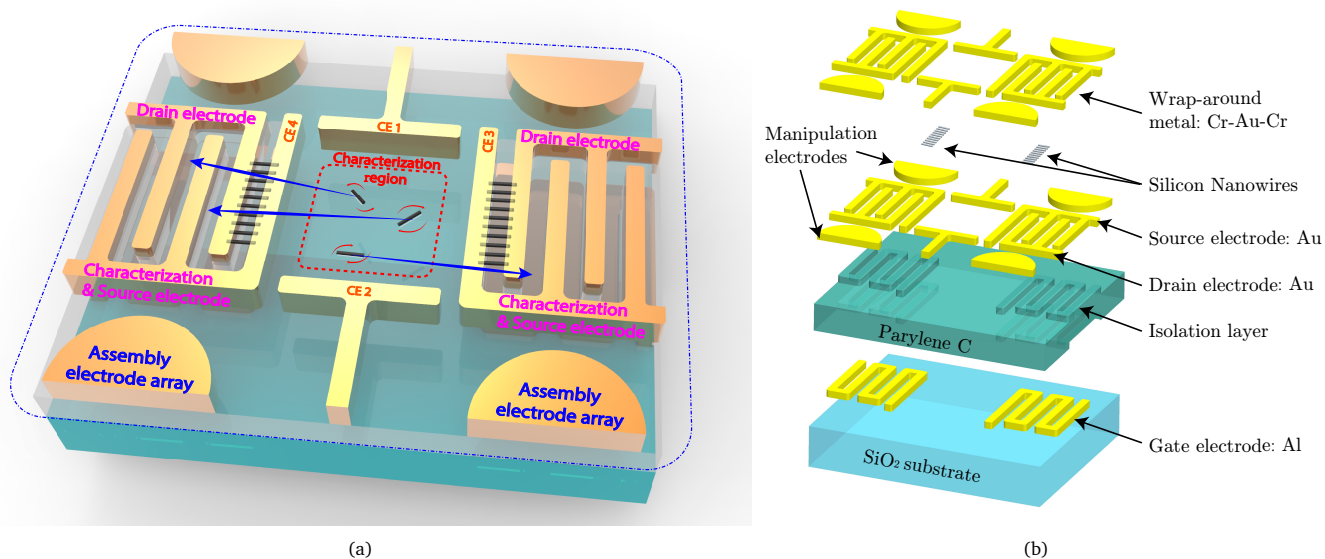


Fig. 1 (a) Schematic of the ACMAN system to fabricate nanowire-based FETs with selected electric properties. First, nanowires are steered from their starting locations to the characterization region (a $150\ \mu\text{m} \times 150\ \mu\text{m}$ square region in the center marked by the red dash line). Then, the electrical conductivities of multiple individual nanowires are quantified with EOS in the characterization region. Meanwhile, the EP-based motion-control, planning, and nanowire-manipulation strategies are used to keep the targeted nanowires inside the characterization region. After characterization, those nanowires are separated and positioned according to their electrical conductivities and finally deposited between the source and drain electrodes to form FET nanodevices. (b) Fabrication schematic for the Si NW-based bottom-gate FETs.

the growth substrate along a single direction. After batch micro-fabrication process of patterned electrodes, unwanted nanowires bridging the source and drain electrodes are removed using nanoprobe under SEM image feedback. These tip-based techniques require ultra-high-vacuum environments, clean rooms, and specialized equipment for precisely positioning and probing. Compared with these tip-based nanomanipulation and assembly approaches^{39–41}, the use of electric-field-induced forces has the advantages of greater efficiency, ease, lower cost and superior scalability.

Particles in fluid suspension experience an EP force under DC fields, while the fluid itself experiences EO forces⁴². The EP force magnitude is proportional to the effective electrokinetic potential (*i.e.*, the zeta-potential) and the field strength. The use of EP force as an actuation source is convenient in that even nominally electrically neutral particles typically have a nonzero electrostatic potential at the slip plane in the interfacial double layer in some solvents or at some pH values. Thus, by actuating a set of electrodes, nanowires in fluid suspension can be manipulated and steered to desired locations under a precisely controlled electric field^{1,37,43}. An EP-based motion-planning and manipulation scheme was developed to drive single^{35–37} and multiple^{43–45} individual nanowires in fluid suspension from one location to their targeted positions. DEP is also commonly used to manipulate and sort nanowires in microfluidic devices^{46–48}. In DEP, the induced dipole moment of the particle interacts with a non-uniform field to give rise to a frequency-dependent force. The DEP force depends on the polarizability of the particle and is proportional the gradient of the field squared. By tuning the field magnitude and the frequency of the applied field, the DEP force is used to manipulate the position of nanowires in fluidic suspension.

DEP also makes possible the characterization and sorting of nanomaterials based on electrical properties⁴⁹. Motion responses under different DEP frequencies have been used to separate^{50,51} and assemble nanowires into functional nanodevices^{52,53}. The DEP-based selection of nanowires provides a rapid mechanism for isolating silicon nanowires (Si NWs) with the highest conductivity and lowest defect density^{52,53}. However, compared with probe-based measurements, previous DEP- and solution-based methods do not precisely quantify the physical properties of each individual nanowire. To address this challenge, a contactless and solution-based electro-orientation spectroscopy (EOS) has recently been developed to measure¹ and sort³⁴ individual nanowires. The EOS technique is based on transient nanowire alignment in AC electric fields of different frequencies to quantitatively measure conductivities of individual nanowires.

Here, we extend the EOS technique to multiple individual nanowires, and combine the characterization with the controlled nanowire manipulation techniques^{43,44} to develop the Automated Characterization, Manipulation, and Assembly of Nanowires (ACMAN) process. To demonstrate the integrated process, we have also fabricated and tested proof-of-concept Si NW-based FETs with selected electrical conductivities. The primary contributions of this paper are: (1) Demonstrating the electrical characterization and sorting of multiple individual nanowires, (2) Integrating the characterization with the automated manipulation/assembly of 1D nanoparticles, into a microfluidic system that is capable of processing simultaneous multiple individual nanowires in a completely online and automated manner; and (3) Experimentally demonstrating the feasibility of the proposed ACMAN system to build Si NW-based functional nanodevices with chosen electrical conductivities. The performance of the FETs

demonstrates not only the feasibility of the integrated ACMAN process, but also the importance of quantitative separation for device fabrication.

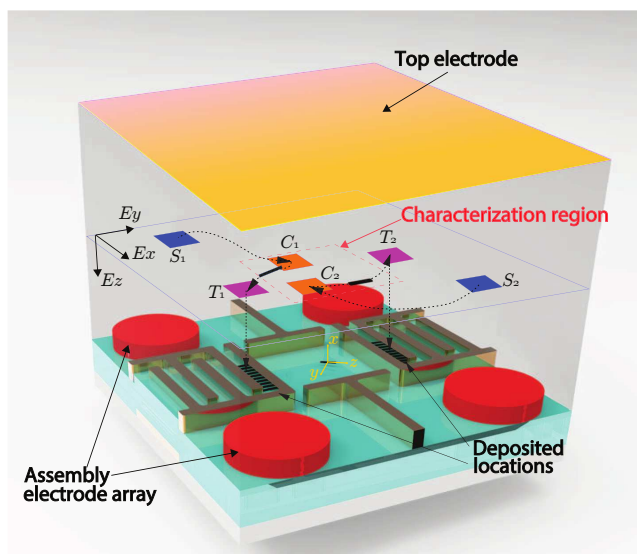


Fig. 2 Schematic of microfluidic device with 2×2 independently actuated assembly electrode array on a bottom substrate, with a common top electrode. The assembly electrode array is used to steer nanowires in fluid suspension at initial locations S_1 and S_2 to the targeted characterization locations C_1 and C_2 and keep them inside the characterization region. Then, after characterization, they are driven to the desired deposition locations T_1 and T_2 . The top electrode is used to control the nanowires in vertical direction to deposit them on the substrate.

2 Automated characterization, manipulation, and assembly of nanowires (ACMAN)

2.1 Integrated ACMAN design

We briefly introduce the ACMAN design before giving more detail in the following sections. Fig. 1(a) illustrates the schematic of the complete ACMAN system to fabricate nanowire-based functional nanodevices. Two regions are defined in the design:

- **Assembly region:** A 3D workspace among the centers of the assembly electrode array, shown in the blue dotted rectangle in Fig. 1(a). The 2×2 assembly electrode array is used to first manipulate nanowires into the characterization region and then after characterization, those electrodes are further used to move nanowires into desired locations for device assembly. One set of characterization electrodes (CEs) is also re-used as the source electrodes for the FET device, shown as the finger-shaped interdigitated electrodes in Fig. 1(a).
- **Characterization region:** A $150 \mu\text{m} \times 150 \mu\text{m}$ square region in the center marked by the red dash line in Fig. 1(a) (schematic illustration) and Fig. 3 (experimental setup). This area is used to measure the conductivity of multiple individual nanowires. The nanowires experience uniformly distributed electric field in the characterization region.

The integrated ACMAN process includes the following four steps:

1. **Manipulation towards characterization region:** Nanowires of interest in the manipulation region are spotted and steered from their starting locations to the characterization region using the developed motion-control, planning, and manipulation strategies. In this step, only the circular assembly electrode array is activated.
2. **Characterization:** Multiple individual nanowires are quantified with EOS in the characterization region. Only the CEs shown in Fig. 1(a) are activated, to avoid other influences on the electro-orientation. In this particular design, either CE 1 or 3 is connected to the AC signal source, while the corresponding CE 2 or 4 is switched to ground, respectively. To extract different alignment rates for each nanowire, AC fields with frequency ranging from 1000 Hz to 4 MHz are applied to CE 3, while CE 4 is grounded, and all other electrodes are floating. After each alignment under one frequency of the AC fields generated through CEs 3 and 4, another AC field is applied through CEs 1 and 2 to reorient the nanowires back for repeated measurements at different frequencies. Due to AC electroosmosis^{54,55}, Brownian motion, imperfect electrode edges causing locally field concentrations and non-uniform electric field, and flow disturbances, the particles experience unexpected motion and drifting during the characterization process. The motion-control, planning, and nanowire-manipulation strategies discussed in the next section are used to keep the targeted nanowires inside the characterization region.
3. **Separation manipulation:** After automated characterization, the nanowires are sent to different target locations according to a conductivity threshold, σ_{th} . Again, the online motion control, planning, and manipulation of nanowires are used to separate those nanowires with preferred conductivities towards different desired assembly locations. For example, low-conductivity (LC) Si NWs ($\sigma_{\text{p}} < \sigma_{\text{th}}$) are moved to the right pair of source/drain electrodes, while high-conductivity (HC) Si NWs ($\sigma_{\text{p}} \geq \sigma_{\text{th}}$) are steered towards the left pair.
4. **Deposition:** Once the nanowires reach their desired locations in fluid, an additional common top electrode, the ITO coverslip on top of the microfluidic channel, is turned on, while all the other electrodes on the substrate are switched to ground to drive nanowires vertically to reach the bottom substrate. Finally, different AC fields are applied to CEs 3 and 4 according to the separation criterion and the counter finger-shaped electrodes are switched to ground. The generated DEP forces capture, attract, and align the nanowires across the source-drain gaps.

In each experiment, a droplet of nanowire suspension is applied to the microfluidic channel. The human operator specifies the separation criterion and selects the nanowires of interest to be analyzed in a visualization user interface. The aforementioned steps 1 to 4 are conducted automatically then repeated sequentially until the desired number of nanowires are deposited. The

details of the automation implementation are reported in the supplementary material.

2.2 Motion control, planning, and manipulation of nanowires under electric-fields in fluid suspension

For self-contained presentation, we briefly present the motion control, planning, and manipulation of nanowires under electric-fields in fluid suspension^{37,43}. Fig. 2 shows the schematic of the microfluidic device to manipulate nanowires. The nanowires were suspended in a droplet of fluid with a generic square-lattice assembly electrode array on the bottom substrate of a microfluidic reservoir. Those electrodes can be independently actuated with different DC voltages to generate the electrical field to control the nanowires motion in the horizontal plane. A top electrode is used to control the nanowires in the vertical direction. Once the nanowires reach their desired deposition locations, the bottom electrodes are turned off and the electrode on the top surface is turned on to align and drive the nanowires vertically until they reach the bottom substrate. Finally, the electrode arrays are turned on again to lay down and deposit the nanowire onto the device surface with the desired orientation.

To compensate for un-modeled disturbances such as EO-induced flow motions, a robust motion control strategy was developed to guarantee the path-following errors convergence for individual nanowires^{37,43}. The path-tracking control adjusts the desired velocity profile according to the direction of the desired trajectory, penalizes the tracking direction, and compensates for the predicted error. A self-placing time-suspension technique is also used to adjust the desired rate of the progression and then the velocity profile online within the planning framework at each time step. Heuristic³⁷, network flow⁴³, and sampling⁴⁵-based motion planning algorithms are utilized to achieve the shortest-distance and minimum-time objectives. These planning algorithms addressed combinatorial optimization with coupled actuation to control multiple nanowires and were validated to simultaneously steer multiple nanowires to follow desired trajectories under controlled EP forces^{35–37,43–45}. Previous work show that the nanowires can be positioned with spatial accuracy of $2\mu\text{m}$. More motion-control and motion-planning details can be found in the supplementary information.

2.3 Automated characterization of multiple nanowires using electro-orientation spectroscopy

The contactless and solution-based electro-orientation spectroscopy (EOS) technique is built upon the direct optical visualization of the frequency-dependent alignment rates of nanowires when they are suspended in a liquid of known properties under a spatially uniform AC electric field of different frequencies³⁴. In the framework of Maxwell-Wagner interfacial polarization⁵⁶, the particle electrical properties are shown in the frequency dependent induced dipole moment. Thus, the alignment rates of nanowires vary under changing frequencies of AC electric fields for 1D nanomaterials of different electrical properties. In particular, the *crossover frequency* indicates the transition of the alignment rate at low frequencies (conductivity dominated alignment)

to that at high frequencies (permittivity dominated alignment). For high aspect-ratio nanowires suspending in a low-conductivity solvent, the crossover frequency ω_c simplifies to^{1,34}

$$\omega_c \cong \frac{\sigma_p}{\epsilon_m(L_{||}^{-1} - 1)}, \quad (1)$$

where σ_p is the conductivity of the particle, ϵ_m is the permittivity of the fluid, and $L_{||}$ in equation (1) is the geometric depolarization factor given by

$$L_{||} \approx \frac{\ln 2\beta - 1}{\beta^2}, \quad (2)$$

where $\beta = a/b$ is the aspect ratio of the prolate-spheroidal-shaped nanowire, and a and b are the semi-major and semi-minor axes of the prolate spheroid, respectively.

By measuring the alignment rates of an individual nanowire at different frequencies, a crossover frequency ω_c is extracted. The geometric depolarization factor $L_{||}$ is determined by estimating the length of the particle using acquired images. Therefore, using (1) the effective electrical conductivity σ_p of the nanowire can be estimated, assuming a known permittivity ϵ_m of the medium.

To enable the capability of characterizing multiple individual nanowires simultaneously using the EOS principle, a pair of parallel electrodes are designed to generate uniformly distributed AC electric fields. Ideally, the uniform field only generates electro-orientation, *i.e.*, no DEP-induced translation motion. If needed, the manipulation electrodes can be used to recenter the nanowires in the characterization region. One pair of parallel electrodes is actuated by AC electric fields of different frequencies to extract different alignment rates for each nanowire, while the other pair of parallel electrodes is used to re-orient the nanowires for repeated measurements under different frequencies. In the multiple-nanowire-characterization process, multiple image regions of interest are tracked simultaneously, with each region of interest containing one nanowire. The dimension and orientation of each nanowire are calculated from the time-lapse image series. The maximum alignment rate at each measured frequency is recorded and plotted to observe the crossover frequency. In order to obtain the crossover frequency, we use the least squares method to fit the alignment rate at different frequencies as

$$\Omega^i(\omega) = \frac{1}{1 + (\omega/\omega_c^i)^2}, \quad (3)$$

where Ω^i is normalized alignment rate of the i th nanowire, ω is the different frequencies of the applied electric field, and ω_c^i is the fitted cross-over frequency for the i th nanowire. Finally, the conductivity of each nanowire is calculated by plugging the crossover frequency into (1) and (2) with the known medium permittivity ϵ_m and the aspect ratio of the particle β , estimated from the online measurements of the nanowires' dimension.

3 Automated assembly of Si NW-based FETs using ACMAN

We demonstrate the ACMAN process by assembly FET devices with Si NWs of different electrical conductivities. In this section, the micro-fabrication of the FET device is briefly discussed. Next,

the performance and characteristics of the assembled nanodevices are experimentally measured and evaluated.

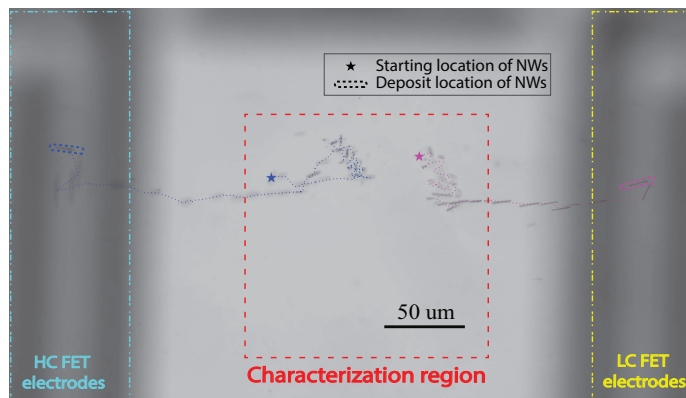


Fig. 3 Overlaid trajectories of two Si NWs separated by their different electrical conductivities using the ACMAN process. The low-conductivity Si NW ($\sigma_{LC} = 0.045$ S/m) is placed between the right pair of FET electrodes, while the high-conductivity Si NW ($\sigma_{HC} \geq 0.46$ S/m) is placed between the left pair of FET electrodes. The red dash square shows the characterization region. The star and ellipse marks represent the starting and target locations of each nanowire. The figure shows overlaid center-of-mass trajectories of the two simultaneously characterized and separated nanowires. The corresponding alignment-rate measurement and crossover-frequency extraction can be found in Supporting Information (SI, Fig. S11). Electronic supporting video is also available online.

3.1 Microfluidic device and Si NW FET fabrication

Conventional microfabrication techniques are used to fabricate electrodes for the microfluidic device that conducts the automated characterization, manipulation, and assembly process. The assembled nanowires with different conductivities on the microfluidic device eventually form the FETs with different characteristics. Fig. 1(b) illustrates the fabrication steps of the Si NW-based bottom-gate FETs.

The FETs are designed to be fabricated on glass wafers (SiO_2 substrate). A 300 nm-thick aluminum layer with 12 μm width in channel gap is patterned as the bottom gate on the SiO_2 substrate using photolithography and sputtering. Parylene C thin film is used to serve as the isolation layer between the gate and the body of the semiconductor. The thickness of the parylene C film is designed as 700 nm. Parylene films are highly biocompatible, biostable with high flexibility and have excellent solution processability. The thickness is uniformly controllable, and the coating is conformal and completely pinhole-free at thicknesses greater than 500 nm. On the top of the substrate and dielectric layer, gold electrodes are patterned using a photolithographic lift-off step. The gold-electrode structure is 300 nm in thickness including a 10 nm chromium adhesion layer. The gold structure contains finger-shaped source/drain electrodes and a 2×2 assembly electrode array with the center-to-center displacement of $L = 900 \mu\text{m}$. The finger-shaped gold electrodes are 30 μm in width with 15 μm channel gap. Due to the conformal coating of parylene films, the channel gap is filled with parylene as the same height as the source and drain electrodes. Therefore, the air gap between the Si NWs and the dielectric layer is minimized to enhance the per-

formance of the FET.

The Si NWs used in the experiments are fabricated using metal-assisted chemical etching from lightly doped (3000 - 5000 $\Omega\text{-cm}$ in average resistivity or $3.3 \times 10^{-2} \Omega^{-1}\text{m}^{-1}$ in bulk conductivity) and heavily doped (3 - 5 $\Omega\text{-cm}$ in average resistivity) n-type silicon wafers. See Supporting Information for a SEM image of as-grown Si NWs (SI, Fig. S10).

Before each experiment, the Si NWs are detached from the aforementioned two types of wafers and suspended in mineral oil to form a mixture of Si NW suspension with a large variation of conductivities. Mineral oil (Drakeol 7 LT Mineral Oil, Calumet Specialty Products and Partners, L.P.; $\epsilon_m = 2.0 \times 10^{-11}$ F/m, and viscosity $\mu_m = 25.9$ cP) is used because of its low conductivity, which results in a thick electrical double layer around the particle and minimizes induced charge electro-osmosis³⁴. Up to ± 50 V DC voltages are applied to assembly electrodes array and 50 V_{pp} AC fields with various frequencies from 1000 Hz to 4 MHz are used in EOS characterization. Si NWs are separated by threshold conductivity $\sigma_{th} = 0.2$ S/m to either side of the desired assembly locations and finally deposited as a thin film of Si NWs to bridge the source and drain electrodes. Approximately 8-12 individually selected nanowires are deposited in each pair of the source and drain electrodes. The selection of threshold value $\sigma_{th} = 0.2$ S/m is based on the effective measurement range of EOS using mineral-oil as the suspending fluid (from 10^{-5} to 1 S/m) and the previously measured conductivity distribution over 100 as-produced and passivated Si NWs (ranging from 10^{-3} to 10 S/m with average about 0.2 S/m)³⁴. In the final deposition process, two 50 V_{pp} AC fields with $\omega_L = 20$ kHz (attracting Si NWs with conductivities above $\sigma_L = 0.001$ S/m) and $\omega_H = 2$ MHz (attracting Si NWs with conductivities higher than $\sigma_H = 0.15$ S/m) are used to trap the nanowires in the less-conductive and more-conductive assembly locations, respectively. Fig. 3 shows the overlaid nanowire trajectories for two simultaneously characterized and sorted Si NWs. The LC Si NW ($\sigma_{LC} = 0.045$ S/m) is placed between the right pair of contact electrodes, while the HC Si NW ($\sigma_{HC} \geq 0.46$ S/m) is placed between the left pair of contact electrodes (see SI, Fig. S11 for the conductivity extraction). The star and ellipse marks represent the starting and target locations of each nanowire.

After nanowire characterization and deposition, the top coverlip and adhesive channel are removed with care. The device is soaked in hexane for about 10 minutes, and then gently rinsed with hexane and isopropyl alcohol (IPA) to remove oil residues, before being gently dried under N_2 flow. All those solvent removal and evaporation processes are handled with great care, to minimize disturbance to the nanowires aligned between the device electrodes.

Finally, a second 350 nm-thick Cr-Au-Cr (100 nm chromium, followed by 150 nm gold, and then 100 nm chromium) layer is sputtered on the top of selected and positioned nanowires with the same pattern as the first gold layer. The top "wrap-around" Cr-Au-Cr layer increases the nanowire-metal contact area and enhances charge-carrier injection. Prior to the wrap-around metal deposition, the edges of the Si NWs at the source and drain contact regions are lightly etched in a buffered hydrofluoric acid (BOE) for 3 seconds to remove the native oxide on the nanowires, form-

ing clean contact regions between the Si NWs and contact metal. The choice of contact metals is dictated by both p- and n-type semiconductors, since p-type is usually observed in undoped Si NWs while n-type is observed in phosphorus doped semiconducting materials. The work function of gold is closely matched to the valence band edge of silicon to enable near-Ohmic contact for p-type transport, while chromium and aluminum metals reduce the Schottky barrier for n-type transport⁵⁷.

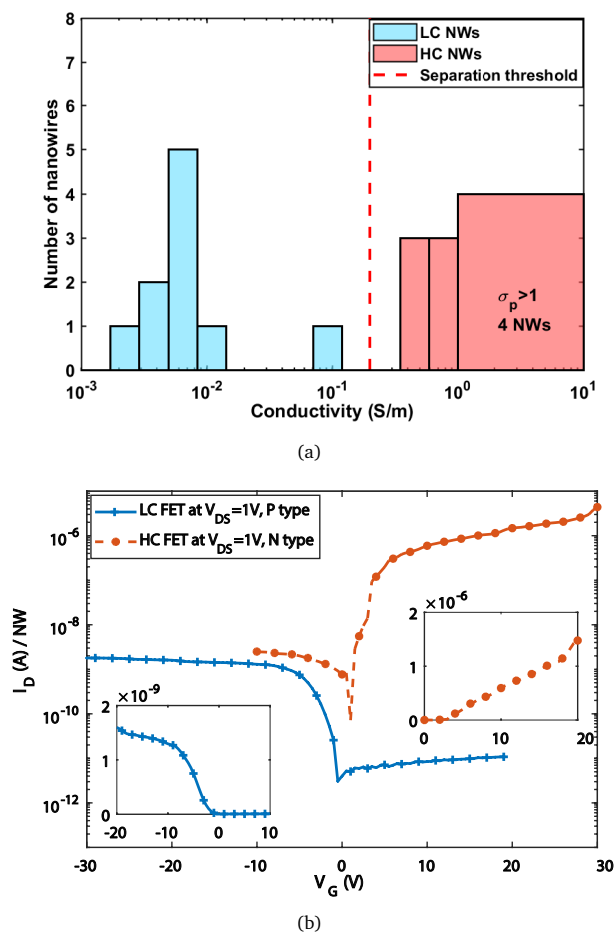


Fig. 4 Transfer characteristics of one of the ACMAN-assembled Si NWs FET devices. A total of 20 Si NWs were initially deposited, with 10 NWs selected and positioned on the HC and the LC sides, respectively, according to their conductivities using ACMAN. After the wrap-around electrode fabrication, the resulting FETs have 3 NWs on each side. The FET assembled with less-conductive Si NWs shows p-type characteristics while the FET assembled with MORE-conductive Si NWs shows n-type characteristics. (a) Measured conductivity distribution against the number of characterized nanowires by EOS characterization. (b) Transfer characteristics in logarithmic scale showing the drain current per nanowire at $V_{DS} = 1$ V with respect to gate voltage V_G for the p-type and n-type FETs after separation. Inset: The transfer characteristics in linear scale.

3.2 Characteristics and performance of assembled Si NW FETs

Following the fabrication process in Section 3.1, four assembled devices consisting of eight FETs are evaluated. Each device con-

tains two Si NW FETs: one side is assembled using LC Si NWs with $\sigma_{LC} < \sigma_{th}$, and the other side is assembled using HC Si NWs with $\sigma_{HC} \geq \sigma_{th}$, where $\sigma_{th} = 0.2$ S/m. All of the current-voltage characteristics of the assembled Si NW transistors are measured using an HP 4140B picoammeter. The detailed evaluation of the transfer characteristics (Figs. S2-S6) and performance metrics (Table S1) of fabricated devices can be found in the Supporting Information.

Fig. 4 shows the measured characteristics of one of the assembled devices. For this device, a total of 20 Si NWs were initially deposited, with 10 NWs selected and positioned on each side according to their conductivities. Fig. 4(b) shows the measured conductivity distribution of the 20 Si NWs that were characterized and separated using simultaneous multiple-nanowire EOS. In the current micro-fluidic device design, there are only four actuated assembly electrodes, therefore, according to⁴³, only two nanowires can be independently manipulated at same time with arbitrary trajectories. The 20 nanowires are characterized and manipulated two nanowires at a time, with a total of ten iterations. Fig. 3 and supporting video illustrate such one iteration. After the wrap-around electrode fabrication, 3 NWs remained on each side in the channel gap. The FET made with selected HC NWs shows n-type characteristics, while the lower conductivity side demonstrates p-type characteristics. Fig. 4(a) shows that the on-current in the HC NW FET is more than two orders of magnitude higher than that of the LC FET, consistent with the two orders-of-magnitude difference in the conductivity of the selected NWs. The large differences in current-voltage characteristics clearly show the importance of NW characterization and separation for consistent FET performance, even when the nanowires are from the same sample, as they were in this case.

For comparison, we also fabricated four FETs using only DEP assembly, omitting the EOS characterization and separation step of the ACMAN process (SI, Fig. S8). This is similar to the procedure described in the related previous work by other authors^{52,53}. Si NWs were collected at different DEP frequencies of 2 MHz and 20 kHz at a field strength of 50 V_{pp} and used to fabricate the HC and the LC FETs, respectively. These DEP frequencies were the same as those used in the deposition step to trap nanowires in the ACMAN scheme. The on-currents (I_{on}) of the four different DEP-only and four ACMAN-assembled FETs are compared in Fig. 5(a). The more conductive ACMAN FETs showed higher I_{on} than the HC DEP-only FETs. Moreover, the on-current ratio of the HC to the LC Si NW-FETs is at least one order of magnitude higher, and up to more than three orders of magnitude higher, for the ACMAN FETs as compared to the DEP-only FETs.

To further quantitatively evaluate the performance of FETs, the sub-threshold swing (S_s), NW trap density (N_{trap}), and device mobility (μ) are calculated for both LC and HC FETs in each device. Fig. 5(b) shows the S_s and N_{trap} data extracted from transfer-characteristic plots. The FETs constructed with HC Si NWs separated and assembled by the ACMAN scheme demonstrate consistently smaller values in both the S_s and trap densities. This behavior suggests that the ACMAN process yields more consistent and faster transitioning FETs, and this is due to better characterization and separation of the highly variable nanowires than

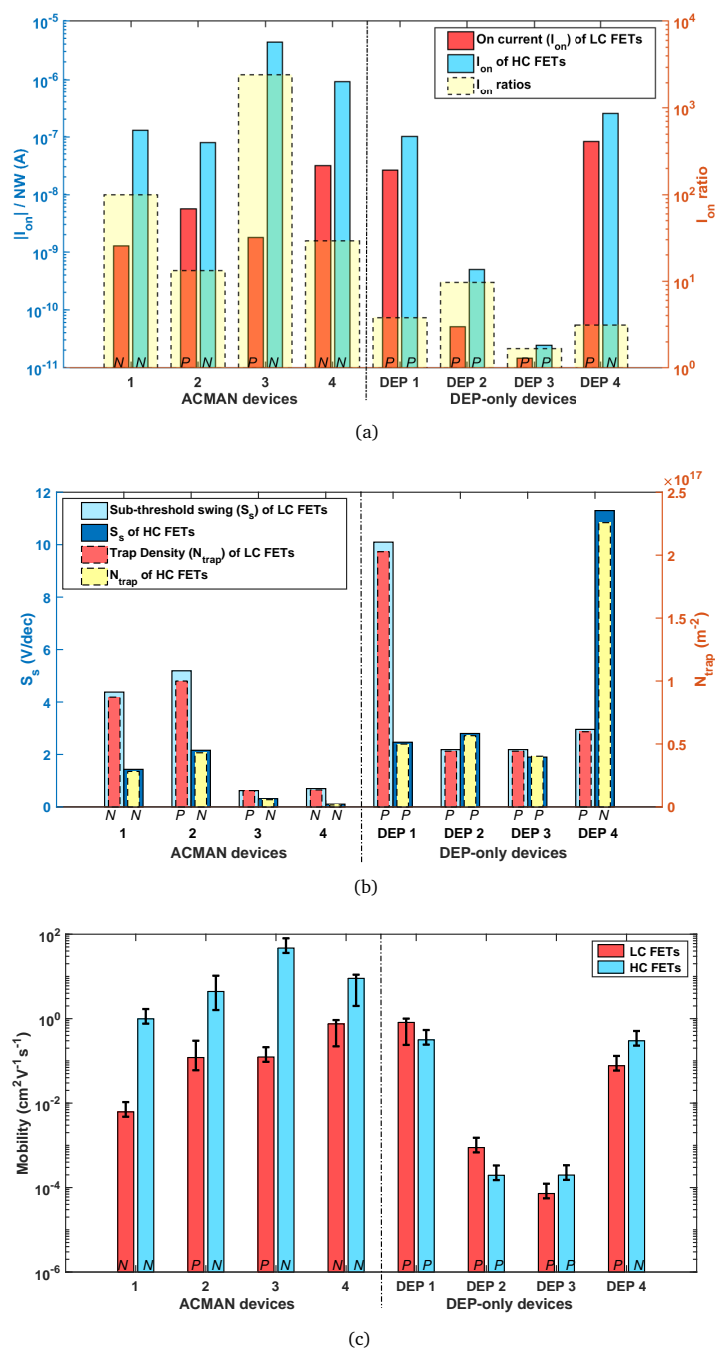


Fig. 5 Characteristics comparison of the four ACMAN and the four DEP-only assembled devices. “P” or “N” stands for the p- or n-type FET, respectively. (a) The on-current (the absolute value $|I_{on}|$) comparison. The red bars represent the on-current of the LC FETs and the blue bars stand for the HC FETs. The shaded dashed bar plots the on-current ratio of the HC FETs to the LC FETs. (b) The sub-threshold swing (S_s) and trap density (N_{trap}) comparison. (c) FET mobility comparison. The red bars represent the on-current of the LC FETs and the blue bars stand for the HC FETs.

DEP-only process.

Another performance metric, carrier mobility (μ), is calculated for the NW-based FETs using the cylinder-on-plate model⁵⁸ from the linear transfer regime. This model considers the finite number of NWs in the channel, as well as the electrostatic fringing

effect of the gate field acting on the aligned NWs. Fig. 5(c) compares the carrier mobility of both ACMAN-assembled and DEP-only FETs, with error bars representing the uncertainties due to variations in nanowire diameters and dielectric layer thickness. The mobility of the HC ACMAN FETs is greater than those of the HC DEP-only FETs by several orders of magnitude. The ACMAN scheme also produces consistently greater differences in HC and LC mobility than the DEP-only process. For the three devices that are most comparable, being p-type for the LC FET and n-type for the HC FET (ACMAN Devices 2 & 3, and DEP-only Device 4), the ACMAN strategy-produced devices outperform the DEP-only devices in terms of the HC-FET mobility, as well as S_s value and the ratio of on-currents of the HC to the LC FETs.

4 Discussion

We have experimentally demonstrated that the ACMAN scheme provides a powerful tool for characterizing, separating, and assembling nanowires with desired properties into devices. Although Si NWs are used here, the ACMAN process is not limited and restricted by materials, and can be used to characterize, manipulate and assemble any other 1D nanomaterials. According to the device measurements (SI, Table S1), the FETs based on the integrated ACMAN scheme have demonstrated good performance characteristics, yielding high on-currents (ranging from 0.1 to 4.4 μA per nanowire), small sub-threshold swings (less than 1 V/dec) and high device mobilities (greater than 1 cm^2/Vs) assembled from the selected, high-conductivity Si NWs. The selected, high-conductivity Si NW FETs demonstrated significant performance improvement compared to that of the low-conductivity FETs, with two orders of magnitude higher on-current per nanowire, 16% to 33% lower sub-threshold swing, and up to 160 times higher mobility values. Therefore, the ACMAN strategy is able to discriminate, separate and assemble nanowire-based FETs with different electrical characteristics.

The ACMAN process enables the use of bottom-up grown nanowires that have been traditionally difficult to be characterized and integrated into devices. In particular, it has been reported that the number, diameter, and doping density of the nanowires incorporated into nanowire-FET devices strongly determine device performance⁴⁰. It has been shown that nanowires of the same composition and even from the same sample can exhibit highly variable properties, with nanowire conductivities varying by two or more orders of magnitude¹. The existing nanowire integration methods, such as directed assembly⁵⁹, contact printing⁶⁰, and DEP⁴⁷, are not capable of quantitatively and precisely characterizing and separating nanowires based on functional properties. In contrast, the ACMAN process enables quantitative selection of nanowires by electrical properties, and positions the desired number of nanowires to bridge the electrodes. Furthermore, compared with probe-based characterization and nanomanipulation methods^{38–41}, the ACMAN technique is much less costly, and more efficient and scalable.

Compared with the recent DEP-based assembly method^{52,53}, the ACMAN strategy has superior positioning and control performance for individual nanowires, but it might not be time efficient. While the DEP-based approach enables rapid separa-

tion and assembly of devices with large number of nanowires, the ACMAN technique is more suited for fabrication of nanodevices requiring fewer, finely selected and positioned nanowires. Such devices may include few or individual nanowire-based bio-probes/biosensors to interact with cells in biomedical applications. We note, however, that for devices with up to approximately 10^2 nanowires, the current ACMAN process is fast enough to no longer be the rate limiting step in the device fabrication; the conventional microfabrication steps for fabricating electrodes take longer than the nanowire sorting and assembly. Therefore, the ACMAN design complements and extends existing characterization and assembly techniques^{52,53} for nanodevice fabrication.

The overall performance of the ACMAN-fabricated FETs is consistent or better than the DEP-only devices described in the most related work^{52,53}, in which Si NWs are collected at various DEP frequencies and further assembled into FETs. In the reported work, the DEP-aligned NWs in the high frequency range (10 MHz and 20 MHz) are considered as high quality, as compared to those under the lower frequency range (30 Hz and 300 kHz)⁵³. The characteristics of the ACMAN FETs fabricated with the low-conductivity NWs are consistent with the measurements report for low-quality DEP-only FETs⁵³. Meanwhile, the highly conductive ACMAN FETs show superior on-current per nanowire and sub-threshold swing compared to the high quality (high-frequency collected) DEP-only FETs⁵³. The higher-conductivity Si-NW FETs in this work show at least $0.1 \mu\text{A}$ order on-current and less than 1.5 V/dec sub-threshold swing, compared to the at most $0.1 \mu\text{A}$ order on-current and greater than 2.1 V/dec sub-threshold swing reported for the high-quality FETs⁵³. However, the device mobilities of the fabricated FETs in this paper do not show similar performances as those in the previous results^{52,53}. This may be because of intrinsic differences in the MACE-grown Si NWs used here, while the VLS-grown Si nanowires used by other authors, or because of differences in NW surface states. The performance characteristics are highly dependent on surface states, and in the FET fabrication process, we did not passivate and post anneal due to the 220°C temperature limit for parylene C.

We note that the measurement results show device-to-device variation that could be affected by interface and process variations. In our experiments, the only sorting criterion is selected as the electrical conductivity threshold. The nanowires are characterized as higher or less electrical conductivities than the threshold and they are separately deposited at different locations. We did not select nanowires with the same electrical conductivities to deposit across different devices. Therefore, the uniformity across devices is not a sorting condition, and methods to calibrate the nanowire-FET-based sensors to suppress device-to-device variation are available for further development⁶¹. Thus, the automated ACMAN approach may provide a tool for future studies of device-to-device variations, and how to control them.

5 Conclusion

In this paper, we have presented the integrated ACMAN process, a strategy for automated characterization, separation and assembly of individual nanowires into functional nanodevices with desired properties. The ACMAN process combined contactless and

solution-based EOS for accurate nanowire characterization with EP-based motion control, planning and manipulation strategies to sort and manipulate multiple individual nanowires. Proof-of-concept Si-NW-based FETs were fabricated by separating and assembling Si NWs according to their electrical conductivities. The higher-conductivity Si NW-based FETs showed superior performance compared with their less conductive counterparts. The experiments confirmed the separation and assembly performance of the integrated ACMAN scheme.

In summary, the primary utility of the ACMAN approach lies in enabling the automated characterization and assembly of multiple individual nanowire with their desired electric properties. It can be used as an efficient and much less-costly substitute for tip-based characterization and assembly methods. It demonstrates superior separation performance than DEP-only methods. However, it is still challenging to work with large numbers of nanowires simultaneously using the ACMAN method, due to limited capacity of the electrodes to generate sufficiently independent electric fields for driving NWs, as well as the requirement for adequate spatial separation between nanowires to avoid chaining effects. We are currently designing and fabricating microfluidic devices with larger numbers of electrodes to test larger-scale simultaneous nanowire control. Developing systematic control methods to achieve time-optimal manipulation of multiple individual nanowires is also among the ongoing research tasks.

Conflicts of interest

There are no conflicts to declare.

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