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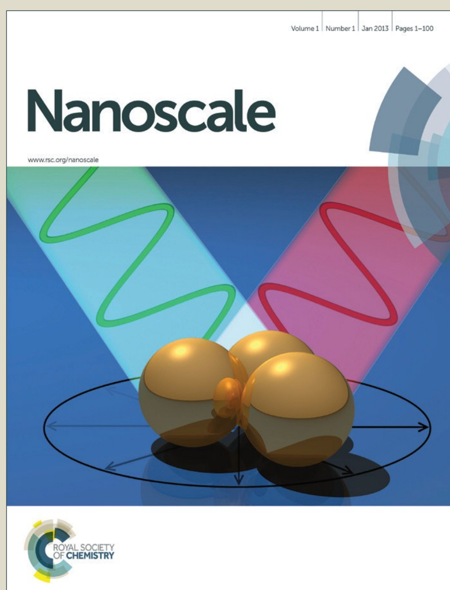

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ARTICLE

Super Nonlinear RRAM with Ultra-low Power for 3D Vertical Nano-Crossbar Array

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Vertical crossbar array provides a cost-effective approach for high density three-dimensional (3D) integration of resistive random access memory. However, individual selector device is not allowed to be integrated with memory cell separately. The development of V-RRAM has been impeded by lacking of satisfactory self-selective cell. In this work, we developed a high performance bilayer self-selective device by using HfO_2 as memory switching layer and mixed ionic and electron conductor as selective layer. The device exhibits high nonlinearity (>10^3) and ultra-low half-select leakage (<0.1 pA). A four layer vertical crossbar array was successfully demonstrated based on the developed self-selective device. High uniformity, ultra-low leakage, sub-nA operation, self-compliance, and excellent read/write disturbance immunity were achieved. The robust array level performance shows attractive potential for low power and high density 3D data storage applications.

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Introduction

Driven by continuous pursuit of reducing the fabrication cost of semiconductor memory, three dimensional (3D) integration is becoming a new paradigm considering the scaling route of planar two dimensional (2D) structure would be ended by the physical limitation. The crossbar array, with the memory cells located at the cross-point of perpendicularly placed parallel wordlines (WLs) and bitlines (BLs), is a sensible architecture for 3D integration, especially for the two-terminal devices, such as resistive switching random access memory (RRAM)[1-7]. One of the virtues of crossbar is, that it can ideally offer the smallest footprint of cell size $4F^2$ (F is the feature size) [8]. However, the crossbar structure has a serious concern called the sneaking current issue. Taking a 2x2 array as an example, if the three neighbor cells are at low-resistance state (LRS), whatever the state of designated cell is, its readout state will always be LRS, resulting in reading error or cross talk (**Fig. S1**). The larger array size is, the more serious cross talk will be. In order to inhibit the sneaking current from the unselected cells, integrating individual selector or developing self-selective cell (SSC) is necessary.

The 3D integration of crossbar can either be stacked layer by layer[8-11] or vertically placed[12, 13]. The former can easily be realized by duplicating the planar crossbar array in vertical direction. Integrating separate selector device with each memory cell is allowed in this structure (**Fig. S2**). It thus has sufficient margin to individually optimize the performance of selector and memory cell. The latter, also known as vertical RRAM (V-RRAM), is similar to bit-cost-scalable vertical NAND in the integration manner[14]. The most advantageous feature of V-RRAM compared with stacked crossbar array is the reduction of lithography steps, which helps to significantly lower the fabrication cost[15, 16]. However, in V-RRAM, it is impossible to integrate individual selectors with the corresponding memory cells (**Fig. S2**). The intermediate electrode would shorten the cells in the same column, leaving behind the self-selective cell (SSC) as the only choice to prohibit the sneaking current[17]. Various self-selective cells have been developed, such as self-rectifying device[18, 19], build-in nonlinear RRAM (BNR)[20-26], back-to-back stacked complimentary switching device[27], among which the build-in nonlinear RRAM is more preferable than others to configure V-RRAM array, owing to its lower power consumption on the unselected cells by using V/2 bias scheme.

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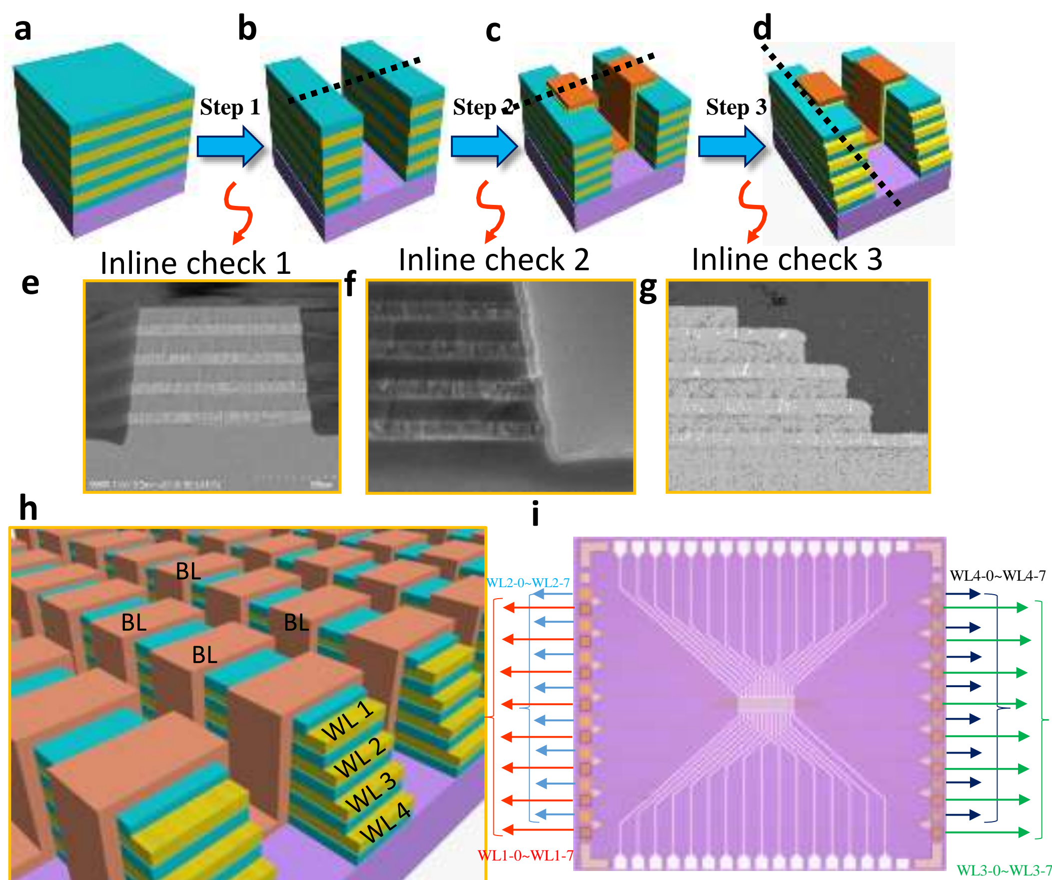

Fig.1 (a) to (d) The fabrication process of the 3D V-RRAM; (e) to (g) The inline check at each step of the process flow. The cut direction of the inline check is shown in (b) to (d) as a black line. ; h) the schematic view of 4-layers 3D V-RRAM array; i) the optical image of the 4×8×32 3D V-

There are several key requirements that an ideal build-in nonlinear RRAM device should meet, including high selectivity, low off-state leakage and self-compliance. The nonlinearity, defined as the ratio of $I_{@Vread}/I_{@Vread/2}$ is helpful to diminish the sneak current from undesignated cells. The difficulty of designing a cell with high nonlinearity underlines how to keep the $I_{@Vread/2}$ (leakage) as low as possible. The high leakage will not only degrade the nonlinearity of devices, but also increase the power consumption of the entire array. Lee et al. proposed a TiO_2/HfO_2 bilayer device with nonlinear low resistance state (LRS) benefiting from the introduction of TiO_2 tunneling layer[20]. Caused by the large leakage current, nonlinearity of only 5 was obtained. By incorporating metal-insulator transition (MIT) materials such as NbO_2, TiO_x, or VO_x, hybrid build-in nonlinear RRAM device with bilayer structure[21-23], have successfully enhanced the nonlinearity up to 100, but the leakage currents were still as high as μA level. Yang et al. proposed a RRAM device with bulid-in nonlinearity by inserting a functionalized graphene interface layer and Wang et al. reported a self-selective cell device with nanoporous Ta_2O_{5-x} material[24-26]. However, these prototype self-selective cell devices also suffer from the large leakage current and only exhibit modest nonlinearity. The lacking of an ideal self-selective cell has greatly retarded the progress of V-RRAM towards commercialization. Thus, there is an urgent demand on developing applicable approaches to realize a favorable self-selective cell.

In this work, we proposed a rational strategy on designing Super Nonlinear RRAM (SNR) device to tackle the sneaking current issue in large size V-RRAM array. The key component of the idea is to configure a material system that can provide high nonlinearity, low leakage current and self-compliance characteristics by combining HfO_2 layer and mixed ionic and electron conductor (MIEC) layer. The HfO_2 material is considered as a promising material with outstanding switching performance [27], and the Cu-containing MIEC, such as CuGeS, exhibiting threshold switching behavior in both polarity with high nonlinearity and low off state leakage [29-35], acts as a good candidate for selector device. The hereinafter developed bilayer Super Nonlinear RRAM device with sidewall configuration shows ultra-low leakage current (0.1 pA) and extremely high nonlinearity (~1000), which is a record of build-in nonlinear RRAM device so far. We have successfully demonstrated a 4-layer 8×32 V-RRAM 3D array using this Super Nonlinear RRAM device as a first attempt. Outstanding array level performance and robust disturbance immunity were achieved.

Experimental

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First, multiple TiN (60nm)/ SiO_2 (100nm) layers were deposited by PVD and PECVD, respectively. Patterning and only one-step etching were applied to form stacked wordlines (WL) with smooth sidewall profile. HfO_2/CuGeS bilayer with various thicknesses and the top electrode W(70 nm) with different size (from 2 μm to 10 μm) were deposited on the sidewall sequentially by magnetron sputtering at room temperature, followed by lift-off process to form bitlines (BL). Each horizontal WL was opened by selective etching successively. The area of the memory cell was defined by the thickness of bottom electrode TiN and the width of the lateral BL width.

the top electrode (or BLs) were deposited sequentially on the sidewall by magnetron sputtering at room temperature, then patterned by lift-off process in one step (Fig. 1f). Meanwhile, devices with single HfO_2 layer and single CuGeS layer were also prepared as control samples. The cell size was actually defined by the thickness of bottom electrode TiN and the lateral width of BL (2~10 μm). Each horizontal WL was finally opened by successively selective etching. Staircase WL contacts on each layer are shown in Fig. 1g. Fig. 1h shows the architecture of the 4 layer 8×32 3D V-RRAM array with its optical image shown in Fig. 1i after fabrication.

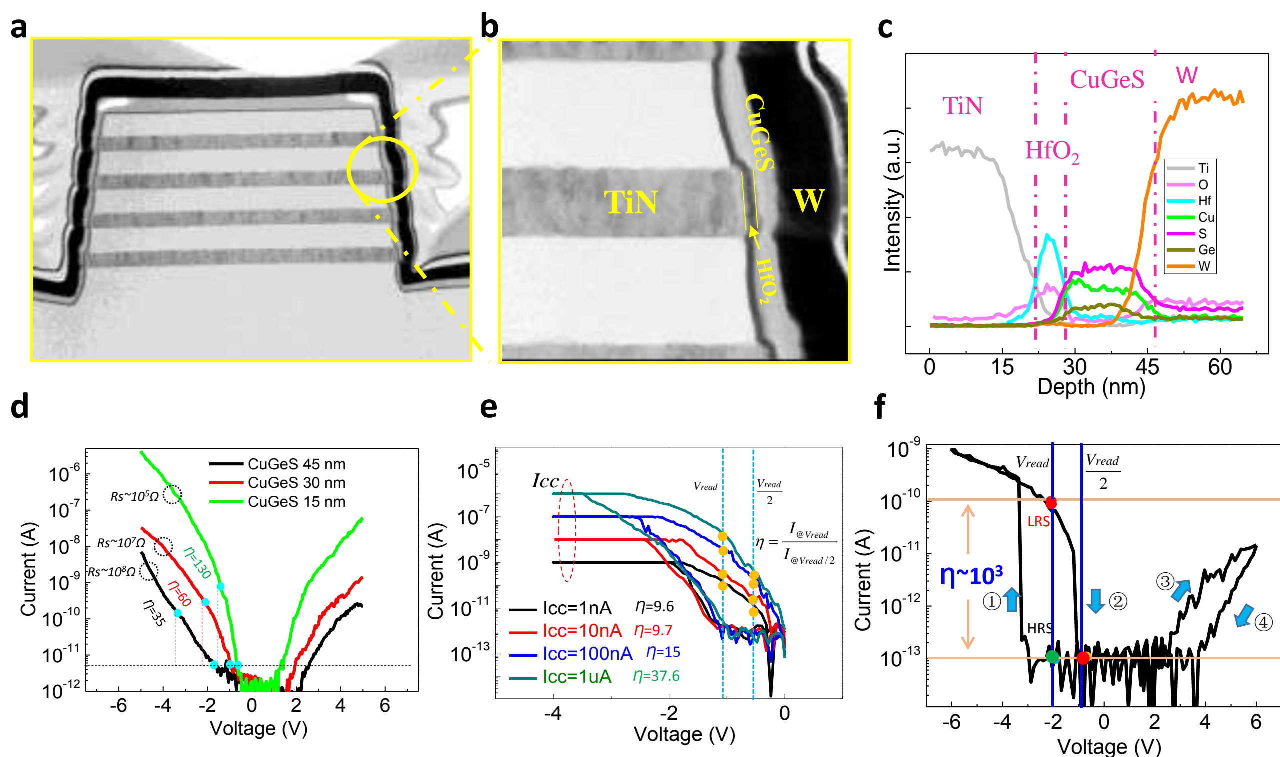

Fig. 2 (a) to (b) TEM image of the 4-layers structure and the TiN/HfO2/CuGeS/W cross-section of the BNR device. (c) EDX line scan over the TiN/HfO2/CuGeS/W cross-section of the BNR device. (d) I-V curves of single CuGeS devices. (e) I-V curves of single HfO2 devices. (f) Typical I-V curve of bilayer BNR device. Outstanding characteristics of high selectivity, low operation current, self- compliance and low leakage current were obtained.

RESULTS AND DISSUSSION:

A vertical integration scheme to build RRAM device with sidewall configuration-the same structure implemented in actual 3D V-RRAM array was developed [36]. Fig. 1a to 1d show the schematic process flow of V-RRAM integration. Multiple TiN (60 nm)/SiO_2 (100 nm) layers were first deposited by PVD and PECVD, alternatingly, followed with patterning and one-step etching to form stacked WLs. Note that the profile of the sidewall should be kept as smooth as possible, in order to avoid the coverage issue during subsequent material deposition and point discharge problem during programming. From the inline check shown in Fig. 1e, smooth sidewall profile was accomplished, owing to the careful control of etching process in this work. After that, the HfO_2/CuGeS bilayer and

Fig. 2a and 2b show the transmission electron microscopy (TEM) image of the cross-section of TiN/HfO_2/CuGeS/W bilayer device and its enlarged magnification, respectively. Well-distinguishable layers with clearly interface could be observed. The element analysis on the chemical composition of material stack was performed by the energy dispersive X-ray (EDX) spectrum obtained from the line scan starting from the TiN electrode to W electrode, as shown in Fig. 2c. Small amount of O signal overlapped with Ti signal was observed on the interface between TiN electrode and HfO_2 layer, indicating the surface of TiN electrode was weakly oxidized during the deposition of HfO_2 material, in accordance with the TEM image in Fig. 2b. It should be noticed that the Cu ions are not uniformly distributed in the CuGeS layer (seen from the Cu signal indicated by solid green line), with more enhanced

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intensity on interface than that in body, implying Cu ions tend to accumulate at the interface. This result is well consistent with the results reported in Padilla's work[37] , where the metal ions of MIEC material are found with a U shape distribution in a metal-MIEC-metal structure at zero bias, with higher concentration on the interface than in the center. This is a natural phenomenon of ion motion in order to keep a dynamic equilibrium between electrostatic ions drifting and diffusion. In this case, the CuGeS layer is deposited on top of HfO_2 layer, where the negative charged traps such as Hf vacancies or non-lattice O ions can be easily generated during sputtering deposition[38]. These negative charged traps attract the positively charged Cu ions in CuGeS layer and enhance their accumulation at the interface. As will discussed later, this accumulation effect is helpful to enhance the nonlinear characteristics of the bilayer device.

Gopalakrishnan[30]. As long as the applied voltage reaches a certain value, the resistance of the device will be reduced dramatically, resulting in an extremely nonlinear I-V characteristics. The switching voltage is increased with the thickness of CuGeS layer, indicating the switching effect is mainly induced by the electric field. The working principle of the behavior observed in the MIEC device can be interpreted by the modulation of electronic current by the motion of Cu ions. Based on the Hall Effect measurement[35], the MIEC material was found to be a p type semiconductor. At low voltage bias, the hole carriers are suppressed by the space charge depletion layer resulting from the interface ions accumulation. In contrast, at high voltage bias, the barrier could be lowered after moving the Cu ions away from the interface and rapid increase of the hole conductivity emerges. The resistance at high voltage bias is determined by hole

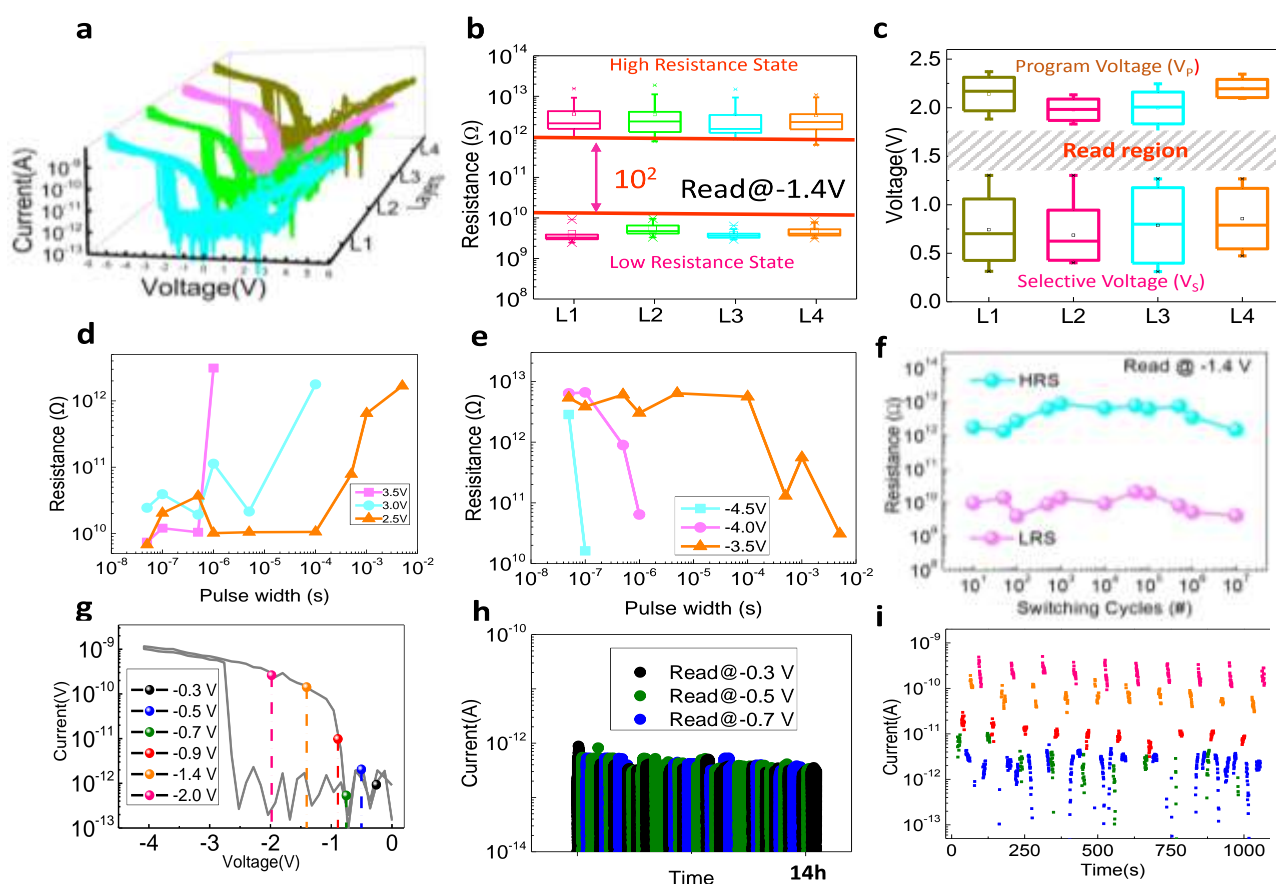

Fig. 3 (a) The distribution of I-V curves in the 4-layer 8×32 arrays; (b) Resistance distributions of BNR devices in 4 layers array; (c) Voltage distributions of BNR devices in 4 layers array; (d) The dependence of switching time on pulse height for reset opration; (e) The dependence of switching time on pulse height for set opration; (f) The endurance of bilayer self-selective cell with more than 10^6 cycles; (g) The scheme of the leakage test voltage, different bias voltage was discribed by different colour; (h) Low-leakage exposure over hours in deep (-0.3V)/shallow (-0.5V) un-select and half-select (-0.7 V) conditions; (i) Repeated exposure to select (-1.4 V), over select (-2V), half-select (-0.7 V) and deep (-0.3V)/shallow (-0.5V) un-select.

Fig. 2d shows the typical I-V curves of TiN/CuGeS/W samples with different CuGeS thickness. During the test, the W electrode was forced by voltage bias while the TiN electrode was kept at ground. The single CuGeS layer devices show switching effect, analogous to the results reported by K.

tunneling and the bulk limitation of CuGeS layer, which is closely related to its thickness. As can be seen in Fig. 2d, the resistance values of the device with 45 nm, 30 nm and 15 nm CuGeS after switching are about 10^8 Ω, 10^7 Ω and 10^5 Ω, respectively. The nonlinearity of each device is also dependent

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on the CuGeS thickness. As shown in Fig. 2d, the 15 nm, 30 nm and 45 nm devices have corresponding nonlinearities of 130, 60 and 35. This is a natural result since the nonlinearity is defined as a ratio of the current read at V and V/2. Lower on-state current could result in lower nonlinearity.

Fig. 2e shows the I-V curve of resistive switching of single HfO_2 layer device, by applying voltage bias on TiN electrode for SET and applying voltage bias on W electrode for RESET. Ultra-low compliance currents of sub μA were adopted during the measurement. Reliable multi-level storage with stable retention and good endurance was demonstrated in Fig. S3. In such low operation current region, continuous conductive filament of oxygen vacancies is impossible to emerge, considering the maximum resistance of one atom point contact is only around 13 kΩ[39]. In other words, other conduction mechanisms such as trap assistant tunneling should be dominant for the LRS with higher resistance. It should be noted that modest nonlinearity was observed in the single HfO_2 layer devices, depending on the value of compliance current. A maximum value of 37.6 was obtained under a compliance current of 1 μA. By setting higher compliance current, the nonlinearity is diminished and finally disappears as soon as the continuous filament is formed. Compared with other reported nonlinearity data concerning single HfO_2 layer device[40, 41], the one presented here is much higher. The possible reason could be attributed to the existence of a TiO_2 interfacial layer, as indicated by the element analysis of EDX line scan measurement. The tunneling conduction across the TiO_2 layer is helpful to increase device nonlinearity[42]. The weak dependence of the LRS current on temperature (Fig. S4) suggests that the conduction in LRS is dominated by electron tunneling, analogous to the results reported by Shimeng Yu [43].

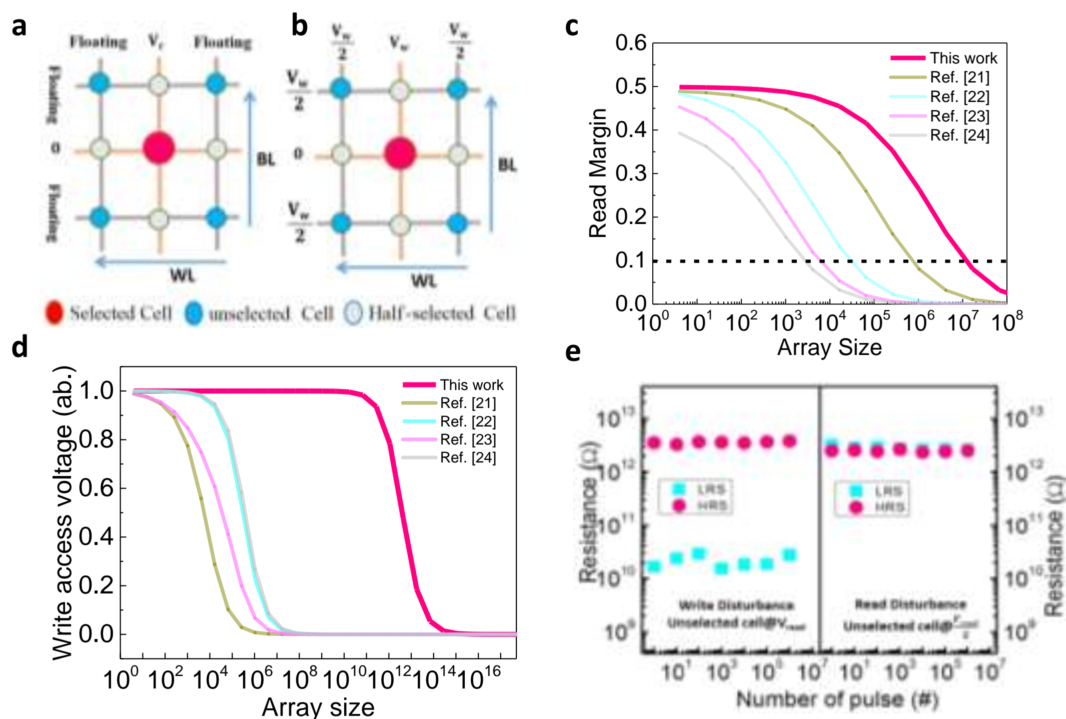

Fig. 4 (a) Worst case bias scheme in read operation; (b) V/2 bias scheme for read and write. (c) Write access voltage analysis; (d) Read margin analysis in the worst case condition. (e) Write and Read disturbance measurement in the vertical array.

Fig. 2f shows the I-V curve of bilayer device composed by the HfO_2 layer and CuGeS layer. The sequence of voltage sweeping denoted as the numbered blue arrows is the same as that applied on single layer control samples. The switching from off-state to on-state appears during the voltage sweeping from 0 V to -6 V with a voltage around -3.5 V (denoted as programming voltage, V_p). Noteworthy, during the backwards sweeping from -6 V to 0 V, the on-state becomes highly insulative at a point around -1 V (denoted as selective voltage, V_s). This behavior is quite similar to the one observed in threshold switching device, featuring resistive switching at a switching voltage and resistance recovery at a holding voltage. The difference between the switching characteristics of HfO_2/CuGeS bilayer device with other threshold device is that the former has memory effect, whereas the later does not. At each switching cycle, the threshold device turns on at the switching voltage and recover to off-state at the holding point. As for the HfO_2/CuGeS bilayer device, the I-V curve of the 2nd voltage sweeping from 0 V to -6 V (displayed in Fig. S5) reveals that the switching point of the device after previous 0 V to -6 V programming is nearby V_s, rather than V_p. Once the device undergoes a RESET process with positive voltage sweeping (from 0 V→6 V→0 V), as indicated by the 3rd and 4th arrows in Fig. 2f, the switching point could be shifted back to V_p again. That is to say, memory effect exists in the bilayer HfO_2/CuGeS

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device, whose LRS moreover, exhibits high nonlinear characteristics. Given a reading voltage of -2 V and half reading voltage of -1 V, the leakage current at $V_{read}/2$ is as low as 0.1 pA (limited by the tester). The selectivity in this case would be as high as 10^3. The high nonlinearity observed in this device offers a possible way to solve the sneaking current issue in 3D V-RRAM array. It should be noted that the voltage sweeping loop of 0 V→6 V→0 V does not mean the device need +6V for RESET. Actually, +2V is enough to RESET the device into HRS (subsequent pulse test result verify this conclusion).

One may ask why the bilayer device has such high nonlinearity, whereas the single HfO_2 device and CuGeS devices only have modest ones. The possible reason may lie in the interface property of the HfO_2 and CuGeS layer. As pointed out by aforementioned EDX result, the Cu ions in the CuGeS layer are accumulated on the interface adjacent to the HfO_2 layer. An enhanced space charge depletion layer could be expected in the bilayer device. With such an interface property, the ultra-low leakage current and increased switching voltage observed in the bilayer device are reasonable. The ultra-low leakage current effectively increases the nonlinearity of the device, in spite of the nA level operation current. Based on the above results, the working principle of the bilayer device could be qualitatively interpreted by the modulation of interface space charge depletion layer. Fig.S6 shows the proposed mechanism of the device. At low voltage, much of the voltage will apply on the enhanced depletion layer and the current remains low (Fig.S6a).Under certain external voltage (e. g V_p), this depletion region could be narrowed by driving the Cu ions away from the interface(Fig. S6b), making the carriers conducting easier and thus increasing the device conductivity dramatically. When the applied voltage falls below a certain value, such as V_s, the conducting of the carrier is prevented by the interface barrier, making the device highly insulative in low voltage region. The current flow though the device after switching is limited by the bulk resistance of CuGeS, which makes the device with self-compliance. In common sense, the memory cell in passive crossbar array is incapable of providing current compliance to protect the cell from over programming. Additional transistors need to be placed beside the array either in rows or in columns, which will not only increase the expense of silicon space, but also complicate the peripheral circuitry design. The self-compliant characteristics observed in the bilayer build-in nonlinear RRAM device offers a feasibility to reduce to concerns on the circuitry designing of compliance current. In additional, the RESET current of the build-in nonlinear RRAM device could be observed as low as 10 pA in Fig. 2f**,** showing high potential to configure a memory system with low power consumption and high energy efficiency.

In order to evaluate the array level performance of the build-in nonlinear RRAM device, statistical measurement was carried out on 4×8×32 3D array**.** Fig. 3a shows the I-V curves of the cells in 4-layers crossbar array, where stable bipolar switching characteristics are clearly observed. The corresponding resistance distributions of HRS and LRS read at -1.4 V are illustrated in Fig. 3b, showing good uniformity with the notably on/off ratio (≈100 times). Fig. 3c displays the distributions of V_p and V_s. The former one spreads in a range from -1.75 V to -2.25 V while the later one varies between -0.7 V and -1.25 V. After precluding the variation, there is still enough voltage window of 0.5 V guaranteed for the successful read operation. Fig. 3d and 3e show the dependence of switching speed on pulse amplitudes for SET and RESET operations, respectively. Higher programming voltage corresponds to shorter switching time. Fig. 3f shows the endurance test result under successive voltage pulses with -4 V/ 1μs for SET and 4 V/500 ns for RESET. After 10^7 cycles, the on/off state ratio read by -1.4 V voltage pulse can still be well maintained. Both HRS and LRS show good non-volatility and stability, confirmed by retention test over 10000 s (shown in Fig. S7). Fig S8 shows that a 10000s data retention time can be obtained at 85℃ and 125℃. To evaluate the stability of leakage current of the bilayer device in array during operation, long time voltage bias and recoverable leakage current after voltage stress were tested. Fig. 3h shows the leakage current in deep (-0.3 V)/shallow (-0.5V) un-selected and half-selected (-0.7 V) conditions. The measured voltages were represented by different color dots as shown in Fig. 3g. After hours of exposure in deep (-0.3 V)/shallow (-0.5 V) un-select and half-select (-0.7 V) voltages, the bilayer build-in nonlinear RRAM device can still maintain low leakage current. Repeated exposure under the select (-1.4 V, t>15 s) and half-select (-0.7 V, t>15 s) conditions show no appreciable effect on the recovered leakage. The ultra-low leakage current can be maintained even after the exposure under higher voltages (-1.4 V and -2V), indicating stable leakage current and robust nonlinearity (Fig. 3i). These aforementioned results suggest that the bilayer device has excellent memory performance and outstanding self-selective characteristics.

To confirm the large-scale feasibility, read and write margins were analyzed based on the device specifications. Fig. 4a shows the worst case of reading with only one BL pulled up and all unselected cells at LRS, and Fig. 4b shows the well-known V/2 bias scheme for the read and write operation. The equivalent circuit for calculating sense margin could be found in the supplementary information (Fig. S9). Owing to its high nonlinearity and on/off ratio, a sufficient read margin (10%) can be obtained up to 10 Mb array in the worst case condition, as shown in Fig. 4c. Fig. 4d shows write access voltage analysis in consideration of voltage drop on the BLs. The resistivity of metal lines is increased dramatically as the line width approaching nm region[36]. Thanks to the large cell resistance, the interconnect resistance has negligible effects on the voltage drop before the array size reaching 100 Gb, which guarantees sufficient write margin easily achievable in large arrays. The read/write disturbance in crossbar array is another important issue of concern. During read/write operations, the unselected cells at the same row or column of the selected cell suffer from $V_{read}/2$ and $V_{write}/2$ voltage stresses. The disturbance immunity during read and write operation is evaluated by measuring the stability of cells in half-selected row or column. During write operation, the typical write voltage is around -4 V. In this case, the half-selected cell will suffer -2 V voltage stress. As shown in Fig. 4e, after 10^6 switching cycles, neither of the HRS and LRS of the half-

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selected cells was degraded. During read operation, the read voltage is typically of 1.4 V. The half-selected cells will suffer 0.7 V voltage stress, which is below the selective voltage of the build-in nonlinear RRAM device and only the leakage current could be detected, regardless of HRS or LRS states. As shown in Fig. 4e, after 10^6 read cycles, the low leakage current can be well maintained. These results imply the build-in nonlinear RRAM devices possess excellent read/write disturbance immunity in array operation.

Conclusions

In summary, we have successfully demonstrated a bilayer build-in nonlinear RRAM device hybridly composed by HfO_2 memory switching layer and MIEC threshold switching layer, as a method to solve the well-known sneaking current issue in V-RRAM array, where separate selector device is not allowed. Promising self-selective characteristics such as extremely high nonlinearity (10^3), ultra-low leakage current (0.1 pA) and self-compliance were achieved. Based on this build-in nonlinear RRAM device, a 4-layer vertical crossbar array was successfully developed as a first attempt, showing outstanding read/write disturbance immunity and high uniformity. The good compatibility of this vertical integration scheme with CMOS platform could easily extend the array size into large scale, thus paving a new way to make a Tera bit scale V-RRAM array with low cost, low power consumption and self-selectivity into reality.

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