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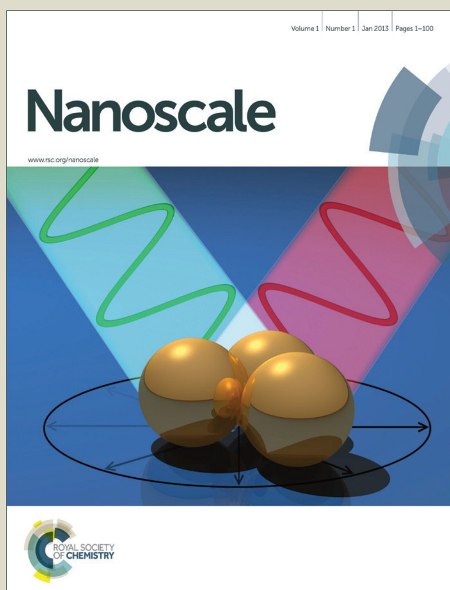

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ARTICLE TYPE

Ultralow Power Complementary Inverter Circuits Using Axially Doped p- and n-channel Si Nanowire Field Effect Transistors

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We successfully synthesized axially doped p- and n-type regions on a single Si nanowire (NW). Diode and complementary metal-oxide-semiconductor (CMOS) inverter devices using single axial p- and n-channel Si NW field-effect transistors (FETs) were fabricated. We show that the threshold voltages of both p- and n-channel Si NW FETs can be lowered to nearly zero by effectively controlling the doping concentration. Because of the high performance of the p- and n-type Si NW channel FETs, especially with regard to the low threshold voltage, the fabricated NW CMOS inverters have a low operating voltage (<3 V) while maintaining a high voltage gain (~6) and ultralow static power dissipation (≤0.3 pW) at an input voltage of ±3 V. This result offers a viable way to fabricate a high-performance high-density logic circuit using a low-temperature fabrication process, which makes it suitable for flexible electronics.

1. Introduction

Complementary metal–oxide–semiconductor (CMOS) inverter devices involving both p- and n-type field-effect transistors (FETs) are among the most common building blocks in logic circuit designs.[1] The current downscaling of mainstream Si CMOS technology has increased the speed of logic circuits. However, it has also increased the dissipated power. Moreover, the current top-down miniaturization trend is expected to reach fundamental physical limits soon, motivating the development of new device structures as well as functional materials to be implemented in nanoscale electronic devices.[2–5]

In particular, one-dimensional nanostructures such as nanowires (NWs), carbon nanotubes (CNTs), and graphene nanoribbons are promising candidates for conducting channels in FETs owing to their fascinating electrical transport properties and consequent application potential to overcome the technical and physical limitations encountered by traditional lithography-based thin-film transistors (TFTs).[6–8]

The superior carrier mobility and small size of CNTs and graphene ribbons have been exploited to surpass Si in terms of the operation speed in logic device applications. Despite advances in these materials, a large gap still exists between the status of CNT- and graphene-nanoribbon-based FETs and industrial application requirements.[9–12] Therefore, Si NWs have been intensively investigated by many research groups as a replacement for standard CMOS-based TFT technology.[3,4,13] In particular, Si nanowires containing p-n junctions are fundamental building blocks for CMOS device applications. Different methods of synthesizing an axially doped p-n junction on a single Si NW have been reported, but currently the applications in which they are implemented, such as photovoltaics[14–17] and tunnelling transistors,[18] are based on p-n junction diodes. The transport properties of the n- and p-type FETs that make up a CMOS inverter must be compatible. Single n- and p-type NW devices for logic circuits have been reported.[19,20] Owing to the difficulty of controlling the transport properties of each part of the axial p-n Si NWs in previous reports, a CMOS inverter based on an axial p-n Si NW has not been demonstrated.[18,21,22]

In this communication, we first present a simple method of synthesizing highly ordered axially doped p- and n-type regions on a single Si NW, where the transport properties of each p- and n-type region can be modulated by effectively controlling the doping concentration. A p-n junction diode and CMOS inverter, each of which can be selectively fabricated on a single Si NW, are then measured, and the results are analysed and discussed. The inverter devices exhibit high performance characteristics, a low operating voltage, and low static power dissipation, making them suitable for high-density, high-performance, and flexible[23-25] logic device applications.

2. Experimental

Synthesis of axially doped p- and n-type regions on a single Si NW and removal of the radial growth layer: The processes used to synthesize axially doped p- and n-type regions on a single Si NW and to remove the radial growth layer are shown in Fig. 1. The p-n Si NWs were grown on (100) Si substrates by a vapour-liquid-solid method catalysed by 40-nm Au nanoclusters in a low-pressure chemical vapour deposition (CVD) reactor, as reported in detail by Koo *et al.*[14] First, 20-µm-long p-type Si NWs were nucleated and grown with Au tips for 20 min. Boron was introduced as a p-type dopant directly during growth with a silane (SiH_4)/diborane (B_2H_6) gas ratio maintained at 5,500:1. When p-type growth was completed, an n-type dopant gas was introduced by switching from B_2H_6 to phosphine (PH_3) and

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maintaining the SiH_4/PH_3 gas ratio at 4,500:1. Phosphorus-doped n-type Si NWs

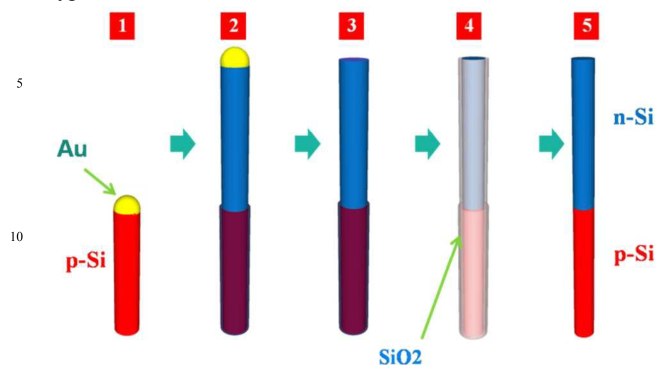

Fig.1 Synthesis of axially doped p- and n-type regions on a single Si NW, and removal of the radial growth layer. (1) Growth of the p-type Si NW, (2) growth of the n-type Si NW on top of the p-type Si NW, (3) etching of the Au catalyst, (4) thermal oxidation of the Si NW, (5) etching of the oxide shell.

20 μm in length were subsequently grown from the ends of the p-type Si NWs with Au tips for 30 min. Both vertical growth of n-type Si NWs on top of the p-type Si NWs and radial growth of an n-type shell layer on the p-type region of each Si NW were observed.

To expose the p-type region, the n-type shell grown on the p-type region was removed by thermal oxidation of the shell and subsequent chemical etching of the oxide. After CVD growth, the substrate with the p-n Si NWs was dipped in a solution of potassium iodide and iodine (KI/I_2) to remove the Au tips. After the Au residue was removed, the NWs were thermally oxidized in a furnace at 800 °C for 15 min in air and then cleaned in oxygen plasma (50 W, 0.3 Torr, O_2 100 sccm, 300 s). Finally, the formed oxide shell was removed in 10% hydrofluoric acid for ~30 s until the surface of the substrate became hydrophobic.

To optimize the operating voltage of the CMOS inverter based on the p-n Si NW, the doping concentrations of both the p- and n-type regions were varied. The SiH_4/PH_3 gas ratio was varied from 3,000:1 to 6,000:1 for the n-type Si region, whereas the SiH_4/B_2H_6 gas ratio was varied from 3,500:1 to 6,500:1 for the p-type Si region.

Fabrication and measurement of p-n junction diode and CMOS inverter based on axial p-n Si NWs: Single-crystalline axially doped p-n Si NWs with a typical diameter of 45–55 nm (after removal of the n-type radial growth layer on the p-type region) were first dispersed via ultrasonication in isopropanol; a drop of the liquid suspension of the Si NWs was then transferred to a silicon substrate using a pipette. A heavily doped p-type Si substrate (0.005 Ωcm) was employed as a back gate with a 100-nm-thick, thermally oxidized SiO_2 top layer as a gate oxide layer. Multiple electrodes were patterned on the NW by a conventional

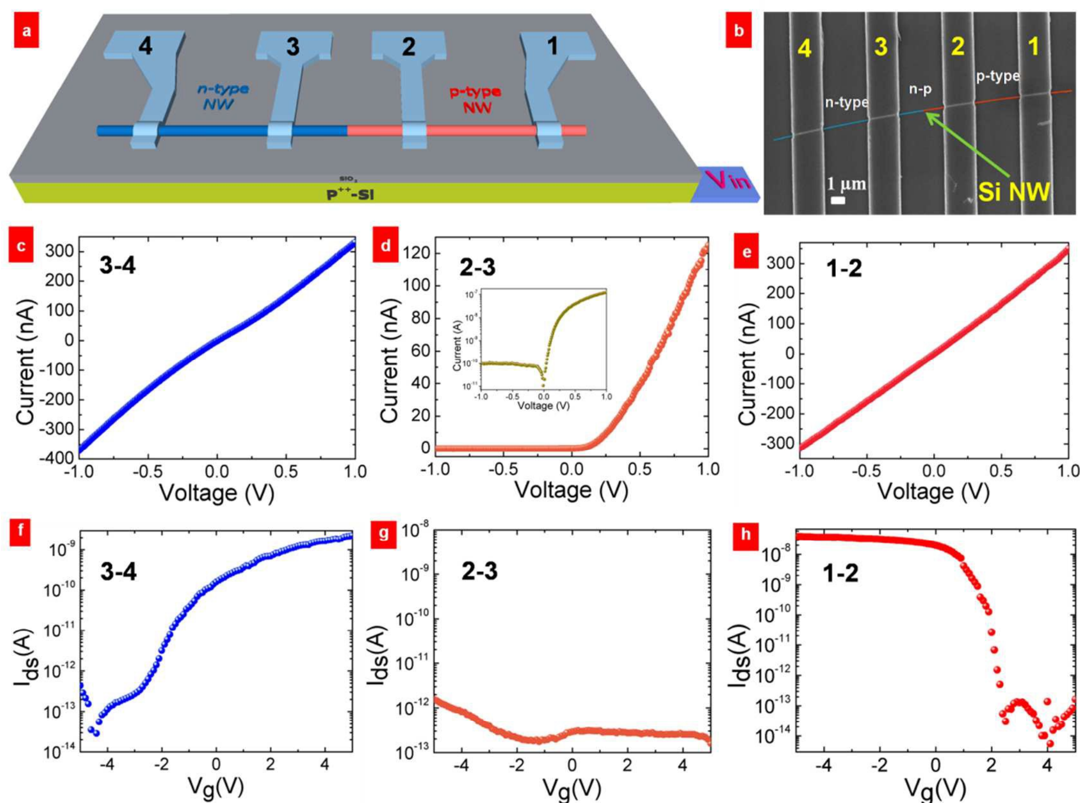

Fig. 2 Schematic drawing, scanning electron microscope (SEM) image, and electrical characteristics of the p-n Si NW device. (a) Schematic drawing of the axially doped p-n Si NW device. (b) SEM image of the p-n Si NW in the device configuration. Current–voltage (I_{ds}–V_{ds}) characteristics measured (c) between two contacts in the n-type region, (d) across the p-n diode region, Inset shows the p-n junction diode in log scale, and (e) between two contacts in the p-type region, all with a back-gate voltage of V_g = 0 V. Transfer characteristics (I_{ds}–V_g) at V_{ds} = 0.1 V (f) in the n-type region, (g) across the p-n region, and (h) in the p-type region.

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photolithography process. Before deposition of the metal electrodes, the samples were immersed in a buffered 1% hydrofluoric acid solution for 15 s to remove the native oxide layer that formed on the surface of the Si NWs during processing.[14] The contact electrodes were subsequently deposited by electron-beam evaporation as follows to form ohmic contacts: a 20-nm-thick nickel–chrome layer (NiCr; 80% Ni and 20% Cr) was first evaporated, followed by an 80-nm-thick Au layer. The electrical characteristics of the devices were measured in air using a probe station with a Keithley SCS-4200 system.

Synthesis of n- and p-type Si NWs: The n- and p-type Si NWs used in this study were grown on Si (100) substrates with Au catalysts using a vapour-liquid-solid method, as reported in detail by T. Koo *et al.*[14]In this experiment, n- and p-type Si NWs were doped with phosphorus or boron directly during growth. The silane (SiH_4)/phosphine (PH_3) gas ratio was varied from 4,000:1 to 10,000:1 for n-type Si NWs, whereas the boron-doped p-type Si NWs were grown with a silane (SiH_4)/diborane (B_2H_6) gas ratio varied from 3,000:1 to 6,500:1.

the metal electrodes. It also proves that the rectifying diode characteristics (Fig. 2d), with the p-n junction diode ideality factor was calculated from log scale of inserted Fig.2d is 1.8, and near absence of gate effects in the transfer characteristics (Fig. 2g) measured between contacts 2 and 3 originate from the p-n junction rather than the Schottky characteristics of the metal–Si contacts. Moreover, the ambipolar gate effect was observed in Si NWs p-n junction diode when the forward bias voltage was set at 1 V, above the rectifying voltage of p-n junction diode (Fig. S1 in the Supplementary Information). The diode should work at ON state. Thus, the region close to the p–n junction exhibit a clear gate effect. [21]

To fabricate a CMOS inverter based on single p-n Si NW FETs, the position of the inverter output metal contact was adjusted to be over the p-n junction region. The operation of NW CMOS inverters was demonstrated in our previous report.[26] A larger threshold voltage requires a larger gate voltage for the device to function as an inverter. To use the CMOS NW as a low-operating-voltage inverter, the threshold voltages of the p- and n-

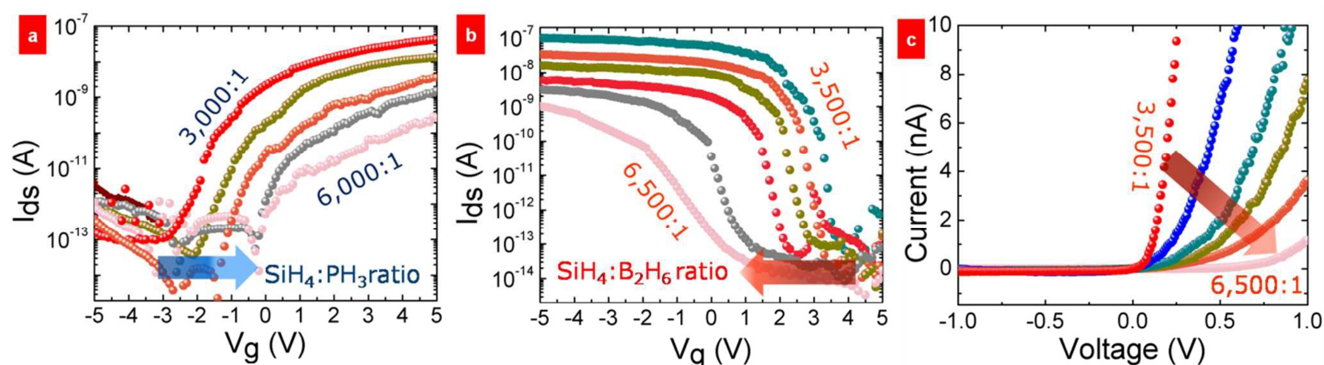

Fig. 3 Tunable threshold voltage and diode behavior at various doping concentrations. (a) I_{ds}–V_g transfer characteristics of the n-type region of the p-n Si NW FETs at different doping concentrations (SiH_4/PH_3 ratios of 3,000:1 to 6,000:1), showing a positive shift of the threshold voltage. (b) I_{ds}–V_g transfer characteristics of the p-type region of the p-n Si NW FETs at different doping concentrations (SiH_4/B_2H_6 gas ratios of 3,500:1 to 6,500:1), showing a positive shift of the threshold voltage. (c) Diode behavior at different doping concentrations.

3. Results and Discussion

The processes used to synthesize axially doped p- and n-type regions on a single Si NW (a p-n Si NW) and to remove the radial growth layer are shown in Fig. 1. The electrical characteristics of the diode based on a p-n Si NW were measured by four electrodes and a back gate, as shown in the schematic drawing in Fig. 2a. Because either the n- or p-type NW region in contact with metal electrodes could possibly show metal–Si Schottky contact diode characteristics, the positions of the metal contacts were adjusted so that the two contacts were positioned on each side of the p-n junction. For contacts 1 and 2, the linear current–voltage (I_{ds}–V_{ds}) characteristics (Fig. 2e) and back-gate transfer characteristics (I_{ds}–V_g) at V_{ds} = 0.1 V(Fig. 2h) were those of a p-type FET, whereas contacts 3 and 4 exhibited n-type FET characteristics (Fig. 2c,f). The linearity of these I_{ds}–V_{ds} characteristics suggests a low contact resistance and that an Ohmic contact forms between both the p- and n-type regions and

type regions should be shifted as close to 0 V as possible. Several schemes have been proposed to make n-type ZnO NW FETs operate in an enhancement mode by tuning the diameter and surface conditions of the ZnO NWs,[27–29] working with the electrode work functions,[30] or employing proton irradiation.[20] In this study, the threshold voltages of the p- and n-type regions of the Si NW are shifted negatively and positively, respectively, toward zero by changing the doping concentrations. The SiH_4/PH_3 gas ratios (i.e. the doping concentrations) were varied, and several FETs based on the p-n Si NWs were constructed; each region, p-type and n-type, was then measured extensively. The effects of the doping concentration on the conductance and threshold voltages of the p-n Si NW FETs are shown in Fig. 3a,b, respectively. The transfer characteristics, that is, the drain current versus gate-source voltage (I_{ds}–V_g), of several n-type regions of the Si NW FETs at different doping concentrations, were obtained by sweeping the gate voltage continuously from –5 to +5 V with a

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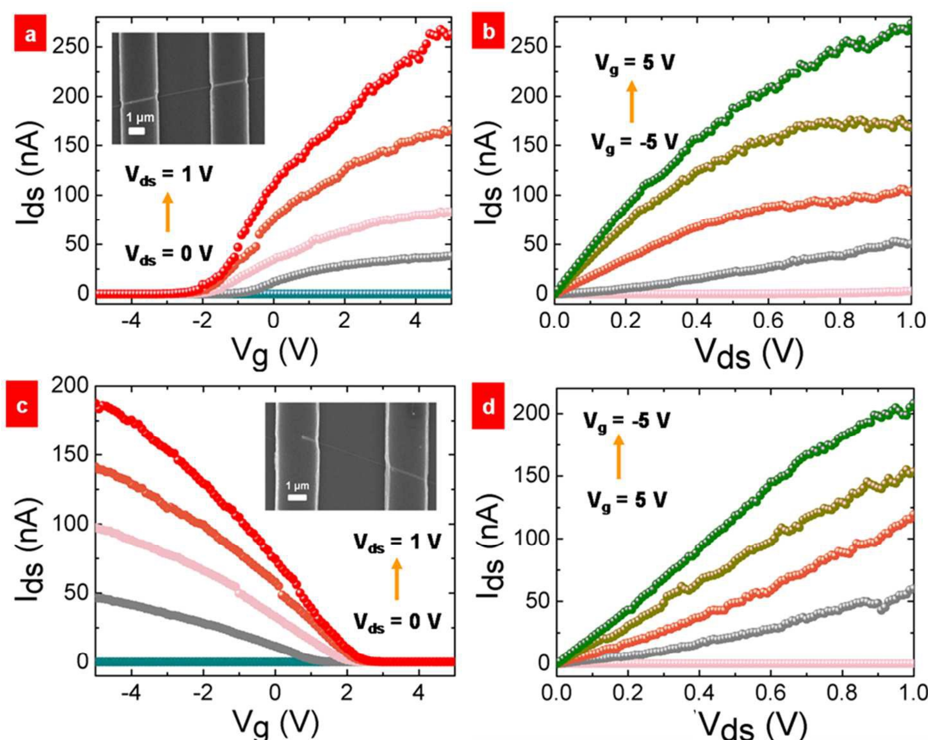

Fig. 4 Electrical transport properties of the p-n Si NW FETs under ambient conditions. (a and c) I_{ds}–V_g transfer characteristics and (b and d) I_{ds}–V_{ds} output characteristics of the n- and p-type regions of the p-n Si NW FETs, respectively.

drain voltage of 0.1 V. The negative threshold voltage shifted positively from approximately –3.5 V to close to –0.5 V as the doping concentration was reduced. The transconductance, electron mobility, subthreshold swing, and carrier concentration were estimated from the transfer characteristics. The average transconductance was estimated to be between 0.9 and 14.3 nS; the electron mobility ranged from 3.3 to 52.9 cm^2 V^{-1} s^{-1}, the subthreshold swing ranged from 83.5 to 248.8 mV dec^{-1}, and the electron carrier concentration ranged from 1.5 × 10^{17} to 1.1 × 10^{18} e cm^{-3} with an increasing doping concentration (SiH_4/PH_3gas ratio changing from 6,000:1 to 3,000:1). Additionally, the ON current reduced from 10^{-7} to 10^{-9} A when the electron carrier concentration was reduced by reducing the doping concentration. A similar approach was applied to the p-type regions of the p-n Si NW FETs. The I_{ds}–V_g characteristics of several p-type regions of the p-n Si NW FETs at different doping concentrations were obtained by sweeping the gate voltage continuously from +5 to –5 V. The positive threshold voltage shifted negatively from approximately +4 V to close to 1.5 V as the doping concentration was reduced by varying the SiH_4/B_2H_6 gas ratio. The average transconductance was estimated to be between 6.0 and 58.3 nS; the hole mobility ranged from 22.3 to 215.7 cm^2 V^{-1} s^{-1}, the subthreshold swing ranged from 108.4 to 217.9 mV dec^{-1}, and the hole carrier concentration ranged from 4.5 × 10^{17} to 1.2 × 10^{18} h cm^{-3}withan increasing doping concentration (SiH_4/B_2H_6gas ratio changing from 6,500:1 to 3,500:1). The ON current also increased from ~10^{-9} to 10^{-7} A (See Table S1 in the Supplementary Information). Note that the NW diameter did not vary with the doping concentration in either the p- or n-type regions.

A positive shift of the knee voltage of the p-n junction diode was also observed in this study, as shown in Fig. 3c. The knee voltage shifted from 0.15 to 0.8 V when the p-type region dopant was reduced (SiH_4/B_2H_6 gas ratio was changed from 3,500:1 to 6,500:1) and when the n-type region dopant was maintained at a 4,500:1 SiH_4/PH_3 gas ratio. The positive shift of the knee voltage is a result of the reduction in the carrier concentration in the p-type region that occurs when the doping concentration is reduced. This leads to a wider depletion region, so a higher forward voltage is required to overcome the barrier potential.

A schematic diagram of a simplified depletion model for the n-type region of Si NW FETs with different doping concentrations at a constant negative gate voltage was proposed by Van *et al.*[26] On the basis of the work of Hong *et al.*,[28] the electron carrier concentration (n_e) was calculated using the equation $n_e = C_{ox}(V_g–V_{th})/e\pi r^2L$, where C_{ox} is the gate oxide capacitance, L is the NW conducting channel length, and r is the NW radius. When the gate voltage is 0 V, this equation reveals that the threshold voltage of the n-type region of the p-n Si NW FETs is proportional to the carrier concentration. Furthermore, at a constant negative gate voltage, the lower electron density easily induces full depletion within the NW. Therefore, reducing the doping concentration leads to fewer electrons in the conducting n-type channel of the p-n Si NW FETs, resulting in reduced conductance and a positive shift in the threshold voltage. However, further reductions in the threshold voltage also degrade the performance (conductivity, transconductance, mobility, and

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I_{ON}/I_{OFF} ratio) of the FET. The transport properties of the n- and p-type FETs that make up a CMOS inverter must be compatible. Further, to maintain a sufficient I_{ON}/I_{OFF} ratio exceeding 10^5 and to achieve a high inverter gain in CMOS inverter devices based on p-n Si NWs, the doping concentration was optimized at a 4,500:1 SiH_4/PH_3 gas ratio, yielding a threshold voltage of approximately –2 V. A similar approach was applied to the p-type region of the p-n Si NW FETs; the optimized doping concentration was achieved at a 5,500:1 SiH_4/B_2H_6 ratio, resulting in a threshold voltage of ~2.5 V.

V. The field-effect electron mobility (μ_e) and resistivity (ρ) for the p-n Si NWs were calculated from four-probe measurements and found to be 39.9 $cm^2\ V^{-1}\ s^{-1}$ and 0.18 Ωcm, respectively (Fig. S2c in the Supporting Information). The electron carrier concentration (n_e) was calculated to be 6.0 × 10^{17} e cm^{-3} using the equation $n_e = C_{ox}V_{th}/e\pi r^2L$.[27] The subthreshold swing, given by $S = \log[dV_g/d(\log I_{ds})]$, was estimated to be 181.9 V dec^{-1}. The same calculation method is applicable to the p-type regions of the p-n Si NW FETs. A V_{th} of 2.5 V, g_m of 142.4 nS, and field-effect hole mobility (μ_h) of 52.6

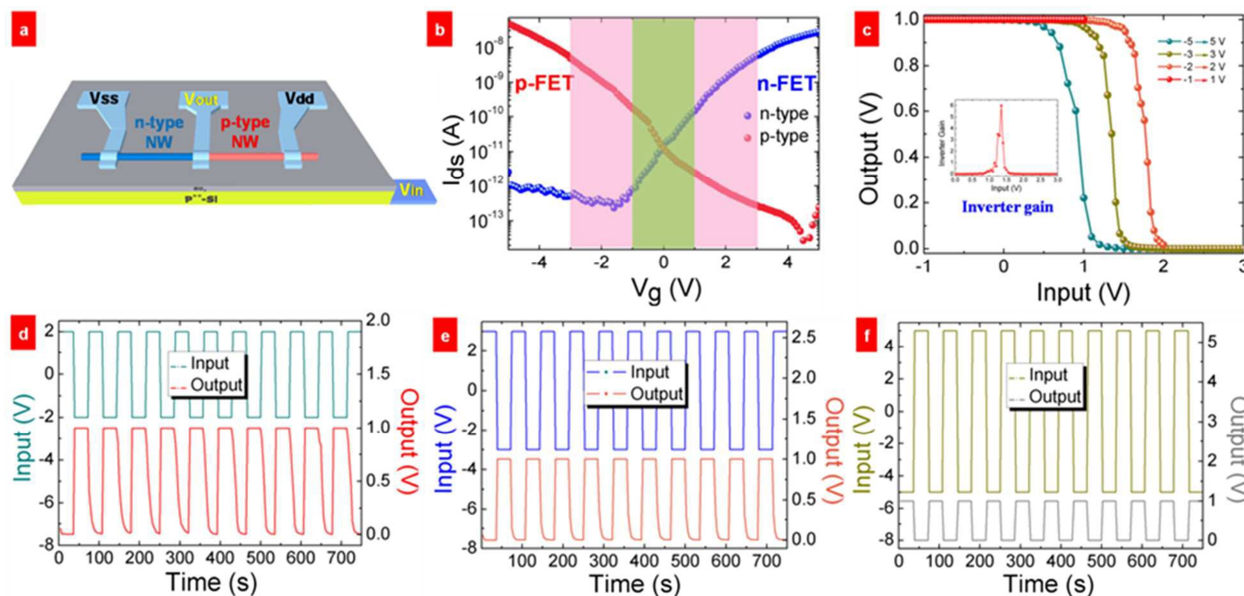

Fig. 5 CMOS inverter based on axially doped p-n Si NW FETs, and its electrical properties. (a) Schematic view of the back-gate inverter device. (b) I_{ds}–V_g transfer characteristics of p- and n-type regions of the axial p-n Si NW FETs. (c) V_{in}–V_{out} inverter characteristics. Inset shows the inverter gain. Dynamic response of the inverter to square-wave input pulses of (d) –2 and 2 V, (e) –3 and 3 V, and (f) –5 and 5 V, where V_{dd} is set to 1 V.

The I_{ds}–V_g transfer characteristics and I_{ds}–V_{ds} output characteristics of the p-n Si NW FETs were measured, as shown in Fig. 4. Figure 4b shows the drain current versus the drain-source voltage (I_{ds}–V_{ds}) curves for the n-type region of the p-n Si NW FETs. The conductance of the NW increased monotonically as the gate potential increased from –5 V to +5 V, exhibiting typical n-type Si NW FET behaviour. Figure 4a shows the drain current versus gate-source voltage (I_{ds}–V_g) curves for the n-type region obtained by sweeping the gate voltage continuously from –5 V to 5 V at a drain voltage ranging from 0 to 1 V. The transconductance (g_m) and field-effect electron mobility (μ_e) of the back-gate p-n Si NW FETs were determined from the I_{ds}–V_g curves using the following equations: $g_m = dI_{ds}/dV_g$ and $\mu_e = g_mL^2/C_{ox}V_{ds}$.[31] The gate oxide capacitance (C_{ox}) of a cylindrical wire on a planar substrate can be estimated as $C_{ox} = 2\pi\varepsilon_r\varepsilon_0 L/\cosh^{-1}(1 + t_{ox}/r)$ using a relative dielectric constant (ε_r) of 3.9, a SiO_2 gate dielectric layer thickness (t_{ox}) of 100 nm, a NW conducting channel length (L) of approximately 3.5 µm, and a NW radius (r) of approximately 25 nm. For the n-type region of the p-n Si NW FETs on a SiO_2/Si substrate, a threshold voltage (V_{th}) of –2 V and a transconductance (g_m) of 108.2 nS were extrapolated from the linear region of the I_{ds}–V_g curve at V_{ds} = 1

$cm^2\ V^{-1}\ s^{-1}$ were calculated from the plots in Fig. 4c,d, and ρ was estimated to be 0.07Ωcm from four-probe measurements (Fig. S2d in the Supporting Information). The hole carrier concentration (n_h) was estimated to be 7.5 × 10^{17} h cm^{-3} using the equation $n_h = C_{ox}V_{th}/q\pi r^2L$.[32] The subthreshold swing (S) was approximately 177.9 mV dec^{-1}. The subthreshold swings of the n- and p-type regions of the p-n Si NW FETs are small enough for low-power-consumption devices. The electrical characteristics of the p-n Si NW FETs and the comparison of mobility between the Si NW FETs in this study and other FETs made from single p-type and n-type Si NWs reported elsewhere are summarized in Table S2 and S3 in the supplementary information, respectively.

The input–output characteristics of a CMOS inverter based on single p-n Si NW FETs were measured in a FET device with three top electrodes and a back gate, as shown in the schematic illustration in Fig. 5a. The I_{ds}–V_g transfer characteristics of the p-n Si NW FETs are shown in Fig. 5b. The input–output characteristics for a supply voltage (V_{dd}) of 1 V, with the input voltage (V_{in}) swept from –1 to 1 V, –2 to 2 V, –3 to 3 V, and –5 to 5 V, are shown in Fig. 5c. Owing to the differences in the threshold voltages and conduction states of the p- and n-type regions of the p-n Si NW FETs, the input voltage was swept

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through different ranges. When the input voltage was swept from –3 to 3 V, sharp switching output swings were observed, which correspond to large inverter gains (dV_{out}/dV_{in}) of approximately 6 (inset of Fig. 5c). The key advantage of the NW CMOS inverter is the ultralow low consumption of static power owing to the small current flow from V_{dd} to the ground. This is irrespective of whether the input voltage is low and the n-type region of the p-n Si NW FET is OFF, or the input voltage is high and the p-type region of the p-n Si NW FET is OFF. The static current is less than 0.3 pA at V_{dd} = 1 V when V_{in} is 0 or 1 V; thus, the static power dissipation is less than 0.3 pW. The dynamic responses of the inverter to square-wave input signals at –2 and 2 V, –3 and 3 V, and –5 and 5 V, all at a frequency of 0.02 Hz and V_{dd} = 1 V, are shown in Fig. 5d,e, and f, respectively. The logic NOT function output voltage stayed close to 0 and 1 V when the input pulse voltages were 3 and –3 V, respectively.

4. Conclusions

A simple method of synthesizing highly ordered axially doped p- and n-type regions on a single Si NW was demonstrated, where the transport properties of each region can be modulated by controlling the doping concentration. The synthesis and removal of the radial oxide layer were optimized. Using single axially doped p-n Si NWs as conducting channels, p-n junction diodes and CMOS inverters were selectively fabricated. The optimized doping concentrations were determined to be a 4,500:1 silane (SiH_4)/phosphine (PH_3) ratio with a threshold voltage of –2 V for the n-type region, and a 5,500:1 silane (SiH_4)/diborane (B_2H_6) ratio with a threshold voltage of 2.5 V for the p-type region of the p-n Si NW FET, all while maintaining a sufficient I_{ON}/I_{OFF} ratio exceeding 10^5. Therefore, the axial p-n Si NW can be used as a conducting channel in the CMOS inverter. The device performance was carefully characterized in terms of the electrical transport and inverter input–output characteristics. The inverter has a low operating voltage of approximately ±3 V, resulting in inverter devices with extremely low power consumption. The results imply that such p-n Si NWs show promise as next-generation building blocks for high-performance, high-density diodes, as well as for logic circuits such as NOT, NOR, NAND, and SRAM for use in flexible electronic applications.

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