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Gate-tunable Diode-like Current Rectification and Ambipolar Transport in Multilayer van der Waals $ReSe_2/WS_2$ p-n Heterojunctions

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Vertically stacked van der Waals (vdW) heterojunctions of two-dimensional (2D) transition metal dichalcogenides (TMDs) have attracted a great deal of attention due to their fascinating properties. In this work, we report two important gate-tunable phenomena in a new artificial vdW p-n heterojunctions created by vertically stacking p-type multilayer $ReSe_2$ and n-type multilayer WS_2: (1) Well-defined strong gate-tunable diode-like current rectification across the p–n interface is observed, and the tunability of the electronic processes is attributed to the tunneling-assisted interlayer recombination induced by majority carriers across the vdW interface; (2) The distinct ambipolar behavior under gate voltage modulation both at forward and reverse bias voltage is found in the vdW $ReSe_2/WS_2$ heterojunction transistors and a corresponding transport model is proposed for the tunable polarity behaviors. The findings may provide some new opportunities for building nanoscale electronic and optoelectronic devices.

1 Introduction

2D TMDs have been widely investigated due to their great potential applications in nanoelectronics and optoelectronics and plasmonics.[1-11] Recently, the heterostructures combined with different 2D crystals by vdW force have been paid much attention. Since the vdW heterostructures avoiding lattice mismatches between different materials are very different from traditional IV, III-V, or II-VI semiconductor heterojunctions connected by covalent bonds between atoms in the interface,[12, 13] they have demonstrated tremendously applied potentials in electronics and optoelectronics such as field-effect transistors (FETs), photovoltaic cells, rectifiers, and light-emitting diodes.[14-19] Here adopting "dry transfer" method,[18, 20, 21] we build a vdW $ReSe_2/WS_2$ p–n junction by using stacked multilayer p-type $ReSe_2$ and n-type WS_2 flakes. In such heterojunctions, we investigate two important gate-tunable phenomena: (1) Well-defined strong diode-like current-rectifying characteristics, (2) distinct ambipolar behavior. The corresponding mechanism has been explained by tunneling-assisted interlayer recombination as well as unique transport model in the interface.

2. Experimental section

2.1 Fabrication and characteristics of vdW $ReSe_2/WS_2$ p-n heterojunctions

High-quality WS_2 and $ReSe_2$ crystals with typical size of 1~2 cm were grown using vertical Bridgman technique, and their crystal characteristics were confirmed by using transmission electron microscopy (**ESI Fig. S1†**). A typical of the vdW $ReSe_2/WS_2$ p-n heterojunctions device and their schematic diagram are shown in **Figures 1a** and **1d**, respectively. In order to build the device, the mechanically exfoliated multilayer WS_2 flake was first deposited on Si substrate coating a 300 nm-thick layer of SiO_2, which was used as the dielectric for back gate, and then mechanically exfoliated multilayer $ReSe_2$ was partly covered onto multilayer WS_2 by the "dry transfer" method to form vdW heterostructures at the overlapped regions of the WS_2 and $ReSe_2$ multilayers (**Figure 1d, ESI section A**). The source and drain electrodes (Cr (8 nm)/Au (80 nm)) were fabricated on the $ReSe_2$ and WS_2 multilayer by using electron-beam lithography, respectively (**Figures 1a and 1d, ESI section A**). Thickness of WS_2 and $ReSe_2$ in the device was ~80 nm (about 100 layers) and ~147 nm (about 150 layers), respectively, which were measured by atomic force microscopy (AFM) (**Figure 1b-c, ESI section A**). The Raman spectra of the $ReSe_2/WS_2$ heterojunctions

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includes all the typical Raman models in both WS_2 and $ReSe_2$ (**Figure 1 e, ESI section A**), indicating the vdW feature of the $ReSe_2/WS_2$ heterojunctions.

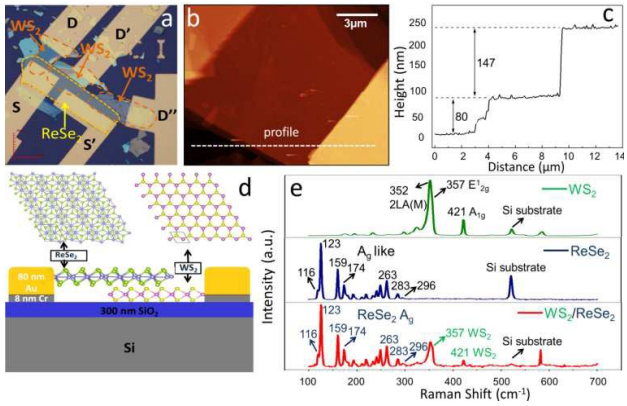

Figure 1 (a) The optical microscope image of the vertical stacked $ReSe_2/WS_2$ p-n heterostructural transistors ; (b) The selected region of AFM image and (c) the corresponding profile of a $ReSe_2/WS_2$ p-n heterojunction; (d) The schematic diagram of a $ReSe_2/WS_2$ p-n heterojunction; (e) Room-temperature Raman spectra for the different positions on the sample: individual WS_2 (green), individual $ReSe_2$ (blue), and the $ReSe_2/WS_2$heterojunctions (red). The wavelength of using laser is 532 nm.

2.2 Electrical measurements

The FETs characterization was performed using Agilent B2902 at room temperature under ambient conditions. In the electrical measurements, a voltage (V_{sd}) was applied across the junction region and the voltage bias V_g was applied to the back gate for modulating the diode device as well as the carrier densities in each semiconductor layer.

3 Results and discussion

Since the nature of the heterojunctions built by thin 2D materials may have gate-tunable diode features such as rectification, output and transfer curve, it is necessary to investigate gate-modulated electrical transport properties of the vdW heterojunctions based p–n diode. The gate-tunable diode-like current rectification and ambipolar behavior were observed in the vdW $ReSe_2/WS_2$ heterojunctions. And a corresponding transport model was proposed for the gate-tunable behaviors.

3.1 Gate-tunable diode-like current rectification

Before testing the electrical characteristics of p–n heterojunction diodes, we first characterized the electrical transport properties of $ReSe_2$ and WS_2 to ensure that Ohmic contacts were achieved (**ESI Fig. S2†**). To this end, the WS_2 and $ReSe_2$ FETs were fabricated on Si substrate covering a 300 nm-thick SiO_2 with Cr (8 nm)/ Au (80 nm) as metal electrodes to form contact with the 2D materials, respectively (**ESI inset of Fig S1a,b**). The linear I_{sd}–V_{sd} curves for both the $ReSe_2$ and the WS_2 (**ESI Figure S1a,b**) indicate Ohmic contact of the electrodes. The I_{sd}-V_{sd} with different back gate voltages (**ESI Figure S1c**) show that for the WS_2 and the $ReSe_2$, I_{sd} increases or decreases with increasing positive gate voltage, respectively, showing n-type and p-type semiconductor behaviors of the WS_2 and $ReSe_2$ (**ESI Figure S1d**). And both WS_2 and $ReSe_2$ multilayers exhibit low on/off ratios (**ESI Figure S1e,f**).

The electrical properties of the $ReSe_2/WS_2$ p-n heterojunctions were studied carefully. A strong current-rectifying phenomenon was observed when the p-type $ReSe_2$ was positively biased (**Figure 2a**). The current rectification behavior in the I_{sd}–V_{sd} plot with a rectification ratio (defined as forward-to-reverse bias current) of ~30 was achieved (**Figure 2a**), which was much higher than that of individual $ReSe_2$ or WS_2 multilayer (both less than 10). The current rectification clearly demonstrates that the p-$ReSe_2$/n-WS_2 heterojunctions are asymmetric for V_{sd}. The gate-tunable diode characteristics should come from ultrathin nature of the heterojunctions. Typical output characteristics of the p-n diode (I_{sd}–V_{sd}) (**Figure 2b**) shows that the I_{sd}–V_{sd} can be modulated by back gate voltage V_g. I_{sd}–V_{sd} curve with varying back gate voltage shows the gate-voltage-dependent rectification effect. Relatively speaking, the output current of the diode is more dependent on the p-type $ReSe_2$ in the p–n heterojunctions and thus increases with an increase in gate voltage, indicating that charge transport of the n-type WS_2 is limited in the device.

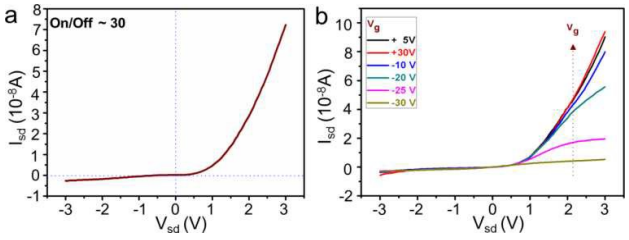

Figure 2 (a) The I_{sd}–V_{sd} plot of $ReSe_2/WS_2$ p–n heterojunction rectifier; (b) Gate-tunable output characteristics of a vertical $ReSe_2/WS_2$ heterojunction p–n diode. The gate voltage V_g= -30, -25,-20,-10, 0, 5 V, respectively.

Generally, the current rectification behavior observed in a conventional bulk p-n junction comes from the fact that forward bias current is determined by recombination followed by diffusion of majority carriers over electrical potential barriers across the depletion region. Although the observed current rectification behavior of p-$ReSe_2$/n-WS_2 vdW heterojunctions shows the similar features to conventional p–n junction diodes, the underlying microscopic mechanism of rectification is entirely different because the vdW 2D p-n junction diode does not allow a depletion region across the two adjacent layers compared with the traditional bulk p-n junction.

To understand the micromechanism on current rectification of our heterojunctions, we calculated the band offset between $ReSe_2$ and WS_2 by using density functional calculations (Vienna *ab* initio simulation package), as shown in **Figure 3**. The exchange–correlation function is treated by the generalized gradient approximation (GGA) with Perdew-Burke-Ernzerhofer parameterization (PBE). The projected augmented wave potential is also employed to describe the electron-ion potential. The calculated band structure is shown in Figure 3a-b, and their valence band maximum (VBM) and conduction band minimum (CBM) values show that $ReSe_2/WS_2$p-n junction forms type-II heterostructures as shown in **Figure 3c (**Calculated band alignment between $ReSe_2$ and WS_2 with respect to the vacuum level) **and ESI Figure. S3†** (The

band offset of type-II $ReSe_2$-WS_2 heterostructure in the Fermi level alignment). Since electrons and holes can be separated effectively when WS_2 and $ReSe_2$ bound together forming type-II heterostructures through van der Waals force, electrons in WS_2 CBM and holes in $ReSe_2$ VBM can transfer to each other at the interface of the junction to achieve balance between electron potentials, as shown in **Figure 3d**. When applying a forward bias, the majority carriers (electrons in n-doped WS_2 and holes in p-doped $ReSe_2$) will continue to accumulate at the interface, which will increase probability of tunnel recombination for the majority carriers, thus resulting in an increase in the forward current. On the other hand, holes in p-doped $ReSe_2$ and electrons in n-doped WS_2 are depleted under a reverse bias, decreasing tunnel recombination probability of the majority carriers and leading to a much smaller reverse current.

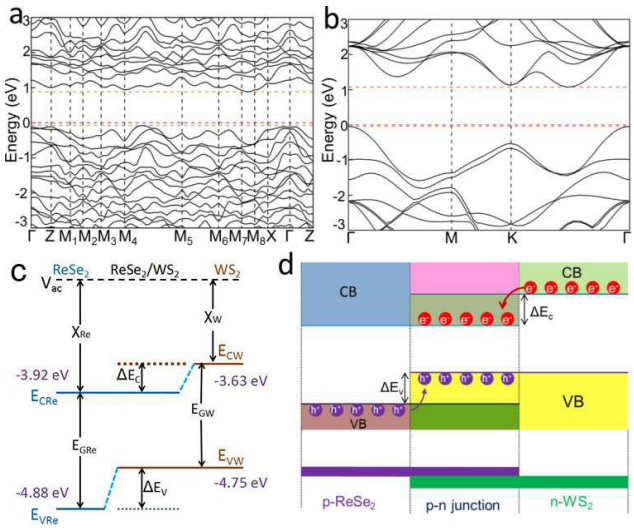

Figure 3 Calculated band structures of (a) $ReSe_2$ and (b) WS_2 with first principle calculations. (c) Calculated band alignment between $ReSe_2$ and WS_2 with respect to the vacuum level. (d) Band profiles in the lateral direction.

3.2 Gate-tunable ambipolar behavior

Unlike the unipolarity of p-type $ReSe_2$ or n-type WS_2 multilayer-based transistors, gate-voltage-dependent ambipolar feature (from n- to p-type) in the $ReSe_2$/WS_2heterojunctions is found by applying forward (**Figure 4**) and reverse bias voltage, and the corresponding transport model is proposed. In the measurements, the gate voltage sweeps from −40 to 15 V for different source-drain voltages. The transfer curve of the p-n diode under a positive source–drain voltage V_{sd} = 4V in **Figure 4a** shows that a typical p-type feature with a current on-off ratio (defined as the ratio of the forward current to the reverse current) of about 10 when V_g< -30 V and a typical n-type feature with a current on-off ratio of 450 when V_g> -30 V, demonstrating an excellent ambipolar property. It is noted that the current on-off ratios have a great increase compared to that of the individual WS_2 or $ReSe_2$ multilayer-based transistor (**ESI Fig. S2†**). The transfer curve of the p-n diode under negative source–drain voltage (V_{sd} = -4 V) shows a similar ambipolar feature (**Figure 4b**). The difference in work function and bandgap between the $ReSe_2$ and WS_2 creates an atomically heterointerface and predicted to be of type II band alignment, the tunneling-assisted interlayer recombination processes induced by majority carriers across the vdW interfacewill play the major role at the interface of the junction (**Figure 3d)**. Note that under the positive V_{sd} (**Figure 4a**), the electrons carriers play a major role, and the majority carriers-electrons at the top surface in n-WS_2 generated by backgate votage will dominate in the $ReSe_2$/WS_2 interface, resulting that the n-type property was much stronger than the p-type property of whole system. And under the negative V_{sd} (**Figure 4b**), the majority carriers-electrons at the top surface in n-WS_2 and majority carriers-holes at the bottom p-$ReSe_2$ were generated by backgate votage, and the majority carriers-electrons together with the majority carriers-holes will play almost the same role in the $ReSe_2$/WS_2 interface, resulting that the n-type and p-type properties show a similar effect of whole system.

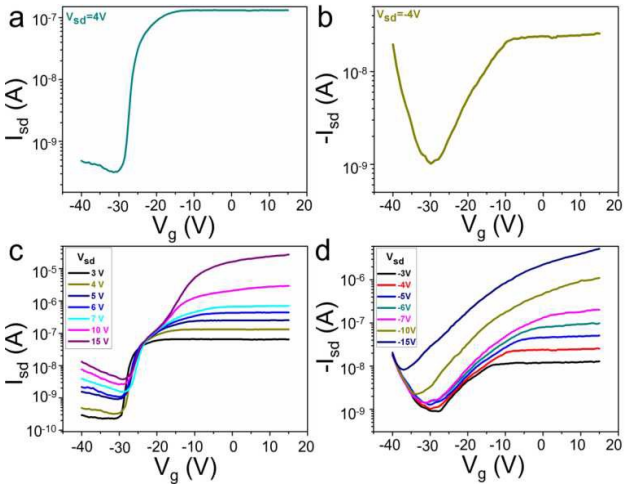

Figure 4. Transfer curves of $ReSe_2$/WS_2 heterostructure transistors measured under (a) positive source drain voltage (V_{sd} = 4 V) and (b) negative V_{sd} (V_{sd} = - 4 V), (c) Different positive V_{sd}, (d) different negative V_{sd}. The transfer curves all displayed logarithmic function I_{sd}-V_g curve of the device.

More importantly, the transfer curve of ambipolar behavior in the $ReSe_2$/WS_2 p-n diode can be tunable by the gate voltage, as shown in **Figure 4 c,d**. The influence of positive V_{sd} on ambipolar curve for V_{sd} = 3,4,5,6,7,10,15 V is shown in **Figure 4c**, finding that the I_{sd} increases with increasing of V_{sd}. This is because that the electrons in WS_2 will accumulate to the junction interface with an increase of V_{sd} to increase recombination possibility of holes and electrons, and thus increases the tunneling current (I_{sd}). It is easily to see that for negative V_{sd}, there is a similar influence on ambipolar curve **(Figure 4d)** compared to positive V_{sd} in **Figure 4c**， and mechanism is the same excepting holes in $ReSe_2$ instead of electrons in WS_2 (**Figure 4d**). Note that I_{sd} at V_g=0 V and V_{sd}= -3 V in **Figure 4d** is a little larger than I_{sd} in Figure **2a** because the later was measured one day later than the former. This may induce that the device adsorbed a large number of water molecules and became slight oxidation due to exposing to the air, and such resulting in an increase in resistor of

the device. Additionally, according to the data presented in **Figure 4b**, we calculate the field-effect mobility (μ) of the $ReSe_2/WS_2$ heterostructure transistors using the equation $\mu = (L/WC_iV_{sd})\partial I_{sd}/\partial V_g$, where L is the channel length, W is the channel width, and $C_i = 1.15 \times 10^{-4}$ F/m^2 is the gate capacitance between the channel and the back gate per unit area ($C_i = \varepsilon_r/d$; $\varepsilon = 8.85 \times 10^{-12}$ F/m is vacuum permittivity; $\varepsilon_r = 3.9$ is relative permittivity of insulating barrier SiO_2; $d = 300$ nm is the thickness of the insulating barrier).[15, 21] The calculated field-effect mobility of hole in p-type part of transfer curve (**Figure 4a)** is 0.4 $cm^2V^{-1}s^{-1}$, while the mobility of electron in n-type part is 0.1 $cm^2V^{-1}s^{-1}$, slightly smaller than its p-type part.

4. Conclusions

In summary, we have fabricated and investigated a new vdW $ReSe_2/WS_2$ p-n heterojunctions. The heterojunctions exhibited interesting gate-voltage-tuned rectifying effect and polarity feature. Our results indicate that the tunneling-assisted interlayer recombination of majority carriers plays a crucial role in the rectifying electrical characteristics of the vdW heterojuctions, revealing that the rectifying characteristics in the vdW p-n $ReSe_2/WS_2$ heterojunctions is a quite different microscopic mechanism from traditional semiconductor p-n heterojunctions. And mechanism of the polarity feature has been well explained by the charge transport model we proposed. These novel gate-voltage tunable electrical properties observed in the new artificial $ReSe_2/WS_2$ p-n heterojuctions will provide us a new method to adjust polarity behavior and rectifying feature of p-n heterojunctions and open some new chances for developing new optoelectronic devices with high-performance.

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Notes and references

Notes

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References

1. B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti and A. Kis, *Nature nanotechnology*, 2011, **6**, 147-150.
2. S. Yang, C. Wang, H. Sahin, H. Chen, Y. Li, S.-S. Li, A. Suslu, F. M. Peeters, Q. Liu and J. Li, *Nano letters*, 2015, **15**, 1660-1666.
3. S. X. Yang, S. Tongay, Y. Li, Q. Yue, J. B. Xia, S. S. Li, J. B. Li and S. H. Wei, *Nanoscale*, 2014, **6**, 7226-7231.
4. S. Yang, Y. Li, X. Wang, N. Huo, J. B. Xia, S. S. Li and J. Li, *Nanoscale*, 2014, **6**, 2582-2587.
5. H. Cai, E. Soignard, C. Ataca, B. Chen, C. Ko, T. Aoki, A. Pant, X. Meng, S. Yang and J. Grossman, *Advanced materials*, 2016,DOI: 10.1002/adma.201601184.
6. C. Wang, S. Yang, H. Cai, C. Ataca, H. Chen, X. Zhang, J. Xu, B. Chen, K. Wu and H. Zhang, *Nanoscale*, 2016, **8**, 5820-5825.
7. C. Wang, S.-X. Yang, H.-R. Zhang, L.-N. Du, L. Wang, F.-Y. Yang, X.-Z. Zhang and Q. Liu, *Frontiers of Physics*, 2016, **11**, 1-5.
8. H. Cai, J. Kang, H. Sahin, B. Chen, A. Suslu, K. Wu, F. Peeters, X. Meng and S. Tongay, *Nanotechnology*, 2016, **27**, 065203.
9. Y. Yu, Z. Ji, S. Zu, B. Du, Y. Kang, Z. Li, Z. Zhou, K. Shi and Z. Fang, *Advanced Functional Materials*, 2016,DOI: 10.1002/adfm.201601779.
10. Z. Li, Y. Xiao, Y. Gong, Z. Wang, Y. Kang, S. Zu, P. M. Ajayan, P. Nordlander and Z. Fang, *ACS nano*, 2015, **9**, 10158-10164.
11. Z. Li, R. Ye, R. Feng, Y. Kang, X. Zhu, J. M. Tour and Z. Fang, *Advanced materials*, 2015, **27**, 5235-5240.
12. W. J. Yu, Y. Liu, H. Zhou, A. Yin, Z. Li, Y. Huang and X. Duan, *Nature nanotechnology*, 2013, **8**, 952-958.
13. B. W. Baugher, H. O. Churchill, Y. Yang and P. Jarillo-Herrero, *Nature nanotechnology*, 2014, **9**, 262-267.
14. R. Cheng, D. Li, H. Zhou, C. Wang, A. Yin, S. Jiang, Y. Liu, Y. Chen, Y. Huang and X. Duan, *Nano letters*, 2014, **14**, 5590-5597.
15. S. Yang, C. Wang, C. Ataca, Y. Li, H. Chen, H. Cai, A. Suslu, J. C. Grossman, C. Jiang and Q. Liu, *ACS Applied Materials & Interfaces*, 2016, 8, 2533-2539.
16. N. Huo, J. Kang, Z. Wei, S. S. Li, J. Li and S. H. Wei, *Advanced Functional Materials*, 2014, **24**, 7025-7031.
17. C.-H. Lee, G.-H. Lee, A. M. Van Der Zande, W. Chen, Y. Li, M. Han, X. Cui, G. Arefe, C. Nuckolls and T. F. Heinz, *Nature nanotechnology*, 2014, **9**, 676-681.
18. Y. Li, Y. Wang, L. Huang, X. Wang, X. Li, H.-X. Deng, Z. Wei and J. Li, *ACS applied materials & interfaces*, 2016, 10, 10158-10164.
19. R. Cheng, D. H. Li, H. L. Zhou, C. Wang, A. X. Yin, S. Jiang, Y. Liu, Y. Chen, Y. Huang and X. F. Duan, *Nano letters*, 2014, **14**, 5590-5597.
20. N. Huo, J. Yang, L. Huang, Z. Wei, S. S. Li, S. H. Wei and J. Li, *Small*, 2015, **11**, 5430-5438.
21. X. Wang, L. Huang, Y. Peng, N. Huo, K. Wu, C. Xia, Z. Wei, S. Tongay and J. Li, *Nano Research*, 2015, 1-10.

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