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Ultrahigh performance negative thermal resistance switching based on individual ZnO:K,Cl micro/nanowires for multibit nonvolatile resistance random access memory dual-written/erased repeatedly by temperature or bias

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Currently, nanostructure-based random access memories (RAMs) mainly focus on the writing of data information by electricity. Here, nonvolatile multibit thermal resistive RAMs (TRAMs), which are dual-written/erased by different temperatures or drain-source biases, are realized successfully in two-terminal devices based on individual ZnO:K,Cl micro/nanowires. The mechanism of emptying and filling of trap states is proposed for the explanation of temperature and bias controlled multibit information writing and erasing. The incorporation of KCl in ZnO lattice creates abundant defects, which can serve as trap centers and store charges. At relatively high temperature, the trapped charges can escape under a low operation voltage, resulting in a downshift of ZnO Fermi level, and moreover the depth of emptied trap is dependent of loaded temperature. Therefore, a tunable high resistance state can be obtained. At relatively high bias, subsequently, electrons can inject into trap states under a low operation temperature, and moreover the depth of filled trap depends on applied voltage. Therefore, a tunable low resistance state can be acquired due to an upshift of ZnO Fermi level. It is due to the thermal excitation and electric field injection induced emptying and filling of trap states that multibit information can effectively be dual-written/erased by different temperatures or biases. The results indicate that the modulation of trap states by impurity introduction in nanostructures gives a direction to the development of novel nanodevices in rewritable nonvolatile temperature and bias information sensor and memory.

1. Introduction

Candidates for modern nonvolatile random access memories (RAMs), including ferroelectric random access memory (FeRAM), in which the polarization of a ferroelectric material is reversed, magnetoresistive RAM (MRAM), in which a magnetic field is involved in the resistive switching (RS), resistive RAM (RRAM), in which the two very distinct resistance levels are switched by submitted to a voltage pulse, and phase-change RAM (PRAM), in which thermal processes control a phase transition in the switching material from the amorphous state to the crystalline state, have attracted a great deal of attention. Compared with the capacitance-based RAMs, the RS characteristics of semiconductor micro/nanowires, such as NiO, ZnO, Zn$_2$SnO$_4$, and GeSe$_2$, have been extensively studied in resistance-change-based RAM due to its superior performance in simple fabrication process, lower power consumption, long retention time, high operation speed, high endurance write cycles, non-destructive readout, favorable scalability, and CMOS process compatibility.

In the RRAM technology, the “0” and “1” logical states correspond to the RS back and forth between low resistance state (LRS) and high resistance state (HRS) by submitted to voltage pulses, and depending on the set and reset processes, the RS characteristics can be classified into bipolar and unipolar switching types. The switching mechanism can be attributed to conducting filament, charge-trap model alteration of Schottky barrier, space-charge-limited current, and Mott transition. Recently, back-to-back bipolar RSs were observed in the ohmic and Schottkey contact two-terminal devices. In 1D micro/nanostructure based systems, the injection of electrons into/from surface and interface states created by doping can modulate their barrier height, and therefore their conduction states can be well controlled. ZnO micro/nanowire, owing to a wide direct bandgap, a large exciton binding energy, and abundant trap states, becomes the ideal candidate for back-to-back Schottky-like diode, and properly doped ZnO micro/nanowire can...
introduce impurity levels and various defect traps, which combine with surface/interface states and intrinsic trap states to form miscellaneous depth trap levels.24-26

In order to meet the demands for increased data storage capacity, multibit memory devices have been explored to replace single bit memory devices. For traditional NAND flash memories, it is difficult to realize the scale-down of multibit storage to the size of a single memory cell due to the geometric configuration, which may face some challenge, such as retention, leaky, or endurance reliability issues when device shrinking, and several works have been proposed to solve the problem.27 For RS memory devices in previous work, the effective multibit effect almost based on setting gates or fabricating special configurations.28-30,31 In addition, comparing to widely exploration for electrical information program, the RRAM, used for thermal data writing, has no relative reports, although the temperature detectors and sensors are rapidly developed today.

In this work, novel programmable thermalresistive RAMs (TRAMs), based on two-terminal devices of individual ZnO:K,Cl superstructure micro/nanowires, were fabricated for the first time, which made the temperature and drain-source bias information acquisition and memory realized easily. The mechanism dominantly originates from the abundant bulk trap states donated by the incorporation of K and Cl impurities. The switching between HRS and LRS corresponds to emptied and filled trap states, respectively, which are regulated by thermal excitation and electric injection, respectively. More interestingly, the depth of emptied and filled trap state can controllably be adjusted by the imposed temperature and bias, which makes the memory a further application in nonvolatile memories, it is difficult to realize the scalesdown of multibit capacity, multibit memory devices have been explored to shrinking, and several works have been proposed to solve the problem.27 For RS memory devices in previous work, the effective multibit effect almost based on setting gates or fabricating special configurations.28-30,31 In addition, comparing to widely exploration for electrical information program, the RRAM, used for thermal data writing, has no relative reports, although the temperature detectors and sensors are rapidly developed today.

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reaches a minimum at about 200 °C, and subsequently increases with further increasing temperature. Additionally, the output currents were also measured by annealing from RT to 75, 200, 250, 260, 270, 300, and 375 °C, respectively, and then recooled to RT, as shown in Fig. 2b and c. It is clear that the single ZnO:K,Cl nanowire-based device is highly sensitive to externally imposed temperature. The device shows a negative giant thermalresistance switching performance at the measurement temperature lower than about 270 °C. On the contrary, it shows a positive thermalresistance switching effect at the measurement temperature higher than about 270 °C. After it is completely cooled to RT, more interestingly, the device can still remain a HRS at the annealing temperature lower than 270 °C, namely the presence of an outstanding resistance difference before and after annealing. Moreover, the HRS can remain for a long time, indicating a nonvolatile memory effect. In addition, the maximum variation in resistance can be obtained before and after annealing at about 200 °C. The results indicate that ZnO:K,Cl has a huge potential for temperature sensor applications, especially for nonvolatile temperature-writing memory applications at an operating temperature lower than 270 °C.

I-V characteristics of TRAM cell were further measured at a low bias voltage of 0.5 V before, under and after annealing at 200 and 375 °C, respectively, as shown in Fig. 3. It can be observed that the changing trend of resistances is consistent with that in Fig. 2. Compared with the conductivity of device before annealing, it not only shows a significant reduction under annealing at 200 °C, but remains a distinguishable decrease after annealing at 200 °C. Contrarily, its conductivity exhibits a huge increase under annealing at 375 °C, and unfortunately it shows hardly a variation after annealing at 375 °C, indicating a poor memory effect. Interestingly, each resistance state echoes a certain temperature, which may enable a memory capacity for writing temperature information bit-by-bit into the two-terminal TRAM cell. Therefore, the temperature-related data storage capability can be achieved at annealing temperature lower than 270 °C. The resistance state which responds to the temperature above 270 °C, may not be an appropriate choice for memory due to little resistance variation.

After annealing at the temperature lower than 270 °C, the device shows a HRS. More interestingly, the device can return to its initial LRS after applying a relatively high bias voltage at RT, indicating that the stored temperature information can be erased effectively by a relatively high drain-source bias. Fig. 4 shows the detailed cyclic I-V characteristics in LRS, HRS, and the course of erasing information. It can be seen that all the I-V characteristics show nonlinear behavior before and after
annealing at 200 °C, as shown in Fig. 4a. To more deeply take insight into the conduction mechanism of TRAM devices, the I-V curves were fit by Poole–Frenkel (PF) emission law.32,33

\[ J = B V \exp \left( -\frac{q(\phi_T - \sqrt{V/\pi \varepsilon_r \varepsilon_0 d})}{kT} \right) \]

(1)

Where \( B \) is constant, \( q \) is unit charge, \( \phi_T \) is barrier energy height for electron emission, \( \varepsilon_r \) is relative permittivity of the RS medium, \( d \) is thickness between the two electrodes, \( k \) is Boltzmann constant, and \( T \) is temperature. In Fig. 4b, the inset shows the test fittings for the plotting \( \ln V \) versus \( V^{1/2} \). The linear plots suggest that PF emission (bulk limited) is the most predominant conduction mechanism in the applied voltage range of 0–0.5 V, demonstrating that the electrical transport is dominated by the bulk traps rather than the surface state related Schottky barrier at micro/nanowire and electrode interface. Moreover, in order to investigate the relationship between effective trap depth of PF emission and temperature, the applied voltage was constant of 0.5 V, and the relation between \( \phi_T \) and \( T \) can be simplified as follow:

\[ -T \ln(j) \propto \phi_T \]

(2)

The temperature dependence of PF emission potential height, from room temperature to 400 °C, was analyzed in Fig. 4c. The trap potential \(-q\phi_T\) is the energies required to transfer electrons from the trap level to the conduction band and the value can be calculated. According to Reference,33-35 the value of \(-q\phi_T\), as obtained are about 287.75 and 761.05 meV for RT and 200 °C, respectively. The fitting results indicate that the PF trap levels is strongly dependent of temperature, which is consistent with the experiment result as illustrated in Fig. 2a, confirming the lower the current level by temperature effect, the larger the trap level for electron barrier.

As seen from Fig. 4d, the annealed device shows a nonvolatile HRS at read-out voltage lower than 0.5 V. With increasing bias voltage, subsequently, the current jumps abruptly at the voltage of about 4.2 V, switching from HRS to LRS in accompany with a large hysteresis loop, as shown in Fig. 4e. Thus, a reset process occurs at about 4.2 V. The corresponding I-V curve was fitted by Fowler–Nordheim (FN) tunnelling.36-40

\[ J = \frac{q^2 E^2}{16\pi^2 h}\exp \left( -\frac{4\sqrt{2m^* q(\phi_{ox})^2}}{3hE} \right) = C_1 E^2 \exp \left( -\frac{C_2 (\phi_{ox})^2}{E} \right) \]

(3)

Where \( E \) is electric field, \( q \) is unit charge, \( \phi_{ox} \) is energy barrier that must be overcome by electron, \( m^* \) is electron mass in as-prepared micro/nanowires, \( h \) is reduced planck constant, and \( C_1=6.82 \times 10^3 \text{eV}^{-3/2} \text{V}^{-1}\mu\text{m} \). The slope of data fitting under high voltage in Figure 4f led to an extracted electron barrier height \( (\phi_{ox}) \) of about 58.87 meV at RT. The FN tunnelling fitting results indicate that the extracted electron barrier strongly depend on the applied bias voltage. Moreover, the depth of filled traps increases with increasing bias voltage, which is well consistent with the experiment results as illustrated in Fig. 11 (b). The A linear decrease relation of \( \ln (|I/V^2|) / |V| \) can be obtained when the applied bias exceeds the mutation voltage of about 4.2 V, as shown in Fig. 4f. Afterward, when the bias voltage is swept to a negative value, the device current remains LRS, and moreover it is still in LRS under the subsequent cyclic sweeping, demonstrating that the device has become LRS after it is first subjected to a voltage higher than 4.2 V. A nonvolatile ON state is achieved. Therefore, the temperature induced nonvolatile HRS can be erased effectively by applying a relatively high bias voltage. Although the current behaviour under negative voltage sweeping is fairly similar to that under positive voltage sweeping, the hysteresis loop shrinks fast as sweeping progresses going on. For this, several cycles of erasing process

Fig. 2. Resistance variation of TRAM cell before, under and after annealing at different temperatures. (a) The current response to temperature varied consecutively from RT to 400 °C at a fixed bias voltage of 0.5 V, revealing that the dominant conduction mechanism changes from a trap excitation into an intrinsic bandgap excitation with increasing temperature. (b) The device is heated from RT to 75, 200, 250, 260, and 270 °C, respectively, and then re-cooled to RT, revealing that there is an obvious increase in resistance after annealing, namely a memory behavior. (c) The device is heated from RT to 300, and 375 °C, respectively, and then re-cooled to RT, revealing that the resistance decrease during annealing and moreover it merely shows a little variation after annealing.

![Image of resistance variation](image_url)

Fig. 3. I-V characteristics of ZnO:K,C1 micro/nanowire-based device before, under, and after annealing at different temperatures. (a) Before, under and after annealing at 200 °C, revealing the presence of a significant resistance difference before and after annealing. (b) Before, under and after annealing at 375 °C, revealing the presence of negligible resistance difference before and after annealing.
under ±5 V were taken, as shown in Fig. 4d. It shows that a relatively large hysteresis loop at first, and then gradually decelerate to zero with periodic cycles.

Owing to the presence of remarkable resistance variation before and after annealing at 200 °C, the temperature was chosen for the memory measurement of TRAM cell. Moreover, the HRS of the device, annealed at about 200 °C, can return to its initial LRS after applying a relatively high bias voltage higher than 4.2 V between two-terminal electrodes, indicating that the stored temperature information can be effectively erased by applying a high drain-source bias voltage. This indicates that suitable temperature and drain-source bias can serve as “gating” on tuning the charge carrier transport in ZnO device. Fig. 5 shows the thermoresistance memory performance for the two-terminal device operated at a fixed bias voltage and triangle wave voltage, respectively. The data can be effectively set-written by annealing at 200 °C under a low operation bias voltage of 0.5 V, and reset/erased by applying a relatively high bias voltage of 5 V in the condition of RT. In the course of readout, moreover, a similarly low bias voltage of 0.5 V is applied. Here, we define the resolution as

\[ R = \frac{I_{on} - I_{off}}{I_{off}} \]  

(4)

Where, \( I_{on} \) is LRS current before annealing and \( I_{off} \) is HRS current after annealing. As seen from the enlargement of a single write-read-erase-read cycle process, as shown in Fig. 5b and d, the resolution can reach two orders of magnitude. The response time of temperature and electricity sensing are 5 s and 0.4 s, respectively, as shown in Fig. 5e and f. The consecutive write-read-erase-read processes reveal a reversible and repeatable memory property. In addition, temperature-related information can be stored for a long time, and moreover they can be reset by a relatively high bias voltage, as shown in Fig. 6, confirming that the nonvolatile nature of the device is stable and durable.

### 3.3 Temperature and voltage dependence of memory mechanism

Fig. 7 shows the schematic diagrams of energy band structure and trapped electron distribution for illustrating the multibit TRAM effect in the two-terminal device. Since the work function of Ag (\( \Phi_{Ag}=4.26 \) eV) is lower than the electron affinity of ZnO (\( \chi_{ZnO}=4.35 \) eV), it is expected that the ohmic behaviour would be formed when ZnO is in direct contact with Ag electrodes. In RT, however, the I-V curves show nonlinear characteristics rather than typical linear ohmic contact characteristics, as shown in Fig. 3 and 6. It has been accepted that oxygen molecules can capture free electrons from the surfaces of n-type ZnO, which creates a surface space-charge layer from the surface to the interior.\(^{41,42}\) For one-dimensional ZnO micro/nanowires, abundant trap states, such as surface/interface states, intrinsic trap states, and impurities introduced by doping, exist inside them. The I-V curves, before and after annealing, can be fitted well by PF emission mechanism, as seen Fig. 6a. Therefore, the bulk defects related traps are dominant conduction mechanism rather than surface traps related Schottky barrier. In nanostructure ZnO, the introduction of K and Cl dopants can form defects such as dislocation and lattice distortion, clearly confirmed by HRTEM observation. Therefore, the defects can serve as trap centers and capture electrons. Moreover, the stored electrons can be excited from one trapped state by a random thermal fluctuation, and then hop into another trapped state. When the trap states are emptied, the population of electrons excited by thermal fluctuation decrease, and correspondingly the Fermi level of ZnO will downshift, resulting in a decrease of conductivity. As
seen from Fig. 2a, with increasing temperature, the conduction of RRAM will go through three stages: trap excitation, trap excitation-intrinsic bandgap excitation, and intrinsic bandgap excitation. With the increase of temperature from RT to 200 °C, electrons trapped by deeper level will be excited. Under annealing at 200 °C, the resistance of devices reaches a maximum, indicating the trapped electrons escape completely, and then decreases with further increasing temperature. When the annealing temperature continues to rise, subsequently, its resistance decreases gradually. Under annealing at 270 °C, its resistance can recover to the initial value at RT. After the device is annealed at the temperature higher than 270 °C, moreover, it only takes place a slight variation in resistance, indicating that the conduction will mainly dominated by intrinsic bandgap excitation. In addition, as seen from the cyclic 1-V characteristic measured at 200 °C, as shown in Fig. 8, the traps can be filled at the voltage higher than about 4.2 V, whereas it is immediately emptied with decreasing bias voltage, which more firmly demonstrates the origination of temperature and bias dependence of memory effect from trap states.

Upon applying an external electrical field between drain and source electrodes, the energy band will tilt. When the applied bias voltage reaches 4.2 V, the tilt height of energy band (qV) will exceed the height of trap barrier (Δφ), resulting in a filling of trap. It is easier for electrons to freely move inside ZnO lattice, and hence the Fermi level of ZnO will upshift and its conductivity increases significantly. As a consequence, the device transforms from HRS to LRS, namely reset process. It is due to the thermal excitation and electric field injection of electrons that result in a memory effect.

In thermal trap excitation stage, the depth of excited trap states increases with increasing temperature and shows a maximum at 200 °C. At the temperature lower than 200 °C, therefore, the trapped electrons can be thermally excited from traps to the conduction band (CB) and then the emptied traps are left in ZnO, resulting in a HRS.

**Fig. 6.** Stability and retention measurement of TRAM cell in both LRS and HRS at RT. (a) Readout by a fixed low bias voltage of 0.5 V. (b) Readout by a consecutive triangle wave voltage with low amplitude of 0.5 V and frequency of 0.1 Hz.
Fig. 7. Schematic energy band structure and trapped electron distribution diagrams for illustrating memory effect in the two-terminal TRAM cell, where $E_f$, $\Delta \phi$, and $qV$ are Fermi level, trap height, and electric field induced tilt height of energy band, respectively. (a) Before annealing, the trap states are partially filled by electrons. (b) After annealing, the trap states are completely emptied due to thermal excitation, and the Fermi level downshifts. The device shows a HRS. (c) At high external bias voltage, the emptied trap states are filled up by electrons from the negative electrode and the Fermi level downshifts. The device transforms from HRS into LRS. (d) After applying a relatively high bias, trap states are filled, which is advantageous for electrons to hop between different traps.

In thermal trap excitation-intrinsic bandgap excitation stage, the bandgap excitation is relatively weak, and few electrons can be excited directly from valence band (VB) to CB. The electrons excited from VB can fill into traps and subsequently localized in traps, resulting in a decrease of resistance. The mechanism of memory is similar to that of thermal trap excitation stage. In thermal trap excitation stage and thermal trap excitation-intrinsic bandgap excitation stage, the resistance states can be designed by different temperatures, means that multibit programmable thermal RRAM and temperature recognition can be realized below 270 °C.

In intrinsic excitation stage, the bandgap excitation dominates the conductivity, and therefore the current increase. Since HRS cannot be formed at the temperature higher than 270 °C, as shown the 300 and 375 °C testing results in Fig. 2c, the too high temperature is not suitable for information writing.  

3.4 Temperature-induced multilevel effect

As seen from Fig. 2a, the conductivity decreases with increasing temperature from RT to 200 °C, indicating that electrons located in deeper traps can be excited at a higher temperature. As seen from Fig. 2a and 10, in addition, the conductivity of device is different after annealing at different temperatures, and furthermore it is strongly dependent of annealing temperature. After applying a relatively high bias voltage, therefore, the HRS of device can be set by annealing at different temperatures. With the increase of annealing...
temperature, moreover, its conductivity shows a more obvious
degree, indicating the population of trapped electrons
decreases dramatically with increasing temperature. After
annealing, additionally, the current jumping occurs at different
bias voltages, further demonstrating that the annealing
temperature determines the concentration of trapped electrons,
namely annealing temperature dependence of conduction states.
After annealing at different temperatures, therefore, the LRS
device can change into different HRS at low operating bias
voltage. As seen from Fig. 9, the current of device, annealed at
different temperatures, can jump at different voltages, and
furthermore they are strongly dependent of the annealed
temperatures, revealing the emptied traps are determined by the
annealing temperature. Moreover, the voltage of current
jumping firstly increase and then decrease with the increase of
annealing temperature, which results from the transform of
thermal trap excitation-intrinsic bandgap excitation stage. The
similar behaviors of RRAM systems can be observed in the
work of others. Therefore, for the LRS devices applied a
relatively high bias voltage, their multibit memory effects can
be realized by annealing at different temperatures. The memory
properties, operated under different temperatures, have been
carried out, as shown in Fig. 10. Owing to the emptied traps are
strongly dependent of annealing temperature, the currents of
devices are different after erasing by the same high electric
field. The trap states of devices are different before heating at
high temperature and after applying high electric field, and
therefore the LRS before heating is different from that after
being subjected to heat treatment and high voltage. It can be
seen that the different HRS of the device, subjected to high bias
voltage, can be set by annealing at different temperatures, and
moreover the change in resistance reaches a maximum after
annealing at 200 °C, confirming a nonvolatile multibit
temperature memory effect.

3.5 Bias-induced multilevel effect

After annealing at 200 °C, traps can be emptied completely, and
correspondingly the device changes into HRS under low
operating bias. As seen from Fig. 11, the HRS device, annealed
at 200 °C, can change into LRS after applying different bias
voltages. Moreover its resistance is strongly dependent of the
applied bias voltages, indicating the depth of filled traps
increases with increase in bias voltage. For the HRS device
annealed at about 200 °C, therefore, its LRS can be set by
applying different bias voltages. Higher bias will lead to the
filling of deeper traps. Because the definition of 0 and 1 may
exchange mutually, the multibit memory performance can be

![Fig. 10. Temperature dependence of multibit HRS memory
effect. The read and set/write operation is carried out at a low
bias voltage of 0.5 V, and the reset/erase voltage is 5 V. The
color curves correspond to the current response.](image)

![Fig. 11. Voltage dependence of multibit LRS memory
effect for the HRS device annealed at 200 °C. (a) After
annealing at 200 °C, the recovery of resistance by applying
different fixed bias voltages from 1 to 10 V with an interval of 1 V,
revealing the bias voltage dependence of the resistance recovery,
namely a multibit voltage writing or erasing effect. (b) After
annealing at 200 °C, the recovery of resistance by applying a
triangle wave voltage with different amplitudes from 1 to 10 V
with an interval of 1 V, revealing that the depth of filled traps
is dependent of the applied bias voltage. (c) After annealing at
200 °C, the TRAM cell with HRS is subjected to various fixed bias
voltages from 1 to 10 V with an interval of 1 V, revealing that the
resistance of LRS is strongly dependent of the applied bias voltage.
The red curve represents current response and the blue curve corresponds to the
applied voltage. (d) The enlarged view of the green dotted frame in (c) shows a
detailed read-erase/write-read/write-erase cycle.](image)
written or erased by temperature or bias voltage, respectively. Based on the mechanism of trap modulation, the depth of emptied traps is determined by annealing temperature and the depth of filled traps is determined by applying bias voltage. The two-terminal devices in our research can be used as programmable multibit TRAMs dual-written/erased by temperature or bias voltage, which might be useful in the next generation of functional thermal-electronic circuits. There remain, however, several performance issues that must be resolved if we are to progress with thermal/voltage ‘dual-use’ memories and, thereby, position them in a distinctive role for multi-functional memories.

Besides for a fixed bias voltage, the memory can similarly be realized under the operation voltage with different wave forms. Fig. 4 and Fig. 12 show the results measured under different wave forms with the same amplitude such as triangle wave, sine wave, saw-tooth wave, and pulse wave. Here, we have attempted to set up new opportunities for RAMs to establish a link between temperature and electricity. Accordingly, this preliminary report of the memory device-featuring multibit data storage capacity, thermal/electronic ‘dual-use’, and free from the form of working voltage-demonstrates, at the laboratory level, functions of multibit programmable thermal/voltage ‘dual-use’ memories.

4. Conclusions

In summary, K and Cl-doped ZnO micro/nanowires were synthesized using a simple carbon thermal reduction. The incorporation of K and Cl leads to the presence of abundant defect traps in ZnO lattice. The individual ZnO:K,Cl micro/nanowire-based device not only shows a negative giant thermal-resistance switching effect at the temperature lower than 270 °C, but shows a novel temperature dependence of trap emptying behavior in the condition of a low operation bias after applying a relatively high bias voltage. Moreover, it shows a bias dependence of trap filling behavior as well in the condition of low operation temperature after annealing at about 200 °C. Therefore, the micro/nanowire-based two-terminal device can be used as programmable multibit TRAMs dual-written/erased by temperature or drain-source bias. The introduction and modulation of trap states in ZnO nanostructures give a direction to the development of novel nanodevices in repeatable writing/erasing temperature and bias sensors and multibit memories.

Acknowledgements

This work was financially supported by the National Natural Science Foundation of China (51612023, 51462023, 51571107), the Project for Young Scientist Training of Jiangxi Province (20133CB23002), the Major Program of Natural Science Foundation of Jiangxi Province (20152ACB20010), the Foundation of Jiangxi Educational Commission (GJJ13058), and the Innovation Fund Designated for Graduate Students of Jiangxi Province (YC2015-B002).

References

Nonvolatile multibit sensors and memories, which are written/erased by different temperatures or bias voltages, are realized successfully in two-terminal devices based on individual ZnO:K,Cl micro/nanowires. The modulation of trap states in nanostructures gives a direction to the development of novel nanodevices in rewritable temperature information sensor and memory.