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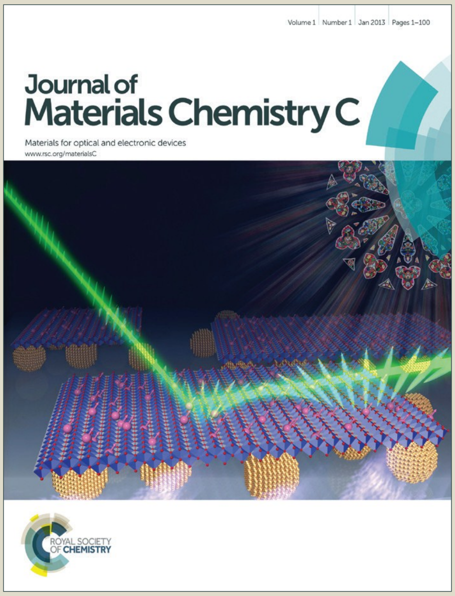

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ARTICLE

Flexible copper wires through galvanic replacement of zinc paste: A highly cost-effective technology for wiring flexible printed circuits

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Conventional electronic circuit wiring methods involve subtractive processes such as etching the copper foils, and thus are inefficient and cause serious environmental problems. The blooming printed electronics technology is expected to be more environmentally benign and have lower cost, due to its additive characteristic. In this paper, we present a simple and efficient strategy to fabricate high performance copper metal fine circuits by a galvanic replacement deposition method. Zinc nanoparticle filled epoxy resin paste is printed onto the substrate film as the seed layer; with a subsequently simple galvanic replacement reaction between Zn and Cu^{2+}, we can obtain a conductive Cu layer that can be further thickened by electroplating. The as-prepared circuits show bulk Cu conductivity, excellent flexibility, adhesion strength and pattern resolution. By adjusting the processing parameters, this technology is compatible to various practical applications, such as flexible circuit boards, RFID tags, touch panels, membrane switches, and photovoltaics, making it a promising solution for low-cost and environmentally friendly fabrication for flexible electronic devices.

Introduction

The last decade has seen an explosive growth of flexible printed circuits and devices, such as large area displays, radio frequency identification (RFID),[1, 2] sensors,[3, 4] wearable electronic devices,[5, 6] photovoltaic devices,[7] smart card and energy storage devices[8] etc. Printed electronics technologies, e.g. inkjet printing,[9, 10] screen printing,[11, 12] gravure printing,[13, 14] transfer printing,[15-17] micro-contact printing,[18] and 3D printing[19, 20] etc., have provided an efficient and inexpensive alternative as the dry & additive fabrication technology for the increasing demands of the flexible electronics. In comparison, conventional wet & subtractive fabrication technologies, such as the copper/aluminum etching process have long been accused for expensive, complicated process, low productivity, high energy consumption characteristics and the involvement of large volume of hazardous wastes.[21, 22]

However, in those cases where high conductivity is obligated, the available pure additive wiring technologies still have limitations. For example, those solution based conductive inks that contain metal nanoparticles (Ag, Au, and Ni etc.) have been used for inkjet printing process; those metal nanoparticles can be printed into desirable patterns and subsequently sintered at relatively low temperatures to achieve highly conductivity.[23,24] Yet a low viscosity of the conductive ink is necessary for inkjet printing, which often involves volatile organic chemicals (VOCs). Additionally, multiple printing cycles are needed to ensure adequate wiring thickness so as to reduce electrical resistance so as to lower down losses.[25] Besides, the high material cost of the commonly used Au and Ag conductive fillers is another limitation for wider applications. As compared, screen printing, gravure printing, and offset printing etc. seem to be more cost-effective and environmentally benign.[25,26] Even though conductive pastes/adhesives have been widely used in the printing electronics technology, Ag pastes, for example, can only reach a conductivity of ~1×10^5 S/cm even with a high filler loading of 80 wt%, which is about six times lower than bulk silver and is much expensive than wiring copper.[26]

Copper (Cu) has long been regarded as the most promising wiring material because it has comparable conductivity to silver while it's about eighty times cheaper.[27] Recent technological advances are mainly focused on the rapid printing and sintering technology for the copper nanoparticle based conductive inks,[25] such as the non-thermal or local surface thermal sintering ones,[28-30] which are aimed to provide lower production cost and better performances. But the poor oxidation resistance of Cu nanoparticles has been a great challenge for wider applications for the copper conductive inks.

An alternative route for wiring Cu-based circuits at low temperature is through electroless plating. The general process of electroless plating involves the surface activation by seeding

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† Electronic Supplementary Information (ESI) available: [details of the Cu^{2+} solutions, the electroplating conditions, the FTIR and DSC-TGA information for the epoxy resin and the Zn-epoxy paste, the lap-shear test and elemental analysis of the p-Cu samples, and the RFID tests,]. See DOI: 10.1039/x0xx00000x

catalytic metal materials on the surface of the substrate to deposit copper on the activated surfaces in an electroless plating bath. By a printing process, such as inkjet printing[31] and micro-contact printing,[32] one can print the catalytic seed layer on the substrate and create Cu film patterns selectively on the seed layer. The palladium (Pd) catalyst is the most widely used material due to its high catalytic activity for initiation of various metal deposition from a wide range of electroless plating baths.[33] Other catalysts or seed materials, such as copper salts/nanoparticles,[34] silver salts/nanoparticles[35] and poly (dopamine)[36] have also been investigated for their lower cost and less pollutive characteristics compared with the Pd method. However, the materials cost, the substrate-dependent adhesion of the catalytic inks and the involvement of hazardous reducing agents are still challenging tasks.[37, 38]

In order to develop highly electrically conductive, low-cost, oxygen resistant and environmentally friendly copper wires by a simple and effective printing technology, herein we demonstrate an effective technology by using zinc (Zn) paste to act as the seed layer which can reduce Cu^{2+} ion into a continuous Cu layer at room temperature. By mixing Zn nano-powder with epoxy resin, this Zn paste can be printed by screen printing technique etc., in which way the Zn seed particles can be firmly adhered on various kinds of substrates e.g. FR4, polyimide (PI) films, poly(ethylene terephthalate) (PET) films and glass boards. Through a galvanic replacement reaction process, a conductive Cu layer can be deposited on the printed Zn patterns. With the subsequent Cu electro-plating process, we can obtain up to 30 µm thick of bulk Cu layer. In this way, we can create a highly conductive copper layer with a wiring resolution of 100 µm, which can be used for general flexible printed circuit (FPC) applications. The circuits show reliable performance of excellent electrical conductivity, mechanical flexibility, foldability, and adhesion strength to the substrates. Additionally, this technology can be conveniently scaled-up to roll-to-roll production.

Experimental

Zn-epoxy paste and Cu^{2+} solution

The Zn paste for screen printing was composed of Zn nanoparticles with the size of 50 nm (Beijing Dk Nano technology Co., LTD) and epoxy resin (Epon 828, Shell), curing agent (methyltetrahydrophthalic anhydride, MTHPA, Nanya Resins), and catalyst (hexamethylenetetramine (99%), Guangzhou Chemical Reagent Factory). The mixing of the resin binder was according to the equal epoxide equivalent weight (EEW) of the epoxy resin and the hydroxyl equivalent weight (HEW) of the curing agent. A small amount of catalyst was added to the resin dispersant to accelerate crosslinking. The Zn loading percentage was 65 wt%. The Zn nanoparticles and resin were mixed with a plantary mixer (HASAI, HM1000) at 800 rpm for 30 min to form the homogeneous Zn paste. The as-prepared Zn paste was degassed in vacuum before use.

$CuSO_4 \bullet 5H_2O$ (AR, Aladdin) and poly (ethylene glycol) (PEG), (M_W: 4000, AR, Aladdin) were selected as the Cu^{2+} source and stabilizer. 23.4 g $CuSO_4 \bullet 5H_2O$ and 23.4 mg PEG4000 were added into 76.6 mL deionized (DI) water (totally 100 g). The pH value was adjusted to 1.5 by using H_2SO_4 before use.

Galvanic replacement deposition of Cu conductive layer and electro-plating thick Cu layer

The Zn seed paste was screen printed onto a PET or PI film, and then the samples were cured at 150 ^{o}C for 20 min. The galvanic replacement reaction was conducted by immersing the samples into the as-prepared Cu^{2+} source solution for 20 min. Then the samples were washed with DI water and dried in an oven (Memmert).

In order to obtain a thicker copper layer, an electroplating process was conducted. The formulation of the electroplating solution is listed in ESI† (table S1). The applied current density was 10 mA/cm^2; the electroplating time was controlled in 5-30 minutes to adjust the thickness of the Cu layer.

Characterizations

The sheet resistance of the copper layer was measured by the four-point-probe method with a resistance analyzer (LorestaGP T610, Mitsubishi Chemical Analytech Co. Ltd.). The tape peeling test was conducted as follows: a Scotch tape (3M, USA) was firmly attached onto the surface of the circuit sample and then quickly peeled off in a vertical-to-film direction. Optical microscopic images were taken on a metallographic microscope (Olympus GX 51). The SEM-EDS

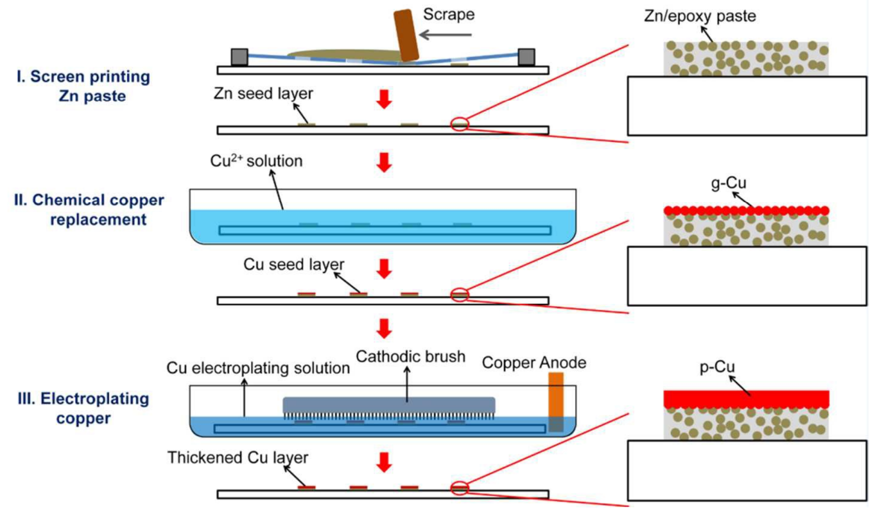

Fig. 1 schematic of the fabrication process.

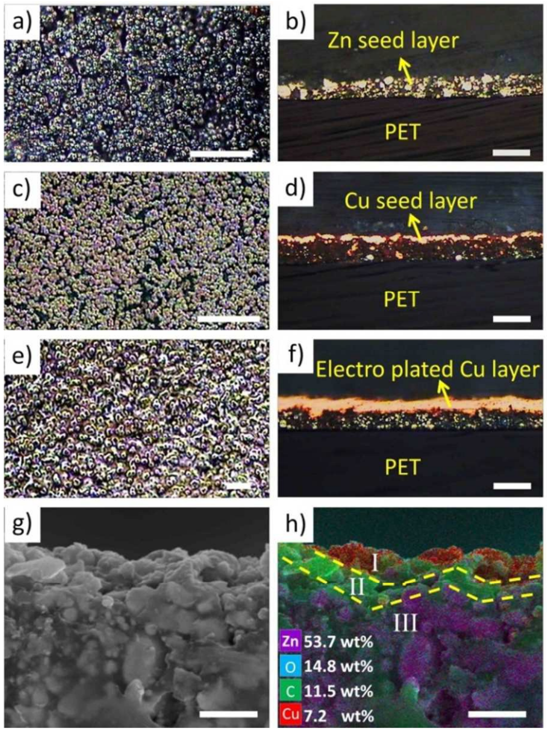

Fig. 2 Optical microscopic images of a) top view of printed Zn paste pattern; b) cross section of Zn pasted pattern; c) top view of Zn paste covered with a thin Cu layer by replacement deposition (g-Cu); d) cross section of the Zn paste covered with a thin Cu layer by galvanic replacement (g-Cu); e) top view of the Cu layer after electro-plating (p-Cu) for 20 min for the sample in c); f) cross section of the Cu layer after electro-plating (p-Cu) for 20 min for the sample in c); and SEM images of g) the cross section of the Zn paste covered with g-Cu; h) the EDS mapping of g). The scale bars of a), c) and e) are 50 μm; the scale bars of b), d) and f) are 20 μm; the scale bars of g) and h) are 5 μm.

analysis was conducted on an FEI Nova NanoSEM450 electron microscope. The differential scanning calorimetry and thermal Gravity analyses (DSC-TGA) of the paste were taken with a NETZSCH STA449 F3 analyzer. The Fourier Transform Infrared Spectroscopy (FTIR) analysis was taken on a NICOLET iS50 FTIR spectrometer. The aging test of the copper conductive pattern was performed in a testing chamber with 85^{o}C/85 relative humidity (RH) for 500 hours and the thermal shocking test was taken at a cyclic changing temperature from -40^{o}C to 125^{o}C for 500 cycles (90 minutes for each cycle).

Results and discussion

Fig. 1 shows the schematic of the Cu galvanic replacement deposition process. Briefly, it needs three steps to create highly conductive Cu conductive patterns: firstly the Zn paste is screen printed on the substrate with desirable patterns, where the epoxy resin contained in the paste acts as both binder and adhesive. Secondly, after the Zn paste is cured, the sample is immersed in the Cu^{2+} ion solution, where the replacement reaction takes place. The Cu^{2+} ions can be reduced into a layer of Cu by Zn and deposited on the surface of the Zn paste layer; some of the copper are embedded into the voids resulting from the elimination of Zn filler particles. The deposited Cu particles interconnect together and form a continuous Cu thin layer (deposited Cu layer by galvanic replacement, marked as g-Cu) which is electrically conductive. Thirdly, a Cu electro-plating process is adopted to thicken the copper layer so that we can obtain a robust and stable Cu metal conductive layer (includes both the Cu layer from galvanic replacement deposition and Cu layer from electro-plating deposition, marked as p-Cu) which is mechanically interlocked on top of the Zn-epoxy film with excellent conductivity. As shown in this figure, a cathodic brush made of stainless steel wires is used to make sure the electrical contact of every single trace.

Fig. 2 presents the morphology of the printed pattern in each step. From Fig. 2a) and b), we can observe that after the Zn paste is cured; the Zn particles are uniformly distributed on the surface, which provides an effective template for the subsequent g-Cu deposition; Fig. 2c) and d) show the in situ reduced g-Cu layer capping on the Zn paste and interconnecting into a percolation network. This continuous g-Cu thin layer shows a resistivity of ~4 × 10^{-4} Ω•cm, which is enough for electro-plating Cu. Fig. 2e) and f) show that the electro-plating deposited Cu (p-Cu) crystals form an uniform p-Cu film, the thickness of which can be adjusted by controlling the deposition time. In this way, we can obtain a highly conductive pure bulk copper (p-Cu) layer with a controllable thickness (5-30 μm) (see ESI† for details).

The formation of the g-Cu can be described as the following equation: $Zn + Cu^{2+} \rightarrow Zn^{2+} + Cu$, which is a simple spontaneous galvanic reaction between Zn seeds and the target metal Cu^{2+} ions. Thus, it needs no catalyst or extra reducing agent, and the reaction can take place immediately at room temperature when immersing the printed Zn seed paste into the Cu^{2+} ion solution. To be noted, some additives (H_2SO_4 and PEG) are needed to control the deposition kinetics by adjusting the pH value and the concentration of the surfactant, so that the deposited Cu can form a uniform thin layer. (see ESI† for details: the Cu^{2+} solution components) Since the Cu^{2+} ion solution is acidic, Zn^{2+} can be easily dissolved. In this way, we can avoid the use of the pricy and environmentally unfriendly palladium (Pd) catalyst and the organic reducing agent that are used in conventional process; and the Cu^{2+}-Zn^{2+}-SO_4^{2}-PEG waste solution can be conveniently recycled. Figure 2g) and f) present the elemental distribution of the sample cross sections of Cu wires after the replacement deposition. From figure 2h), we can observe that in the surface layer which is marked as area I, the element is dominated by Cu, while in the bottom layer which is marked as area III, the elemental composition is C, O, and Zn which refers to the original

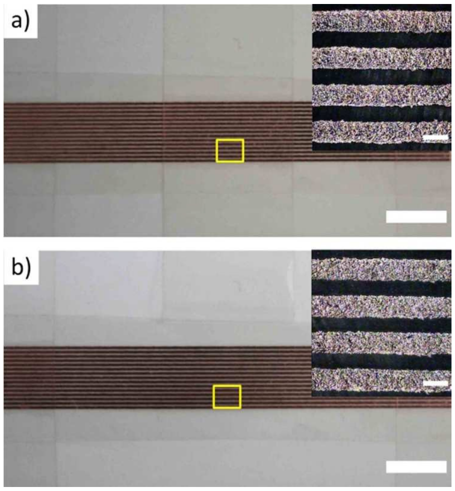

Fig. 3 Tape peeling test of the Cu circuits. a) Before peeling (a scotch tape is adhered on top). b) After peeling. The inserts are optical microscope images of the selected area. The scale bars of a) and b) are 5 mm. The scale bars of the insets are 200 μm.

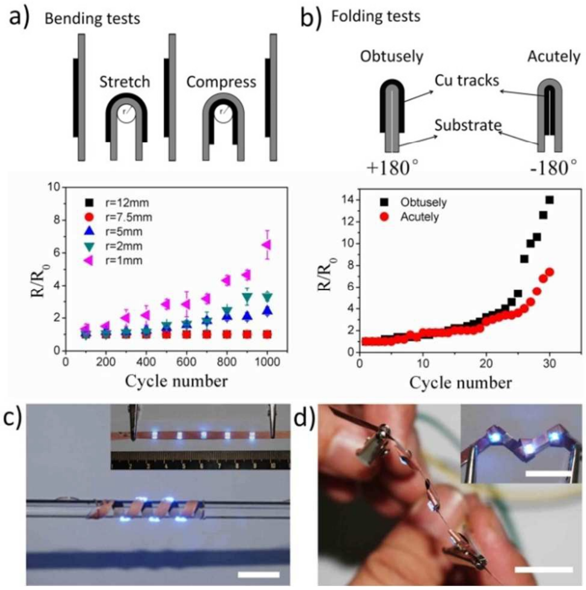

Fig. 4 Flexibility and foldability test results of p-Cu circuits on PET substrate. a) Top: scheme of bending test of p-Cu circuits. Bottom: normalized resistance of Cu circuits v.s. bending cycles. b) Top: scheme of folding test of p-Cu circuits. Bottom: normalized resistance of p-Cu circuits vs. folding cycles. c) The p-Cu conductive tracks integrated with blue LEDs are conformally wrapped around a glass stick. Inserted: unwrapped p-Cu conductive tracks integrated with blue LEDs. The LEDs are turned on. d) The side view of the knotted p-Cu tracks integrated with blue LEDs, the creases are folded. Insert: top view of the knotted p-Cu tracks. The LEDs are turned on. The scale bars are of 2 cm.

Zn-epoxy paste. In the middle layer, which is marked as area II, there is much less Zn than area III, indicating that the Zn in area II has mostly been replaced into Cu.

A strong bonding strength is a basic requirement for fine circuits. The adhesion between the p-Cu layer and the PET substrate was evaluated with the tape peeling test as shown in Fig. 3. Straight and parallel p-Cu circuit lines (200 μm in width and distance) remained intact after we peeled off the tape, and nothing was remained attached on the tape, indicating that a strong mechanical strength of both the p-Cu layer itself and the interfaces between the p-Cu layer, the Zn-epoxy paste and the substrate. This result suggests the excellent robustness of the continuous p-Cu layer. Meanwhile, the mechanical interlocking effect of the rough interface surface between the p-Cu layer and the epoxy resin guarantees the adhesion force among them.[39] (see ESI† for details) Besides, the oxygen-containing functional groups, such as C-O and C=O, on the surface of the epoxy resin may potentially interact with the p-Cu metal and thus further reinforce the interfacial bonding as well.[40-43] (see ESI† for details: FTIR analysis) Therefore, the Zn-epoxy paste layer plays an important role in enhancing the adhesion between metal and the polymer substrate.

The p-Cu conductive patterns fabricated on flexible substrates are highly flexible and foldable. For example, Fig. 4c shows that p-Cu circuits fabricated on PET film can be wrapped around a glass stick (with a diameter of 8 mm) with the integrated light-emitting diodes (LEDs) still work by emitting blue light; furthermore, even when we knot the p-Cu conductive circuits and fold the creases as shown in Fig. 4d, the LEDs can still work very well. In order to systematically evaluate the flexibility and foldability, a series of tests were conducted with the p-Cu circuits (5 cm × 1 mm) printed on PET (75 μm in thickness). In the bending tests, the circuits were bent at different radius of curvature for 1000 cycles and each cycle comprised one stretching and compressing of the p-Cu circuits as shown in Fig. 4a. Meanwhile, their resistance upon bending cycles was measured. The results were normalized as R/R_0 vs. bending cycles as shown in Fig. 4a, of which R is the resistance of p-Cu circuits after bending and R_0 is the resistance before bending tests. It showed that when the p-Cu circuits were bent at a radius of 7.5 mm and 12 mm, R/R_0 remained stable after 1000 cycles. When the bending radius decreased to below 5 mm, R/R_0 increased to different extents. In general, the electrical resistance of the sample increased at the smaller bending radius, and R/R_0 after 1000 cycles increased gradually to about 2, 3.3 and 6.5 at the radius of 5 mm, 2 mm and 1 mm, respectively. This is because that when the p-Cu circuits are repeatedly bent, materials damages such as fatigue cracks tend to occur and accumulate with the bending cycles. Smaller bending radius results in more severe deformation and larger stress that would cause more cracks and faster fatigue of the p-Cu layer.[44] In spite of the resistance increase, a ~6.5 times of R_0 means a low electrical resistivity of ~10^{-5} Ω·cm in the r = 1 mm case, which is applicable for a lot of flexible electronics applications. In the folding tests, the foldability of the p-Cu circuits was evaluated by measuring the resistance while folding the samples acutely (-180°) and obtusely (+180°), as depicted in Fig. 4b. For both folding types, the resistance increased slowly in the first 15-20 cycles, of which R/R_0 was 2.8 for the obtuse type and 2.2 for the acute type after 20 cycles. More drastic resistance increase was found after more bending cycles tests. Besides, the obtuse type showed a faster fatigue than the acute one, indicating that the tensile stress caused more serious damage to the p-Cu film, which was related to the thickness of the substrates as discussed in the previous reports[44, 45]. Similar to the bending tests, folding the p-Cu circuits caused severe deformation and stress in the p-Cu layer resulted in fatigue and even failure of the p-Cu circuits. Also, the excellent foldability of the p-Cu circuits ensures reliable performance for applications in harsh working conditions.

Furthermore, the accelerated aging tests were performed to evaluate the reliability of the p-Cu circuits when being used in severe working environments. The electrical resistance of the sample remained unchanged after being aged in an 85°C/85RH environment for 500 hours (ESI† Fig. S11); no indication of increase of electrical resistance of the sample was found after the sample was aged for 500 cycles of temperature variation between -40°C and 125°C.(ESI† Fig. S12) The excellent aging reliability performance shown in the tests is mainly due to the stable physical and chemical property of the epoxy resin and bulk copper wires, and the fracture toughness and tensile strength of the p-Cu layer, which is even comparable to the conventional copper-clad plated products.

As can be seen, the introduction of epoxy resin plays an important role in this technology; firstly, it enables the Zn seed paste adequate printability for the screen printing process; secondly, the cured epoxy resin has excellent adhesion strength with many kinds of substrate materials, which serves as a binder. Finally, it provides a strong mechanical interconnection to the p-Cu layer, which guarantees excellent reliability of the p-Cu circuits. Overall, the current technology is simple and can be conveniently reproduced.

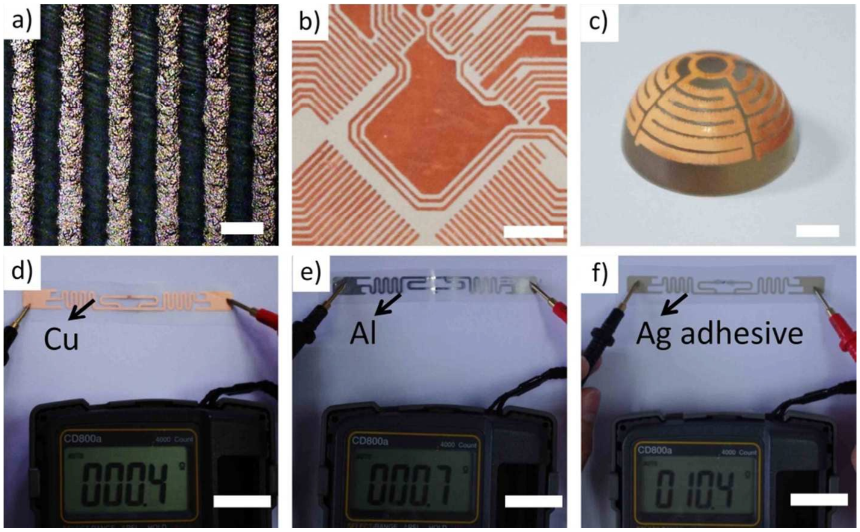

Fig. 5 Circuits made by replacement deposition of Cu. a) optical microscope image of 100 μm width circuits after electroplating Cu. b) A part of electronic circuits, the minimum line width is 200 μm. c) A volumetric antenna prepared by the involvement of pad printing. d) a piece of UHF-RFID antenna sample fabricated with p-Cu. e) A commercial UHF-RFID antenna sample fabricated with Al. f) A piece of UHF-RFID antenna sample fabricated with Ag paste. The scale bar of a) is 200 μm; the scale bar of b) and c) is 5 mm; the scale bars of d)-f) are 20 mm.

We have demonstrated a simple, additive, and Pd-free technology for wiring highly conductive Cu circuits, which is based on inexpensive materials and cost-effective processes. Because of the excellent process compatibility to screen printing and electroplating processes, this technology is promising for large scale and roll-to-roll fabrications. By our method, we can conveniently achieve a printing resolution down to 100 μm (Fig. 5 a), which satisfies the basic requirements for various applications, such as RFID tags, touch pads, and some flexible integrated circuits boards as shown in Fig. 5 b). This wiring resolution is comparable to the best case for conventional lithographic wiring resolution. Through properly adjusting the rheology of the Zn paste, we can integrate some other printing techniques to our current process, such as gravure printing, transfer printing and offset printing, which shows even better printing resolution and cost-effectiveness. We can also fabricate volumetric circuits conveniently by pad printing on a non-planer surface, as shown in Fig. 5 c), which may potentially find advanced radio frequency applications etc.[46, 47]

Fig. 5 d)-f) present the RFID samples with the antennas fabricated with different methods. it is found that the electrical resistance of p-Cu pattern that fabricated by our technology is similar to that of the commercial aluminium (Al) antenna, and is about 26 times smaller than that of the Ag paste (75 wt% of Ag loading) based antenna. In this case, the reading/writing distance for p-Cu RFID is about 3.5 m, similar to the commercial Al one, while the Ag conductive adhesive based antenna only has a reading/writing distance of 1.8 m.（details are shown in ESI† table S2）The excellent performance of the p-Cu based RFID shown in the tests is mainly due to its high conductivity, which is beneficial to reduce signal losses. Therefore, the highly conductive p-Cu circuits fabricated by our technology make them find potentially low cost and high performances electronic device applications.

Concluding remarks and outlook

In summary, we have developed a simple technology combining galvanic replacement and electro-plating processes on Zn seed paste. This simple additive process can lead to the fabrication of high quality conductive Cu wires. The Zn paste that we developed is compatible with various efficient printing techniques, and is simple and inexpensive. Through evaluating the performance and fabricating prototypes, we have demonstrated that the fabricated p-Cu circuits have superior conductivity and reliable performances, which may find immediate electronics applications, such as flexible circuit boards, RFID tags, touch panels, membrane switches, photovoltaics and others.

What's more, following our methodology, this technology can be extended to the combinations of other seed and conductive materials: for example, using iron and nickel etc. as the seed metals and using Ag or Au etc. to replace Cu as the conductive materials. Thereafter, in this case study, we have proposed a simple and easy-to-operate technology for fabricating a wide range of high performance electronic circuits.

Acknowledgements

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Notes and references

1 S. W. Hwang, X. Huang, J. H. Seo, J. K. Song, S. Kim, S. Hage Ali, H. J. Chung, H. Tao, F. G. Omenetto and Z. Ma, *Adv. Mater.*, 2013, 25, 3526-3531.
2 Z. Li, T. Le, Z. Wu, Y. Yao, L. Li, M. Tentzeris, K. S. Moon and C. Wong, *Adv. Funct. Mater.*, 2015, 25, 464-470.
3 S. W. Hwang, J. K. Song, X. Huang, H. Cheng, S. K. Kang, B. H. Kim, J. H. Kim, S. Yu, Y. Huang and J. A. Rogers, *Adv. Mater.*, 2014, 26, 3905-3911.
4 R. C. Webb, A. P. Bonifas, A. Behnaz, Y. Zhang, K. J. Yu, H. Cheng, M. Shi, Z. Bian, Z. Liu and Y.-S. Kim, *Nat. Mater.*, 2013, 12, 938-944.
5 W. H. Yeo, Y. S. Kim, J. Lee, A. Ameen, L. Shi, M. Li, S. Wang, R. Ma, S. H. Jin and Z. Kang, *Adv. Mater.*, 2013, 25, 2773-2778.
6 W. Honda, S. Harada, T. Arie, S. Akita and K. Takei, *Adv. Funct. Mater.*, 2014, 24, 3299-3304.

7 M. Song, D. S. You, K. Lim, S. Park, S. Jung, C. S. Kim, D. H. Kim, D. G. Kim, J. K. Kim and J. Park, *Adv. Funct. Mater.*, 2013, 23, 4177-4184.
8 J. Yeo, G. Kim, S. Hong, M. S. Kim, D. Kim, J. Lee, H. B. Lee, J. Kwon, Y. D. Suh and H. W. Kang, *J Power Sources*, 2014, 246, 562-568.
9 W. Shen, X. Zhang, Q. Huang, Q. Xu and W. Song, *Nanoscale*, 2014, 6, 1622-1628.
10 M. Liu, J. Wang, M. He, L. Wang, F. Li, L. Jiang and Y. Song, *ACS Appl. Mater. Interfaces*, 2014, 6, 13344-13348.
11 W. Wu, S. Yang, S. Zhang, H. Zhang and C. Jiang, *J. Colloid Interface Sci*., 2014, 427, 15-19.
12 K. Jost, D. Stenger, C. R. Perez, J. K. McDonough, K. Lian, Y. Gogotsi and G. Dion, *Energ. Environ. Sci.*, 2013, 6, 2698-2705.
13 D. A. Alsaid, E. Rebrosova, M. Joyce, M. Rebros, M. Atashbar and B. Bazuin, *J. Disp. Technol.*, 2012, 8, 391-396.
14 G. Hernandez‐Sosa, S. Tekoglu, S. Stolz, R. Eckstein, C. Teusch, J. Trapp, U. Lemmer, M. Hamburger and N. Mechau, *Adv. Mater*., 2014, 26, 3235-3240.
15 A. Carlson, S. Wang, P. Elvikis, P. M. Ferreira, Y. Huang and J. A. Rogers, *Adv. Funct. Mater.*, 2012, 22, 4476-4484.
16 T.-I. Kim, M. J. Kim, Y. H. Jung, H. Jang, C. Dagdeviren, H. A. Pao, S. J. Cho, A. Carlson, K. J. Yu and A. Ameen, *Chem. Mater.*, 2014, 26, 3502-3507.
17 C. H. Lee, D. R. Kim and X. Zheng, *Nano Lett.*, 2011, 11, 3435-3439.
18 A. Tabatabai, A. Fassler, C. Usiak and C. Majidi, *Langmuir*, 2013, 29, 6194-6200.
19 J. T. Muth, D. M. Vogt, R. L. Truby, Y. Mengüç, D. B. Kolesky, R. J. Wood and J. A. Lewis, *Adv. Mater.*, 2014, 26, 6307-6312.
20 Y. Zheng, Z. Z. He, Y. X. Gao and J. Liu, *Sci. Rep.*, 2013, 3, 1786.
21 J. La Dou, *Int. J. Hyg. Envir. Heal.* 2006, 209, 211-219.
22 J. Liu, C. Yang, H. Wu, Z. Lin, Z. Zhang, R. Wang, B. Li, F. Kang, L. Shi and C. P. Wong, *Energ. Environ. Sci.*, 2014, 7, 3674-3682.
23 J. Perelaer, R. Abbel, S. Wunscher, R. Jani, T. van Lammeren and U. S. Schubert, *Adv. Mater*., 2012, 24, 2620-2625.
24 S. Jeong, S. H. Lee, Y. Jo, S. S. Lee, Y. H. Seo, B. W. Ahn, G. Kim, G. E. Jang, J. U. Park, B. H. Ryu and Y. Choi, *J. Mater. Chem. C*, 2013, 1, 2704-2710.
25 D. Tobjork and R. Osterbacka, *Adv. Mater.*, 2011, 23, 1935-1961.
26 C. Yang, C. P. Wong and M. M. Yuen, *J. Mater. Chem. C*, 2013, 1, 4052-4069.
27 Y. Lee, J. R. Choi, K. J. Lee, N. E. Stott and D. Kim, *Nanotechnology*, 2008, 19, 415604.
28 J. Perelaer, R. Jani, M. Grouchko, A. Kamyshny, S. Magdassi and U. S. Schubert, *Adv. Mater.*, 2012, 24, 3993-3998.
29 D. Angmo, T. T. Larsen‐Olsen, M. Jørgensen, R. R. Søndergaard and F. C. Krebs, *Adv. Energ. Mater.*, 2013, 3, 172-175.
30 W.-H. Chung, H.-J. Hwang, S.-H. Lee and H.-S. Kim, *Nanotechnology*, 2013, 24, 035202.
31 K. Cheng, M. H. Yang, W. W. Chiu, C. Y. Huang, J. Chang, T. F. Ying and Y. Yang, *Macromol. Rapid Comm.*, 2005, 26, 247-264.
32 P. C. Hidber, W. Helbig, E. Kim and G. M. Whitesides, *Langmuir*, 1996, 12, 1375-1380.
33 D. Zabetakis and W. J. Dressick, *ACS Appl. Mater. Interfaces*, 2012, 4, 2358-2368.
34 M. Charbonnier, M. Romand, Y. Goepfert, D. Leonard and M. Bouadi, *Surf. Coat. Tech.*, 2006, 200, 5478-5486.
35 Y.-C. Liao and Z.-K. Kao, *ACS Appl. Mater. Interfaces*, 2012, 4, 5109-5113.
36 S. Ma, L. Liu, V. Bromberg and T. J. Singler, *ACS Appl. Mater. Interfaces*, 2014, 6, 19494-19498.
37 P. Zhu, Y. Masuda and K. Koumoto, *J. Mater. Chem.*, 2004, 14, 976-981.
38 Y. Chang, C. Yang, X.-Y. Zheng, D.-Y. Wang and Z.-G. Yang, *ACS Appl. Mater. Interfaces*, 2014, 6, 768-772.
39 K. Cho and E. C. Cho, *J. Adhes. Sci. Tech.*, 2000, 14, 1333-1353.
40 C. K. Y. Wong, M. M. F. Yuen and B. Xu, *Appl. Phys. Lett.*, 2009, 94, 263102.
41 W. J. Lee, Y. S. Lee, S. K. Rha, Y. J. Lee, K. Y. Lim, Y. D. Chung and C. N. Whang, *Appl. Surf. Sci.*, 2003, 205, 128-136.
42 C. Wang, L. Xiang, Y. Chen, S. Wang, D. Xiao and W. He, *J. Adhes. Sci. Tech.*, 2015, 1-12.
43 W.-J. Liu, X.-J. Guo and C.-H. Chuang, *Surf. Coat. Tech*., 2005, 196, 192-197.
44 R. S. Guo, Y. Yu, Z. Xie, X. Q. Liu, X. C. Zhou, Y. F. Gao, Z. L. Liu, F. Zhou, Y. Yang and Z. J. Zheng, *Adv. Mater.*, 2013, 25, 3343-3350.
45 H. Y. Wu, S. W. Chiang, W. Lin, C. Yang, Z. Li, J. P. Liu, X. Y. Cui, F. Y. Kang and C. P. Wong, *Sci. Rep.*, 2014, 4, 6275.
46 J. J. Adams, E. B. Duoss, T. F. Malkowski, M. J. Motala, B. Y. Ahn, R. G. Nuzzo, J. T. Bernhard and J. A. Lewis, *Adv. Mater.*, 2011, 23, 1335-1340.
47 C. Pfeiffer, X. Xu, S. R. Forrest and A. Grbic, *Adv. Mater.*, 2012, 24, 1166-1170.

This work demonstrates a galvanic replacement reaction based route to fabricate highly conductive flexible Cu circuits. The Zn/epoxy paste serves as a seed layer as well as interconnects the electroplated Cu layer to the substrate. As a cost-effective and environmentally benign one, this technology can provide down to 100 µm fine Cu lines with a thick Cu layer up to 30 µm.