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Structural reliability evaluation for low-*k* nanoporous dielectric interlayers integrated into microelectronic device†

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As integrated microelectronic circuit device dimensions continue to shrink, low dielectric constant (low-*k*) interlayer dielectrics are required for minimizing RC signal delay, capacitive coupling noise, and power consumption. The implementation of low-*k* materials in an interconnect structure, however, is known to be a very difficult task because of many criteria imposed by the structural functionality and the integration process. Here, we report structural reliability evaluation for the integration of low-*k* nanoporous organosillicate dielectrics into a multilayer structure, involving capping, chemical mechanical polishing (CMP), post-CMP cleaning, and thermal annealing processes. We have successfully investigated the structural reliability of the low-*k* dielectric layer subjected to such the harsh processes using synchrotron grazing incidence X-ray scattering and reflectivity (GIXS and XR) analyses. This study additionally demonstrated that synchrotron GIXS and XR techniques are very powerful tools for providing valuable, accurate insight into the nanopore structure in low-*k* dielectric thin layers and the structural changes with the integration process conditions.

Introduction

Continuous improvements in device density and performance have been achieved by reducing feature size and scaling down device dimensions to the deep sub-micrometer level. The coupling of the inter-metal capacitance effect with line resistivity is now a limiting factor for the ultra-large-scale integration of electric circuits. To resolve this problem, it is necessary to have low dielectric constant (low-*k*) materials with insulation properties for the integration of copper (Cu) interconnects on high performance integrated circuits.[1-4]

One of the most critical challenges during the integration of low-*k* materials in damascene structure rises from the mechanical failures caused by scratching, peeling, and delamination during integration processes such as etching, resist stripping, chemical mechanical polishing (CMP), and post-CMP cleaning. During CMP and post-CMP cleaning, frictions associated with abrasive particles, polishing pressure and shear are known to cause mechanical damages, and chemical damages often occur due to the penetration of slurry residues (containing abrasive particles, slurry pH buffer, and electrolyte salts) and post-CMP cleaning chemicals into the pores of the dielectric layer.[5-11] Such damages in the low-*k* dielectric layers are known to take place at the scales from micrometers to a few nanometers.[12-16]

Thus, damage-free processing and quantitative characterization of any possible damages of the complex interface system in damascene structure significantly dominate the reliability of multilevel interconnects and need to be clarified before practical implementations. In particular, the nanometer scale damages are quite difficult to analyze. Furthermore, evaluating the nanometer scale damages should be nondestructive and accurate, and involve simple yet non-invasive sample preparation.

In this study, we report the first structural reliability evaluation for the integration of low-*k* nanoporous polymethylsilsesquioxane (PMSSQ) dielectric layer into damascene structure using synchrotron grazing incidence X-ray scattering (GIXS) and X-ray reflectivity (XR), which are non-destructive analytical techniques. Low-*k* nanoporous PMSSQ film layers were prepared and then integrated into damascene structures with a bottom etching stop layer, a top capping layer, a diffusion barrier layer, a thin copper (Cu) seed layer and a thick Cu electroplating layer, followed by a series of damascene processes, namely CMP, post-CMP cleaning and annealing (Scheme 1). The synchrotron GIXS and XR analyses were successfully carried out on the low-*k* dielectric layers and the damascene-processed specimens, providing the structural details and changes at a subnanometer level. The non-destructive X-ray analyses confirmed that minor damages were caused by the damascene processes, particularly CMP and post-CMP cleaning with aqueous dilute hydrofluoric acid (dHF). The analyses further found the importance of the presence of a capping layer on the porous low-*k* materials as protection of the porous layer from CMP and post-CMP

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cleaning processes. In addition, this study demonstrated that synchrotron GIXS and XR are very powerful tools for evaluating the integration of low-*k* interdielectric layers into multilayer devices based on damascene processes.

Experimental part

A low-*k* precursor solution (HL02™, LG Chem. Ltd., Daejeon, Korea),[17] which contained PMSSQ precursor and radially multi-branched porogen, was received from LG Chem; the porogen content was 30 wt% with respect to the PMSSQ precursor. The low-*k* precursor solution (5 wt% solid) was spin-coated on silicon (Si) wafers and followed by curing at 200 °C for 10 min and 420 °C for 1 h under nitrogen atmosphere. The resulting low-*k* nanoporous PMSSQ dielectric films (S1 in Scheme 1) were determined to have a refractive index of 1.28 at 633 nm, a dielectric constant of 2.25 at 1 MHz, and a modulus of 6.5 GPa.

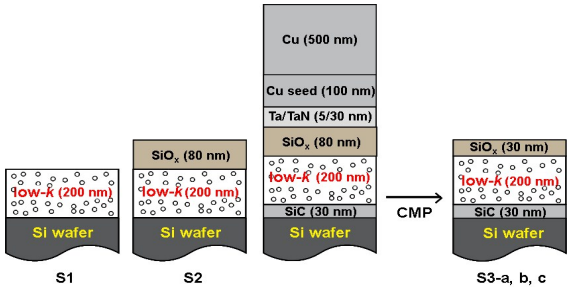
In a previous study we found that silicate (SiO_x) is a good protective capping layer material for low-*k* PMSSQ dielectric layer and, furthermore, its adhesion to the low-*k* dielectric layer can be improved significantly after a carbon dioxide (CO_2) plasma treatment of the dielectric layer surface.[18] Taking this fact into account, a 80 nm thick SiO_x capping layer was deposited on the top of the CO_2 plasma treated low-*k* dielectric layers by thermal deposition of tetraethoxysilane (TEOS) and put under subsequent curing at 400 °C for 2 h in nitrogen atmosphere (S2 in Scheme 1). To realize damascene low-*k* film stack, a multilayer stack structure, Si/SiC(30 nm thick)/low-*k* film(200 nm)/SiO_x(80 nm)/tantalum(Ta, 5 nm)/tantalum nitride(TaN, 30 nm)/Cu seed(100 nm)/Cu(500nm) was introduced. Here, SiC is a good candidate for an etch stop dielectric material in the damascene process. A Ta/TaN layer was deposited onto the SiO_x layer as a barrier by consecutive physical vapour deposition (PVD) process. Cu seed layer was deposited onto the Ta/TaN barrier layer by PVD, followed by final Cu layer deposited via electrochemical deposition.

The Cu layer was removed out using a CMP polisher (Mirra, Applied Materials, Santa Clara, CA, USA) equipped with polyurethane pad (IC1000, Rodel-Nitta, Tokyo, Japan), and the SiO_x layer was further over-polished in part at the same time for 30 nm-thick target. We used an orbital polishing tool with acidic slurry (SiO_2 abrasive and H_2O_2 oxidant) for high-removal-rate under 1.5 psi. The Cu layer was removed in a three-step process: Cu removal with a high rate (200 nm/min), Cu clearing with a medium rate (100 nm/min), and barrier removal with a low rate (20 nm/min).

The damascene-processed low-*k* dielectric film stacks were cleaned in three different ways to prevent Cu contamination and slurry residue. A set of the films stacks were cleaned with dHF solution (0.1 wt%) and followed by rinsing with dionized (DI) water and drying at 80 °C for 30 min (S3-a in Scheme 1). Another set of the film stacks were cleaned using only DI water and dried at 80 °C for 30 min (S3-b in Scheme 1). The other set of the film stacks were cleaned using only DI water and dried at 80 °C for 30 min, followed by thermal annealing at 400 °C for 3 h in a vacuum to completely remove all possible residual organics and absorbed water in the low-*k* layer (S3-c in Scheme 1).

Synchrotron GIXS measurements were performed at the 3C beamline[19-22] of the Pohang Accelerator Laboratory (PAL), Pohang University of Science & technology. In the GIXS measurements, the sample-to-detector distance (SDD) was 1172 mm, and an X-ray source with a wavelength λ of 0.1608 nm and a two-dimensional (2D) charge-coupled detector (CCD: Mar USA, Evanston, IL, USA) were used. From the measured 2D GIXS patterns, one-dimensional (1D) scattering profiles were extracted at a vertical exit angle α_f of 0.18° and a horizontal exit angle $2\Theta_f$ of 0.34° respectively. The obtained in-plane and out-of-plane GIXS profiles were quantitatively analyzed using GIXS formulas derived previously.[19,23]

Synchrotron XR measurements were carried out at the 3D beamline[23-25] of PAL. An X-ray radiation source (λ = 0.154 nm) was used. The measured XR profiles were normalized to the intensity of the primary beam, which was monitored by an ionization chamber. The XR data were analyzed by a least square fitting procedure of parameterized model electron density profiles to the experimental data. In the XR data analysis we applied a recursive formula given by Parratt's dynamical theory,[24,26] which properly incorporates absorption, refraction, and multiple scattering effects. Interfacial roughness was additionally determined by introducing Névot–Croce damping factors into the recursive formula, assuming Gaussian smearing functions.[27]



Scheme 1 Schematic cross-sections of the low-*k* nanoporous PMSSQ films (S1) and their stacks with other materials (S2; S3-a, b and c). The stacked specimens in a damascene structure were undergone CMP process and followed by post-CMP cleaning processes: S3-a, cleaned with dHF solution and subsequently with DI water; S3-b, cleaned with only DI water; S3-c, cleaned with only DI water and followed by thermal annealing at 400 °C for 3 h under vacuum. The cleaned S3-a and b stacks were further dried at 80 °C for 30 min.

Table 1 Process conditions after the integration for low-*k* films

Sample	Process		
	CMP	Post-CMP cleaning	Post-CMP annealing
S1	-	-	-
S2	-	-	-
S3-a	done	dHF [a] + DI water [b]	-
S3-b	done	DI water	-
S3-c	done	DI water	400 °C/30 min

[a]Dilute hydrofluoric acid (0.1 wt%). [b]Deionized water.

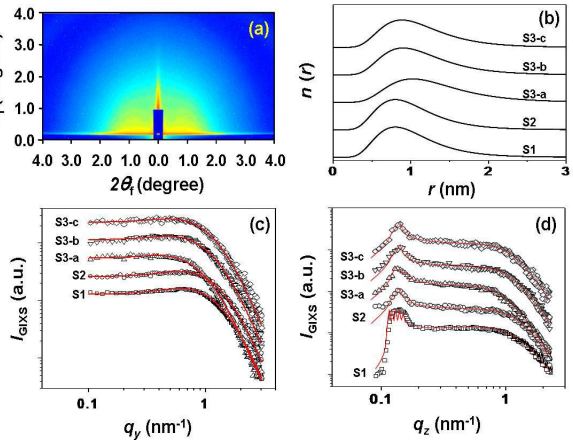


Fig. 1 (a) A representative of the measured 2D GIXS patterns, which was obtained at an incidence angle α_i of 0.18° for a 200 nm thick nanoporous low-*k* film (S1 in Scheme 1); (b) pore radius *r* and distribution determined from the analysis of the GIXS data in (c) and (d); (c) in-plane GIXS profiles extracted along the q_y direction (i.e., $2\theta_f$ direction) at α_f = 0.18° from the 2D GIXS patterns measured for the low-*k* film and the dielectric stacks in Scheme 1; (d) out-of-plane GIXS profiles extracted along the q_z direction (i.e., α_f direction) at $2\theta_f$ = 0.34° from the 2D GIXS patterns of the low-*k* film and dielectric stacks. The symbols are the measured data and the solid lines represent fits to the data.

Results and discussion

The low-*k* dielectric films as well as the low-*k* stacks (Scheme 1) were examined using synchrotron GIXS technique to investigate their structures and structural changes after SiO_x capping, CMP, post-CMP, cleaning and thermal annealing of which the details are described in Table 1. Fig. 1a shows a representative of the 2D GIXS patterns measured from the S1 film specimens (i.e., as-cured low-*k* nanoporous PMSSQ films). Similar 2D GIXS patterns were observed for the low-*k* dielectric film stacks. It features a weak structure factor around $2\theta_f = 1°$ which is apparent in the in-plane scattering profiles shown in Fig. 1c. The weak but distinguishable structural interference originates not from ordering or random distribution but from the correlation between neighbouring pores in the films. The analysis of pore structure considered inter-pore structure factor with an approach using a hard sphere model and an approximation that the pores are locally monodispersed.[19,28,29] As shown in Fig. 1c and 1d, the in-plane and out-of-plane scattering profiles could be satisfactorily fitted with the GIXS formula derived for spherical pore model; details of the GIXS formula and data analysis are given in Supplementary Information. The obtained pore size distributions are displayed in Fig. 1b. The analysis results collectively indicate that the pores generated in the low-*k* film layers were spherical and had a sharp interface with the PMSSQ matrix. The obtained structural parameters are summarized in Table 2.

The low-*k* dielectric stack specimens were further subjected to XR analysis. As shown in Fig. 2a and 2b, the measured XR profiles present high frequency Kiessig fringes over the whole range of q_z (= $(4\pi/\lambda)\sin\theta_i$, where θ_i is the grazing incidence angle of incoming X-ray beam with respect to the film plane) and additionally display the critical angles of the individual layers and the substrate at q_z = 0.20 to 0.35 nm^{-1}. The XR profiles were satisfactorily analyzed, using the Parratt algorithm.[24,26] The XR analysis results are given in Table 2 and Fig. 2c and 2d.

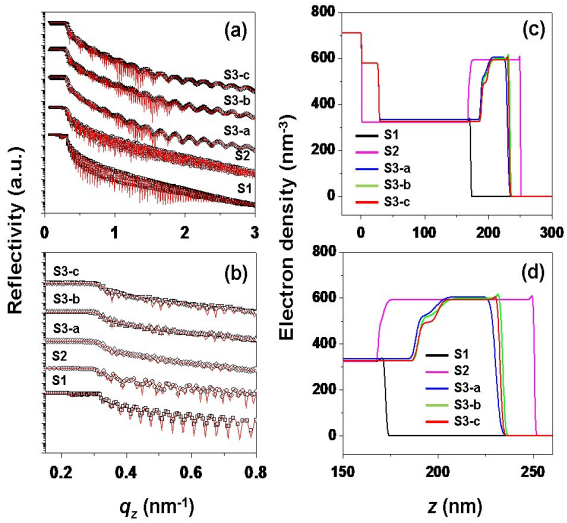


Fig. 2 X-ray reflectivity profiles measured for the low-*k* nanoporous PMSSQ film (S1) and dielectric stacks (S2, S3-a, S3-b and S3-c): (a) entire reflectivity profiles; (b) magnifications of the region of q_z = 0.15° to 0.18° in (a). The symbols are the measured data and the solid lines represent fits to the data. Electron density profiles of entire range along the film thickness direction of the low-*k* film and the dielectric stacks, which were determined from the analysis of the data in (a) and (b): (c) entire profiles from Si substrate to air; (d) magnifications of the region around the low-*k*/SiO_x interface and SiO_x surface.

The as-cured low-*k* porous PMSSQ film was characterized by $\bar{r}$ = 1.04 nm (average pore radius), $\rho_{e,av}$ = 323 nm^{-3} (average electron density) and *P* = 22.8 % (porosity with respect to the PMSSQ film itself as-cured without porogen loading) (S1 in Table 2). In addition, the presence of a very thin but relatively dense skin layer was confirmed; t_s = 2.2 nm (thickness), $\rho_{e,s}$ = 353 nm^{-3}, σ_{surf} = 0.73 nm (surface roughness). This skin layer might be formed by thermal curing of a portion of PMSSQ precursor itself, which was segregated toward the free surface from the PMSSQ precursor/porogen mixture. The $\rho_{e,s}$ value of the skin layer, however, is still lower than that of the as-cured PMSSQ film (419 nm^{-3}) without porogens.

The nanopores formed in the low-*k* dielectric layer were found to be preserved throughout the CO_2 plasma treatment and SiO_x capping layer deposition process (S2 in Table 2). A denser skin layer ($\rho_{e,s}$ = 476 nm^{-3} and t_s = 2.7 nm) was found to form in the low-*k* dielectric layer, however. Moreover, the skin layer in contact with the SiO_x layer had an interfacial roughness σ_{interf} of 1.60 nm, which was larger than the surface roughness before the CO_2 plasma treatment and SiO_x layer deposition. This denser skin layer with high interfacial roughness might originate from the CO_2 plasma treatment, rather than the SiO_x capping layer formation process.

Table 2 GIXS and XR analysis results for low-*k* nanoporous PMSSQ dielectric layers and their integrated stack specimens

Specimen	Pore size and size distribution			Thickness (nm)				Roughness (nm)		Electron density (nm^{-3})						P [k] (%)
				SiO_x		Low-*k*				SiO_x			Low-*k*			
	r_0 [a] (nm)	σ [b]	$\bar{r}$ [c] (nm)	t_s [d]	t_i [e]	t_s	t_i	σ_{surf} [f]	σ_{interf} [g]	$\rho_{e,s}$ [h]	$\rho_{e,i}$ [i]	$\rho_{e,av}$ [j]	$\rho_{e,s}$	$\rho_{e,i}$	$\rho_{e,av}$	
S1	0.80	0.415	1.04	-	-	2.2	169.0	0.73	-	-	-		353	323	323	22.8
S2	0.80	0.415	1.04	1.7	77.4	2.7	167.4	0.50	1.60	619	593	594	476	323	325	22.3
S3-a	1.03	0.419	1.34	2.9	28.7	10.2	160.3	2.01	3.84	628	605	607	518	335	346	17.4
S3-b	0.90	0.415	1.17	3.1	30.0	11.0	161.7	1.03	3.82	626	599	593	516	326	338	19.3
S3-c	0.89	0.415	1.15	3.0	29.6	10.5	161.3	1.16	2.25	623	594	596	493	326	336	19.8

[a]Pore radius determined from the peak maximum of the radius r and the size distribution σ of pores. [b]Width of the radius r and the size distribution of primary pores. [c]Average pore radius determined from the radius r and the size distribution of pores. [d]Thickness of skin layer. [e]Thickness of bulk layer. [f]Surface roughness. [g] Interfacial roughness between SiO_x and low-*k* layer. [h]Electron density of skin layer. [i]Electron density of inner part. [j]Average electron density of film including both skin and bulk layer. [k]Relative porosity estimated from the electron density of the film with respect to the electron density (419 nm^{-3}) of the PMSSQ film itself prepared without porogen loading.

The SiO_x capping layer was characterized to have $\rho_{e,av}$ of 594 nm^{-3}, which was much higher than that of the low-*k* layer. A dense skin layer ($\rho_{e,s}$ = 619 nm^{-3} and t_s = 1.7 nm) was also confirmed to be present in the SiO_x capping layer. The skin layer had σ_{surf} = 0.50 nm, which was relatively smaller (i.e., smoother) than that of the low-*k* layer before the CO_2 plasma treatment and SiO_x deposition. In the S2 specimen, the SiC etching stop layer was additionally characterized to have an electron density ρ_e of 578 nm^{-3}.

In the S3-a specimen, the SiO_x capping layer revealed some changes in the skin layer. In fact, this skin layer was newly formed by the CMP and subsequent cleaning process after the damascene structure formation as shown in Scheme 1. The new skin layer was characterized to have t_s = 2.9 nm, $\rho_{e,s}$ = 628 nm^{-3} and σ_{surf} = 2.01 nm. Overall, this skin layer was thicker, denser and rougher, compared to that formed in the as-prepared SiO_x capping layer. Different from the skin layer, the inner part exhibited structural characteristics identical with those in the as-prepared SiO_x capping layer. These results indicate that the CMP and subsequent cleaning process, including dHF cleaning, DI water rinsing and drying, inevitably generated a new skin layer but could not cause any changes in the main part of SiO_x capping layer.

Similar new skin layer formations were observed in the S3-b and c specimens. The inner part of the SiO_x layer was also confirmed to be unchanged but the t_s values were slightly larger and the σ_{surf} values were almost a half of that in the SiO_x layer of the S3-a specimen. These different characteristics in the skin layers might be caused by the differences in the cleaning processes after the same CMP process. In fact, there were two differences in the cleaning processes: the usage of dHF solution for S3-a specimen and the thermal annealing at 400 °C for 3 h for S3-c specimen. The SiO_x layers in the S3-b and c specimens showed similar skin layer features. These results collectively suggest that the skin layer formed in the SiO_x capping layer of the S3-a specimen have experienced a certain level of chemical etching by the dHF solution used in the post-CMP cleaning process.

The results above collectively inform that the SiO_x capping layer made an important role as the protection layer for the low-*k* nanoporous dielectric layer from the very harsh CMP process and the post-CMP cleaning processes.

Different from the SiO_x layer, the low-*k* nanoporous dielectric layer in the damascene structures was found to have some discernible structural changes brought by the CMP and post-CMP cleaning processes, as shown in Fig. 1b-d and 2d and Table 2. In the S3-b specimen, the nanopores in the low-*k* layer experienced 12.5% increase in size and slightly broader size distribution. The skin layer was thickened by 307.4 % and densified by 8.4 %. σ_{interf}, the roughness of the interface in contact with the SiO_x capping layer, was also increased by 138.8 %. Nevertheless, the main part of low-*k* layer revealed an electron density $\rho_{e,i}$ of 326 nm^{-3}, which is comparable to that of the unprocessed sample (323 nm^{-3}). These results collectively indicate that the low-*k* layer in the damascene structure was intact under protection by the SiO_x capping layer from the harsh CMP process but went under some sacrificial damages in a depth of 11 nm from the interface in contact with the SiO_x layer by the CMP process. The damage with 11 nm depth might be attributed to the collapse of the nanopores under the downward and shear stresses generated during the CMP process. Due to the mechanically densified skin layer, the overall porosity P of the low-*k* layer was reduced to 19.3 % from 22.8 %.

The degree of damages was slightly more pronounced in the post-CMP cleaning process including dHF treatment (S3-a specimen). Furthermore, the main part of low-*k* layer became slightly dense after the cleaning process. These results suggest the usage of dHF solution in the post-CMP cleaning process causes a minor negative effect on the low-*k* layer. As a result, the P value of the low-*k* layer was further reduced to 17.4 %.

Both the σ_{interf} and $\rho_{e,s}$ values were reduced and the $\rho_{e,i}$ value remained unchanged in the S3-c specimen compared to those in the S3-b specimen. These values inform that the thermal-annealing after the DI water cleaning makes a positive contribution of

reducing any damaged parts in the low-*k* layer in a certain level. Therefore, the *P* value of the low-*k* layer was slightly increased to 19.8 %.

Overall, the GIXS and XR analysis results provide important features about the integration process of low-*k* nanoporous interdielectric layers into the multilayer microelectric devices fabricated by damascene process including very harsh CMP process and subsequent cleaning process as follows.

First, the SiO_x layer, which can be fabricated from TEOS or any other sources, demonstrated excellent structural and chemical stability and further very good process compatibility to CMP process.

Second, the SiO_x layer has proven its role and performance level as an excellent protection layer for low-*k* nanoporous dielectric layer. Despite the aid of SiO_x protection layer, the CMP process caused the nanopores to collapse in the low-*k* layer with a depth of ca. 11 nm from the interface in contact with the SiO_x protection layer. The results suggest that during the CMP process, the downward and shear stresses generated by the CMP were strong enough to penetrate with depth of 11 nm into the low-*k* layer through the SiO_x protection layer. Thus, damage minimization in the low-*k* layer needs optimized CMP process with lesser downward and shear stresses, which may require longer processing time.

Third, the SiO_x layer is a dielectric material and has a dielectric constant higher than that of the low-*k* layer. Therefore, SiO_x layer with minimal thickness throughout the CMP process would bring improvements. It also may be eliminated via etching process as a post-CMP treatment if necessary.

Fourth, the usage of dHF in the post-CMP cleaning process was found to bring negative contribution to the low-*k* layer. DI water, however, was enough to clean out the undesired materials after the CMP process. Therefore, the usage of dHF is not recommended for the post-CMP cleaning process. Otherwise, dHF needs to be used sparingly or more dilute solution of HF may be used.

Fifth, the 400 °C thermal-annealing in vacuum in the post-CMP cleaning process was confirmed to bring positive contribution via eliminating any damages in the low-*k* layer caused by the harsh CMP process. Thus, thermal-annealing step is recommended as the final step of post-CMP cleaning process.

Finally, with the aid of SiO_x capping layer the nanoporous PMSSQ dielectric material demonstrated an excellent feasibility as a low-*k* interdielectric layer candidate for the fabrication of advanced multilayer-structure microelectronic devices.

Conclusions

In this study, a low-*k* nanoporous PMSSQ dielectric material was successfully fabricated on Si substrates as damascene-structured multilayer stacks through the formations of a SiC etching barrier layer, a SiO_x capping layer, a Ta/TaN barrier layer, a Cu seed layer and an electroplated Cu layer. The multilayer stacks were subjected to a damascene process, including very harsh CMP process and subsequent cleaning processes. The damascene-processed stack specimens were quantitatively characterized for the first time by using synchrotron GIXS and XR. These GIXS and XR analyses provided structural details on the damascene-processed dielectric stacks, which are essential for the structural reliability assessment of low-*k* nanoporous PMSSQ dielectric layer integration into advanced multilayer-structure microelectronic devices fabricated via a damascene-process based on CMP.

Overall, the low-*k* nanoporous PMSSQ dielectric with the aid of SiO_x capping layer demonstrated excellent compatibility to the CMP, which is the mainly harsh step in the damascene process required in the production of advanced multilayer-structure microelectronic devices. Moreover, the PMSSQ dielectric retained its nanoporous structure throughout the CMP processes, providing advantageous low-*k* property essential for the reduced feature size and the scaled down device dimensions.

In addition, the strategy of combining the GIXS and the XR techniques was succeeded as a very powerful, nondestructive tool to assess low-*k* dielectric layer and its integration into microelectronic circuits in complex multilayer-structures.

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